Applications Note: SY8718A1

High Efficiency,23V,2.0A Synchronous Step Down Regulator For Dimmable LED Driver

General Description

The SY8718A1 is a high efficiency synchronous step-down LED regulator that achieves up to 2.0A output current. It operates at 1MHz and integrates two very low $R_{DS(ON)}$ power switches to minimize and reduce the external components.

It supports the PWM dimming duty 5%-100% to achieve dimmable LED lighting application.

Ordering Information

SY8718 □(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY8718A1ADC	TSOT23-6	----

Features

- Wide Input Range: 4V-23V
- Up to 2.0A Output Current Capability
- Low $R_{DS(ON)}$ for Internal Switches
  High Side/Low Side:125mΩ/75mΩ
- Fixed 1MHz Switching Frequency
- Cycle by Cycle 3.5A Peak Current Limit for High Side and 2.5A Valley Current Limit for Low Side
- High Accuracy for Low Dimming Scale
- Output Voltage Discharging
- Over Temperature Protection
- Compact Package: TSOT23-6

Applications

- DVR Or NVR(IP Camera) System Application
- 12VDC Lighting

Typical Applications

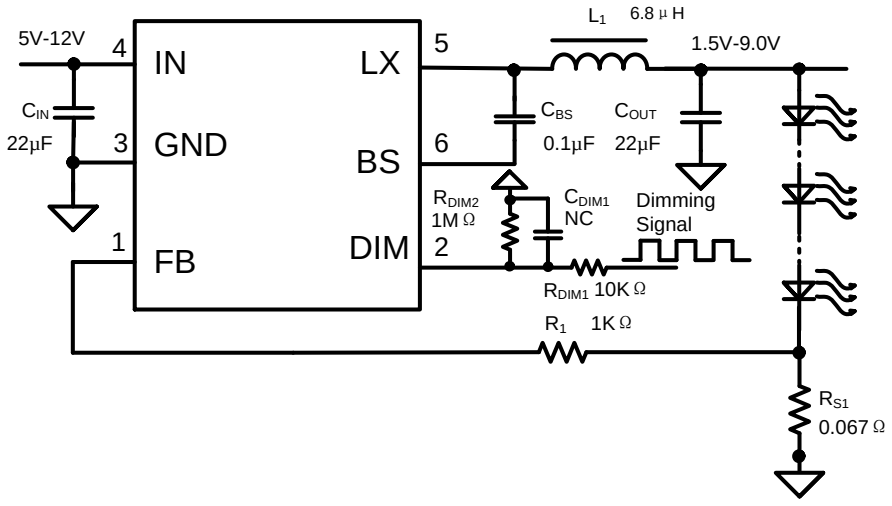
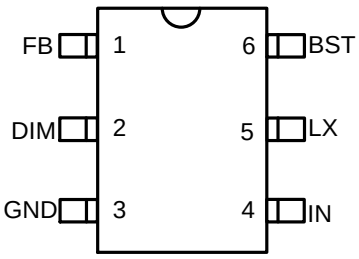


Figure.1 Schematic

Pinout (Top View)



(TSOT23-6)

Top Mark: Wr ***xyz***, **(**Device code: Wr; ***x=year code, y=week code, z= lot number code*****)**

Pin Name	Pin Number	Pin Description
FB	1	Output current feedback pin. The output current: I_{OUT} =0.1V/ R_S
DIM	2	Dimming signal input. The PWM dimming duty range: 5%-100% Support the dimming frequency from 20KHz to 500KHz
GND	3	Ground pin
IN	4	Input supply pin. Decouple this pin to GND pin with a 1μF ceramic cap
LX	5	Switching node pin. Connect this pin to the inductor
BST	6	Boot-strap pin. Supply for top side gate driver. Decouple this pin to LX with a 0.1μF ceramic cap

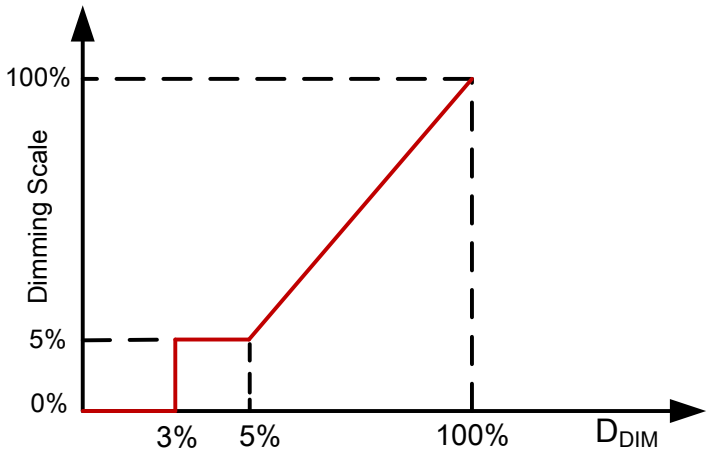


Figure.2 Ideal dimming curve of SY8718A1

Block Diagram

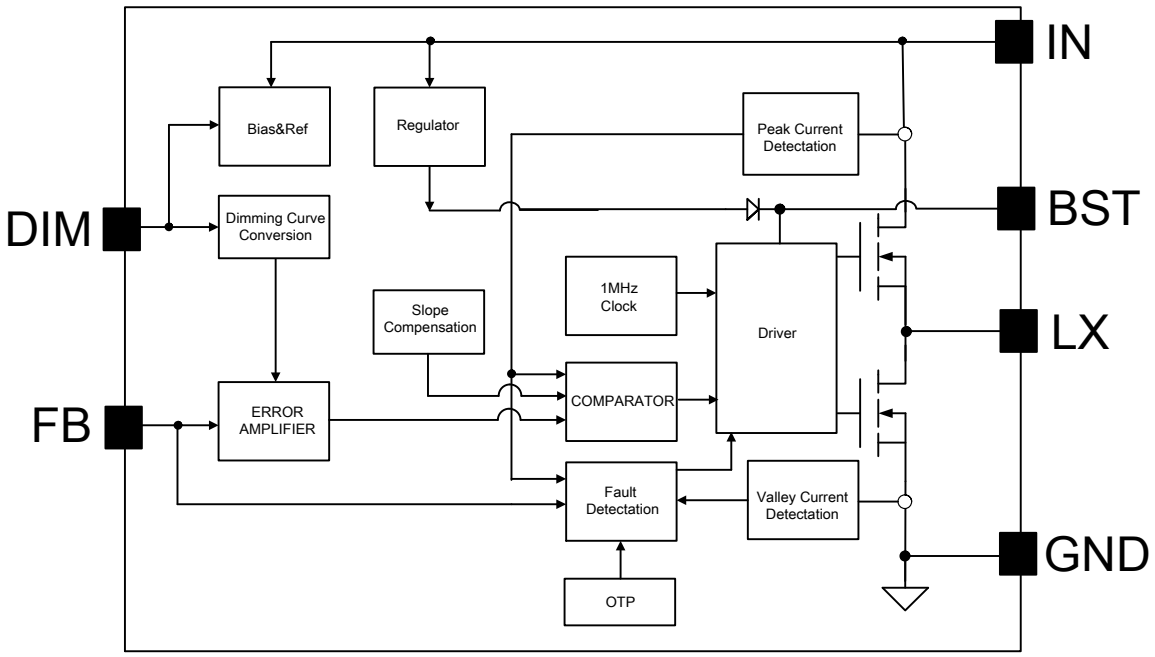


Figure.3 Functional Block Diagram

Absolute Maximum Ratings (Note 1)

IN, DIM, FB ---------- -0.3V to 25V
LX ---------- -0.3V (*1) to 25V (*2)
BST-LX ---------- -0.3V to 4V
Power Dissipation, PD @ TA = 25°C TSOT23-6 ---------- 1.5W
Package Thermal Resistance (Note 2)

Θ_{JA} ---------- 66°C/W

Θ_{JC} ---------- 15°C/W
Junction Temperature Range ---------- -40°C to150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
(*1) LX Voltage tested down to -3V<20ns
(*2) LX Voltage tested up to +25V<20ns

Recommended Operating Conditions (Note 3)

Supply Voltage IN ---------- 4V to 23V
Junction Temperature Range ---------- -40°C to 125°C

Electrical Characteristics

(V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 2.0A T_A = 25°C unless otherwise specified)

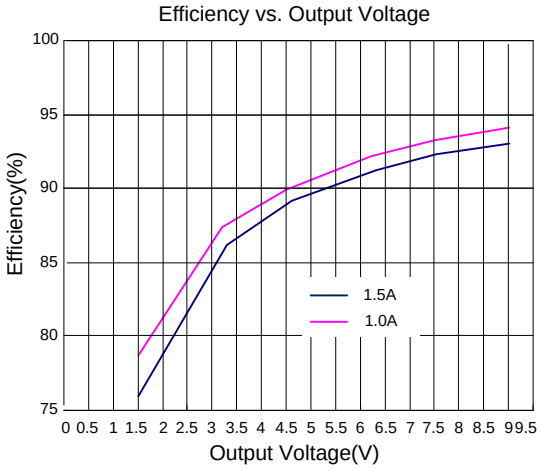
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
IN Pin						
Input Voltage Range	V_{IN}		4.0		23.0	V
IN UVLO Rising Threshold	V_{UVLO}		3.5		4.0	V
UVLO Hysteresis	V_{UVLO_HYS}			0.2		V
Quiescent Current	I_Q	V_{DIM}=2V, V_{FB}=0.105V		2.5		mA
FB Pin						
Feedback Reference Voltage	V_{FB}	D_{DIM}=100%, V_{IN}=12V, V_{OUT}=2.0V, I_{OUT}=1.0A	96	99	102	mV
		D_{DIM}=100%, V_{IN}=12V, V_{OUT}=8.0V, I_{OUT}=1.0A	98	101	104	mV
Feedback Min Reference Voltage	V_{FB_MIN}	D_{DIM}=5%	3	5	7	mV
Integrated Power Switches						
High Side FET $R_{DS(ON)}$	$R_{DS(ON)1}$			125		mΩ
High Side FET Peak Current Limit	I_{LIM_HIGH}	T_{ON} <300ns		3.5		A
Low Side FET $R_{DS(ON)}$	$R_{DS(ON)2}$			75		mΩ
Low Side FET Valley Current Limit	I_{LIM_LOW}			2.5		A
DIM Pin						
PWM Dimming Duty Range	D_{DIM}		5%		100%	
Dimming ON Threshold	V_{DIM_ON}				1.5	V
Dimming OFF Threshold	V_{DIM_OFF}		0.4			V
BST Pin						
Bias Voltage For High FET Driver	V_{BST_LX}	4V≤V_{IN}≤23V		3		V
Operating Frequency	F_S		0.8	1.0	1.2	MHz
Min ON Time	T_{ON_MIN}			80		ns
Max Duty Cycle	D_{MAX}		89%	92%		
Thermal Shut Down						
Thermal Shutdown Temperature	T_{SD}			150		℃
Thermal Shutdown Hysteresis	T_{HYS}			15		℃

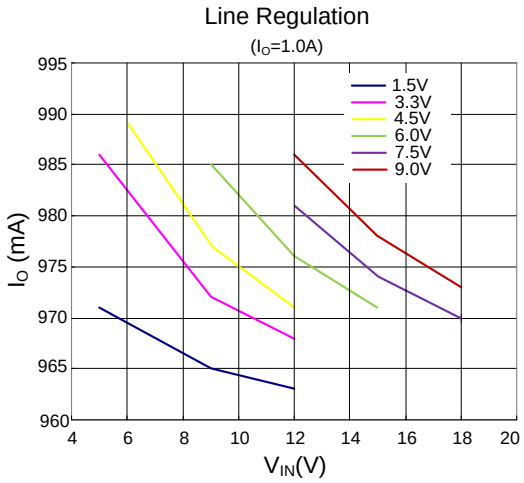
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

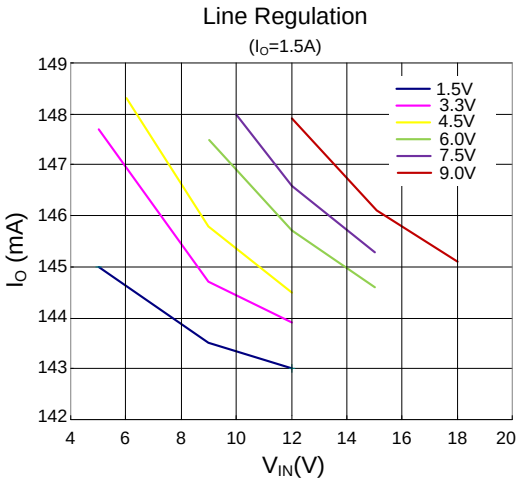
Note 2: θJA is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

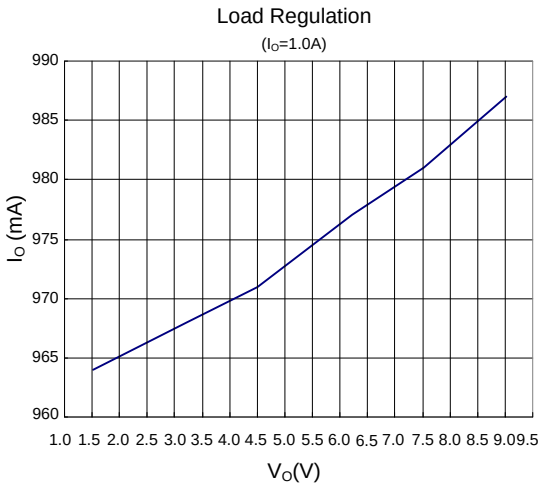
Note 3: The device is not guaranteed to function outside its operating conditions.

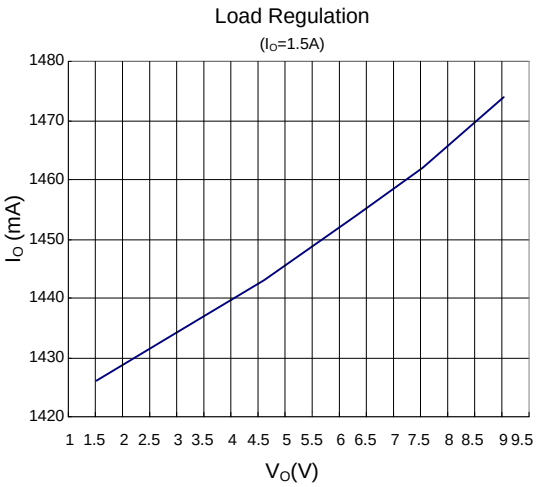
Typical Operation Characteristics





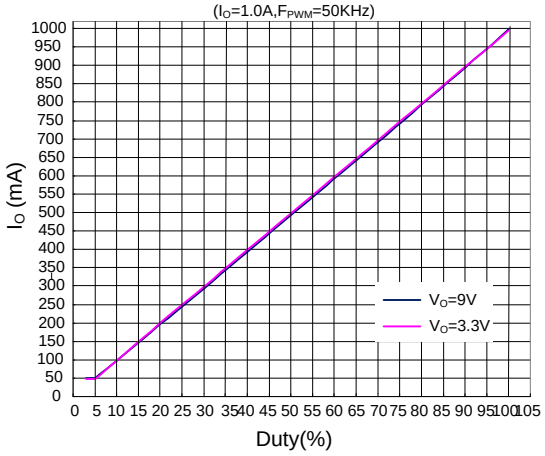






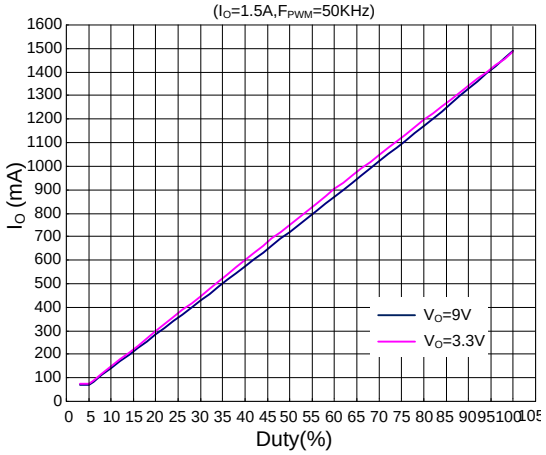
Dimming Curve

(I_O=1.0A,F_{PWM}=50KHz)

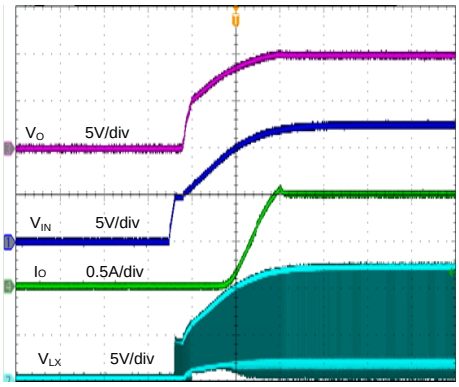


Dimming Curve

(I_O=1.5A,F_{PWM}=50KHz)

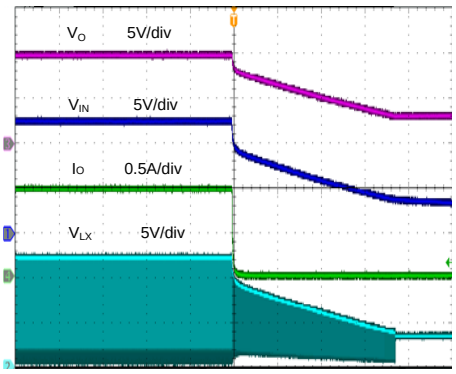


Startup



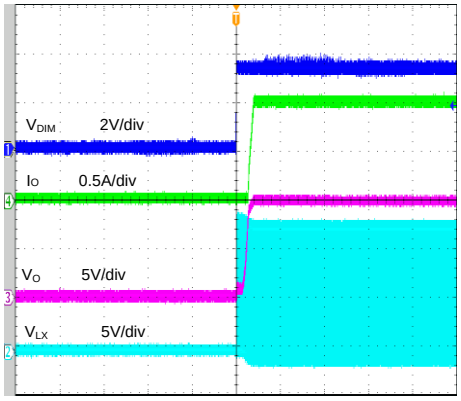
Time (2ms/div)

Shutdown



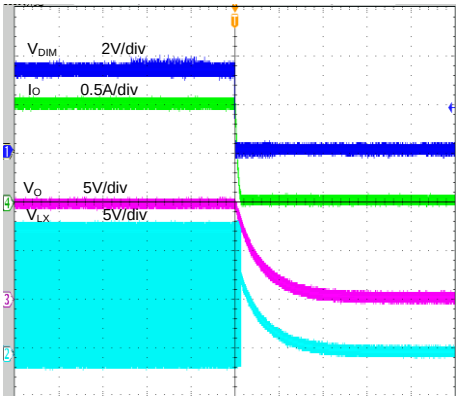
Time (20ms/div)

DIM ON



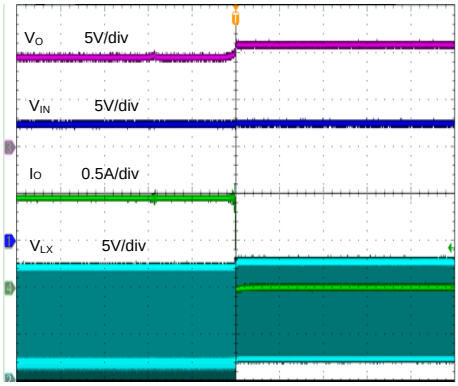
Time (2ms/div)

DIM OFF



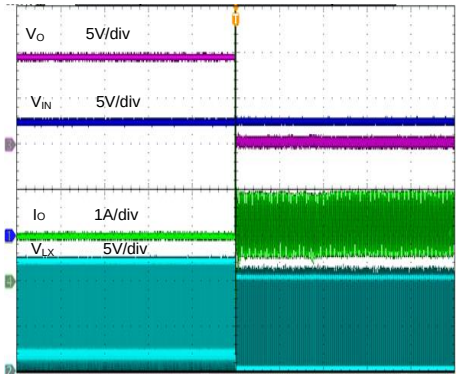
Time (2ms/div)

Open LED Test



Time (2ms/div)

Short LED Test



Time (2ms/div)

Operation

The SY8718A1 is a 23V and up to 2A constant output current capability synchronous buck regulator IC that integrates two very low $R_{DS(ON)}$ power switches to minimize the switching transition loss and conduction loss. The high switching frequency is used to minimize the external inductor and capacitor size to reduce the cost and simplify the design. It supports the PWM dimming duty from 5%-100% for DIM pin to achieve dimmable LED lighting application.

Application Information

It is rather simple to design the power circuit because of the high integration of SY8718A1.

Current Sensing Resistor R_{S1}

Choose the proper R_{S1} to program the output current I_{OUT}

$$R_{S1}=\frac{0.1V}{I_{OUT}} (1)$$

To prevent the FB pin from damaging caused by output abruptly shorted, the R_1 is needed.

Input Capacitor C_{IN}

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS}=I_{OUT}\times\sqrt{D\times(1-D)} \quad (2)$$

A typical X7R or better grade ceramic capacitor with suitable capacitance should be chosen to handle this ripple current well. To minimize the potential noise problem, place this ceramic capacitor really close to the IN and GND pins. Caution should be taken to minimize the loop area formed by C_{IN} and IN/GND pin.

Output Capacitor C_{OUT}

The output capacitor is selected to improve the loop stability and handle the output current ripple noise requirements. For the best performance, it is recommended to use a X7R or better grade ceramic capacitor greater than 10uF capacitance.

Main Inductor L_1

There are several considerations in choosing this inductor.

1) Select the proper inductance to ensure the loop stability.

2) It is suggested to choose the ripple current to be about 40% of the maximum output current as long as the loop stability allows. The inductance is calculated as:

$$L_1=\frac{V_{OUT}\times(1-\frac{V_{OUT}}{V_{IN,MAX}})}{F_S\times I_{OUT,MAX}\times 40\%} \quad (3)$$

Where Fs is the switching frequency and $I_{OUT,MAX}$ is the full scale LED current.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN}>I_{OUT,MAX}+\frac{V_{OUT}\times(1-\frac{V_{OUT}}{V_{IN,MAX}})}{2\times F_S\times L_1} \quad (4)$$

Boot-strap Capacitor C_{BST}

This capacitor provides the gate driver voltage for internal high side MOSEFET. A low ESR more than 100nF ceramic capacitor connected between BST pin and LX pin is recommended.

Dimming Performance

The DIM pin is used to regulate output current by the PWM signal, which supports the frequency from 20KHz to 500KHz. The logic high voltage is 1.5V and the logic low voltage is 0.4V. Only the PWM duty of DIM that is more than 5% can turn on LED, the PWM duty of DIM that is lower than 3% will turn off the LED. The DIM duty from 5% to 100%, the output current will be 5%-100%, the ideal dimming curve shows as figure 2.

Layout

For the best efficiency and minimum noise problems,

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

2) C_{IN} must be close to the pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.

3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

4) The FB pin must not be adjacent to the LX line on the PCB layout to avoid the noise problem.

The recommended layout of SY8718A1 shows as figure 4

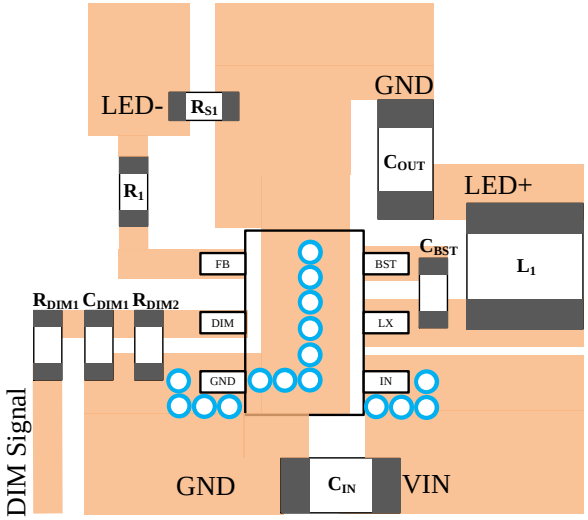
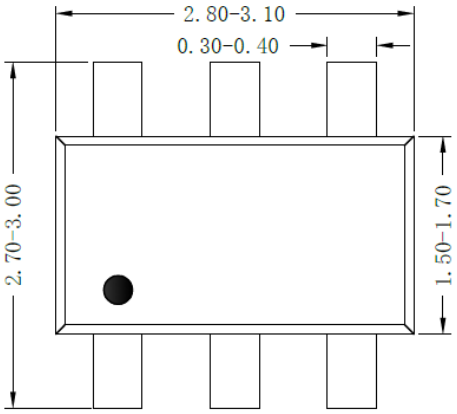
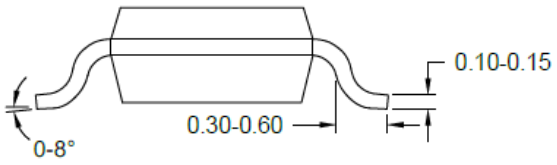


Figure.4 Recommended PCB Layout

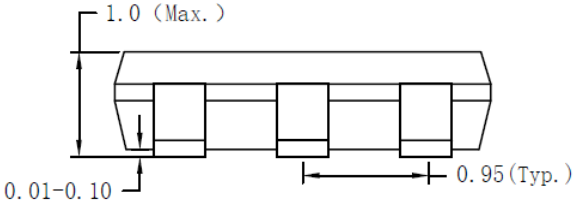
TSOT23-6 Package outline & PCB layout



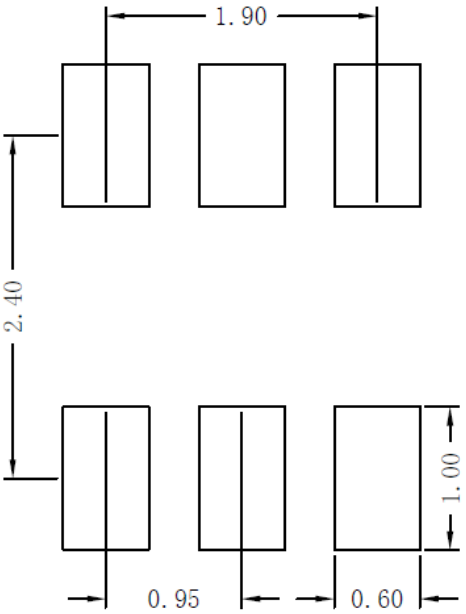
Top view



Side view



Front view



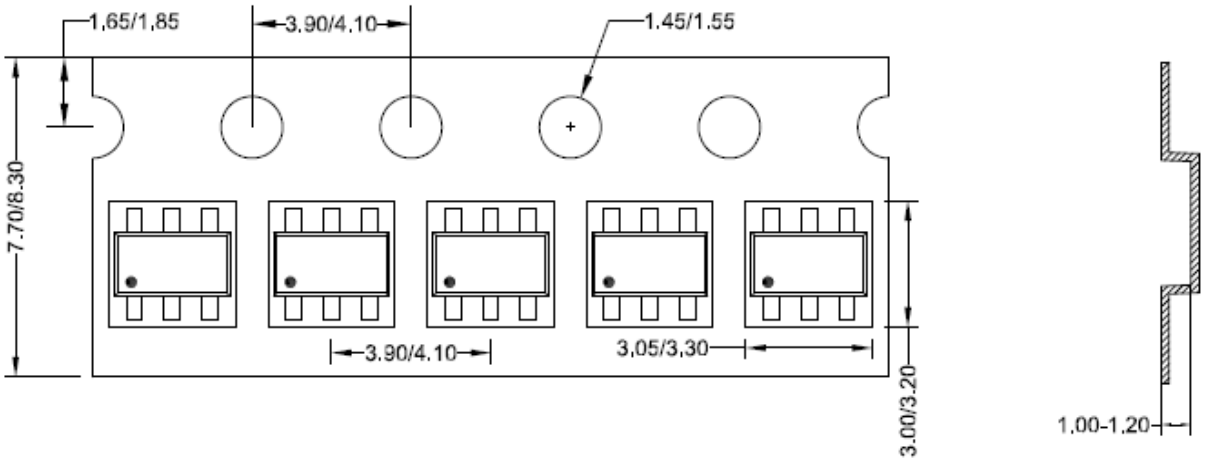
Recommended Pad Layout

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Taping & Reel Specification

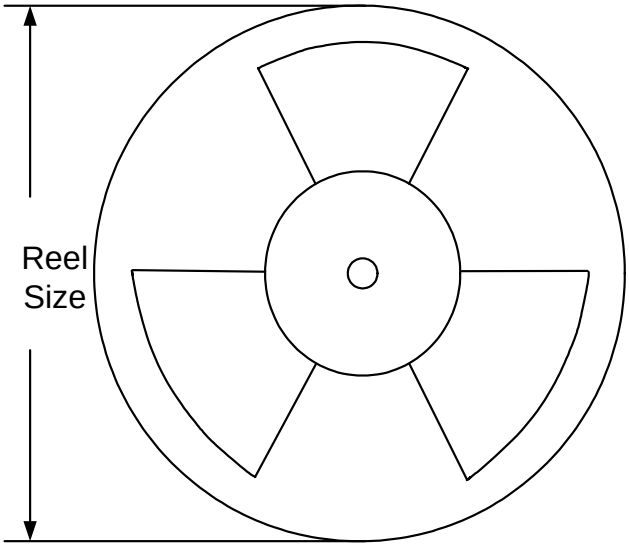
1. Taping orientation

TSOT23-6



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
TSOT23-6	8	4	7	400	160	3000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
September 5, 2018	Revision 0.9	Initial Release

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