4-Bit Programmable Synchronous Buck Controllers

ADP3159/ADP3179

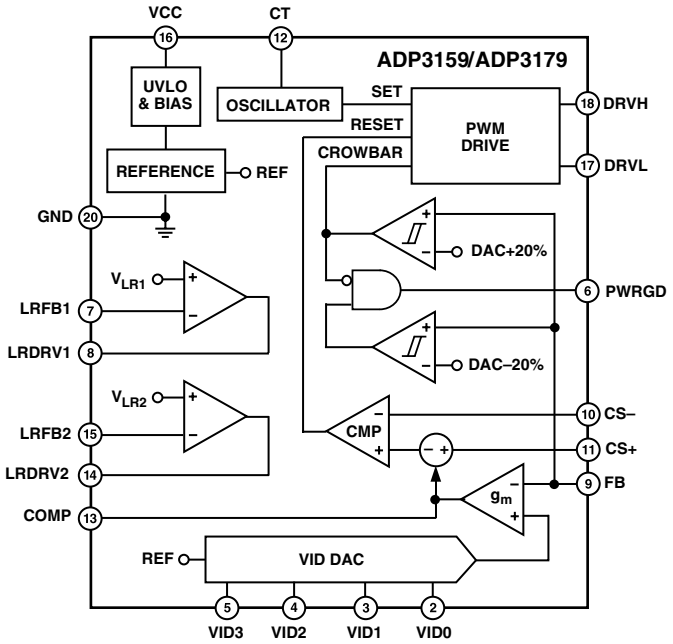
FEATURES

- Optimally Compensated Active Voltage Positioning with Gain and Offset Adjustment (ADOPT™) for Superior Load Transient Response
- Complies with VRM 8.4 Specifications with Lowest System Cost
- 4-Bit Digitally Programmable 1.3 V to 2.05 V Output
- N-Channel Synchronous Buck Driver
- Two On-Board Linear Regulator Controllers
- Total Accuracy ±0.8% Over Temperature
- High Efficiency Current-Mode Operation
- Short Circuit Protection
- Power Good Output
- Overvoltage Protection Crowbar Protects Microprocessors with No Additional External Components

APPLICATIONS

- Core Supply Voltage Generation for:
  - Intel Pentium® III
  - Intel Celeron™

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADP3159 and ADP3179 are highly efficient output synchronous buck switching regulator controllers optimized for converting a 5 V main supply into the core supply voltage required by high-performance processors. These devices use an internal 4-bit DAC to read a voltage identification (VID) code directly from the processor, which is used to set the output voltage between 1.3 V and 2.05 V. They use a current mode, constant off-time architecture to drive two N-channel MOSFETs at a programmable switching frequency that can be optimized for regulator size and efficiency.

The ADP3159 and ADP3179 also use a unique supplemental regulation technique called Analog Devices Optimal Positioning Technology (ADOPT) to enhance load transient performance. Active voltage positioning results in a dc/dc converter that meets the stringent output voltage specifications for high-performance processors, with the minimum number of output capacitors and smallest footprint. Unlike voltage-mode and standard current-mode architectures, active voltage positioning adjusts the output voltage as a function of the load current so it is always optimally positioned for a system transient. The devices also provide accurate and reliable short circuit protection and adjustable current limiting. They also include an integrated overvoltage crowbar function to protect the microprocessor from destruction in case the core supply exceeds the nominal programmed voltage by more than 20%.

The ADP3159 and ADP3179 contain two fixed-output voltage linear regulator controllers that are designed to drive external N-channel MOSFETs. The outputs are internally fixed at 2.5 V and 1.8 V in the ADP3159, while the ADP3179 provides adjustable output, which is set using an external resistor divider. These linear regulators are used to generate the auxiliary voltages (AGP, GTL, etc.) required in most motherboard designs, and have been designed to provide a high bandwidth load-transient response.

The ADP3159 and ADP3179 are specified over the commercial temperature range of 0°C to 70°C and are available in a 20-lead TSSOP package.

REV. A

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ADP3159/ADP3179–SPECIFICATIONS[1] (VCC = 12 V, T_A = 0°C to 70°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
FEEDBACK INPUT						
Output Accuracy	V_{FB}					
1.3 V Output		Figure 1	1.289	1.3	1.311	V
1.65 V Output		Figure 1	1.637	1.65	1.663	V
2.05 V Output		Figure 1	2.034	2.05	2.066	V
Line Regulation	ΔV_{OUT}	VCC = 10 V to 14 V		0.06		%
Crowbar Trip Point	$V_{CROWBAR}$	% of Nominal DAC Voltage	115	120	125	%
Crowbar Reset Point		% of Nominal DAC Voltage	40	50	60	%
Crowbar Response Time	$t_{CROWBAR}$	Overvoltage to DRVL Going High		400		ns
VID INPUTS						
Input Low Voltage	$V_{IL(VID)}$				0.6	V
Input High Voltage	$V_{IH(VID)}$		2.0			V
Input Current	I_{VID}	VID(X) = 0 V		185	250	µA
Pull-Up Resistance	R_{VID}		20	30		kΩ
Internal Pull-Up Voltage			5.0	5.4	5.7	V
OSCILLATOR						
Off Time		T_A = 25°C, CT = 200 pF	3.5	4.0	4.5	µs
CT Charge Current	I_{CT}	T_A = 25°C, V_{OUT} in Regulation	130	150	170	µA
		T_A = 25°C, V_{OUT} = 0 V	25	35	45	µA
ERROR AMPLIFIER						
Output Resistance	$R_{O(ERR)}$			1		mΩ
Transconductance	$g_{m(ERR)}$		2.05	2.2	2.35	mmho
Output Current	$I_{O(ERR)}$	FB– Forced to V_{OUT} – 3%		625		µA
Maximum Output Voltage	$V_{COMP(MAX)}$	FB– Forced to V_{OUT} – 3%		3.0		V
Output Disable Threshold	$V_{COMP(OFF)}$		600	750	900	mV
–3 dB Bandwidth	BW_{ERR}	COMP = Open		500		kHz
CURRENT SENSE						
Threshold Voltage	$V_{CS(TH)}$	FB– Forced to V_{OUT} – 3%	69	78	87	mV
		FB– ≤ 0.45 V	35	45	54	mV
		0.8 V ≤ COMP ≤ 1 V		1	5	mV
Input Bias Current	I_{CS+}, I_{CS-}	CS+ = CS– = V_{OUT}		0.5	5	µA
Response Time	t_{CS}	CS+ – (CS–) > 87 mV to DRVH Going Low		50		ns
OUTPUT DRIVERS						
Output Resistance	$R_{O(DRV(X))}$	I_L = 50 mA		6		Ω
Output Transition Time	t_R, t_F	C_L = 3000 pF		80		ns
LINEAR REGULATORS						
Feedback Current	$I_{LRFB(X)}$			0.3	1	µA
LR1 Feedback Voltage	$V_{LRFB(1)}$	ADP3159 Figure 2, VCC = 4.5 V to 12.6 V	2.44	2.5	2.56	V
		ADP3179 Figure 2, VCC = 2-4.5 V to 12.6 V	0.97	1.0	1.03	V
LR2 Feedback Voltage	$V_{LRFB(2)}$	ADP3159 Figure 2, VCC = 4.5 V to 12.6 V	1.75	1.8	1.85	V
		ADP3179 Figure 2, VCC = 2-4.5 V to 12.6 V	0.97	1.0	1.03	V
Driver Output Voltage	$V_{LRDRV(X)}$	VCC = 4.5 V, $V_{LRFB(X)}$ = 0 V	4.2			V
POWER GOOD COMPARATOR						
Undervoltage Threshold	$V_{PWRGD(UV)}$	% of Nominal DAC Voltage	75	80	85	%
Undervoltage Hysteresis		% of Nominal DAC Voltage		5		%
Overvoltage Threshold	$V_{PWRGD(OV)}$	% of Nominal DAC Voltage	115	120	125	%
Overvoltage Reset Point		% of Nominal DAC Voltage	40	50	60	%
Output Voltage Low	$V_{OL(PWRGD)}$	$I_{PWRGD(SINK)}$ = 1 mA		250	500	mV
Response Time				250		ns
SUPPLY						
DC Supply Current[2]	I_{CC}			7	9	mA
UVLO Threshold Voltage	V_{UVLO}		6.75	7	7.25	V
UVLO Hysteresis			0.8	1	1.2	V

NOTES

[1]All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC).

[2]Dynamic supply current is higher due to the gate charge being delivered to the external MOSFETs.

Specifications subject to change without notice.

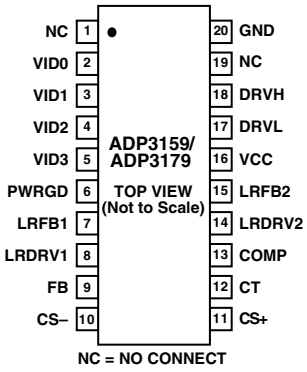
ABSOLUTE MAXIMUM RATINGS*

VCC . . . . . –0.3 V to +15 V
DRVH, DRVL, LRDRV1, LRDRV2 . . . . –0.3 V to VCC + 0.3 V
All Other Inputs and Outputs . . . . . –0.3 V to +10 V
Operating Ambient Temperature Range . . . . . 0°C to 70°C
Operating Junction Temperature . . . . . 125°C
Storage Temperature Range . . . . . –65°C to +150°C
θ_{JA} . . . . . 143°C/W
Lead Temperature (Soldering, 10 sec) . . . . . 300°C
Vapor Phase (60 sec) . . . . . 215°C
Infrared (15 sec) . . . . . 220°C

*This is a stress rating only; operation beyond these limits can cause the device to be permanently damaged. Unless otherwise specified, all voltages are referenced to GND.

PIN CONFIGURATION

RU-20



PIN FUNCTION DESCRIPTIONS

Pin	Mnemonic	Function
1, 19	NC	No Connection.
2–5	VID3, VID2, VID1, VID0	Voltage Identification DAC Inputs. These pins are pulled up to an internal reference, providing a Logic One if left open. The DAC output programs the FB regulation voltage from 1.3 V to 2.05 V.
6	PWRGD	Open drain output that signals when the output voltage is in the proper operating range.
7, 15	LRFB1, LRFB2	Feedback connections for the linear regulator controllers.
8, 14	LRDRV1, LRDRV2	Gate drives for the respective linear regulator N-channel MOSFETs.
9	FB	Feedback Input. Error amplifier input for remote sensing of the output voltage.
10	CS–	Current Sense Negative Node. Negative input for the current comparator.
11	CS+	Current Sense Positive Node. Positive input for the current comparator. The output current is sensed as a voltage at this pin with respect to CS–.
12	CT	External capacitor connected from CT to ground sets the Off-time of the device.
13	COMP	Error Amplifier Output and Compensation Point. The voltage at this output programs the output current control level between CS+ and CS–.
16	VCC	Supply Voltage for the device.
17	DRVL	Low-Side MOSFET Drive. Gate drive for the synchronous rectifier N-channel MOSFET. The voltage at DRVL swings from GND to VCC.
18	DRVH	High-side MOSFET Drive. Gate drive for the buck switch N-channel MOSFET. The voltage at DRVH swings from GND to VCC.
20	GND	Ground Reference. GND should have a low impedance path to the source of hte synchronous MOSFET.

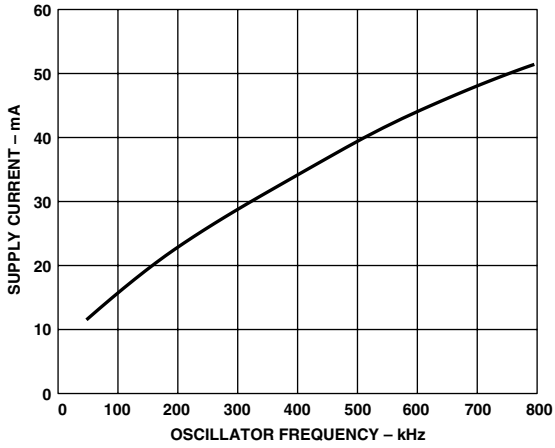
ORDERING GUIDE

Model	Temperature Range	LDO Voltage	Package Description	Package Option
ADP3159JRU	0°C to 70°C	2.5 V, 1.8 V	Thin Shrink Small Outline	RU-20
ADP3179JRU	0°C to 70°C	Adjustable	Thin Shrink Small Outline	RU-20

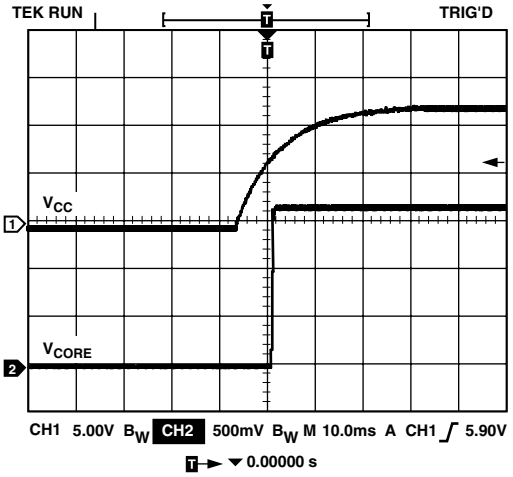
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP3159 and the ADP3179 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

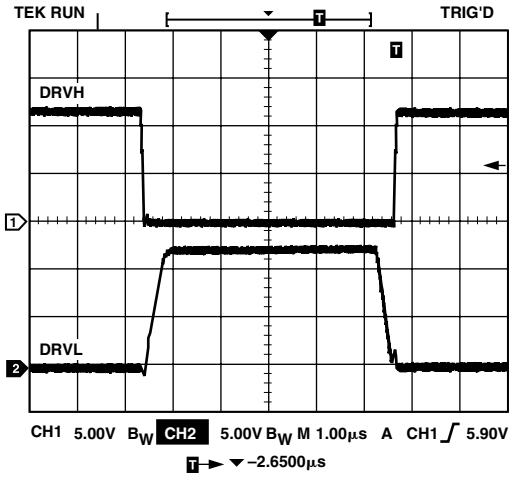
ADP3159/ADP3179 –Typical Performance Characteristics



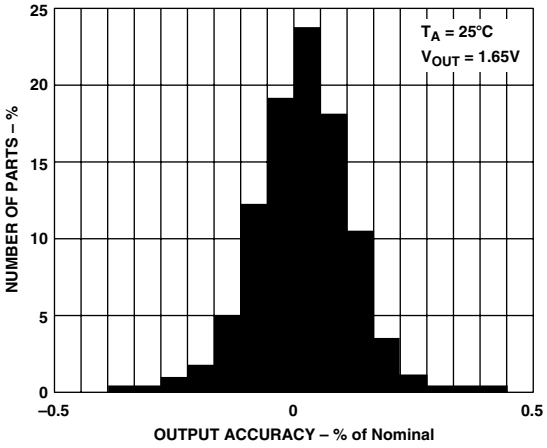
TPC 1. Supply Current vs. Operating Frequency Using MOSFETs of Figure 3



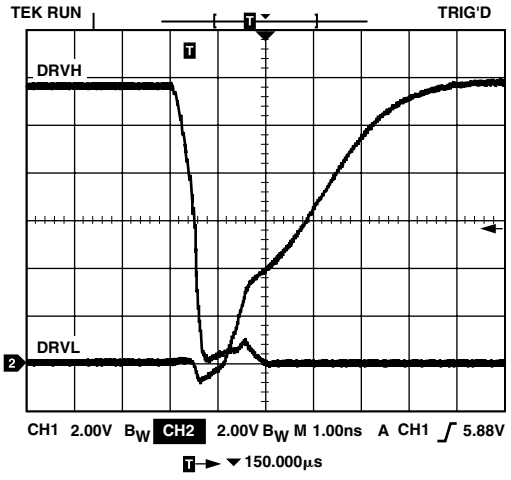
TPC 4. Power-On Start-Up Waveform



TPC 2. Gate Switching Waveforms Using MOSFETs of Figure 3



TPC 5. Output Accuracy Distribution



TPC 3. Driver Transition Waveforms Using MOSFETs of Figure 3

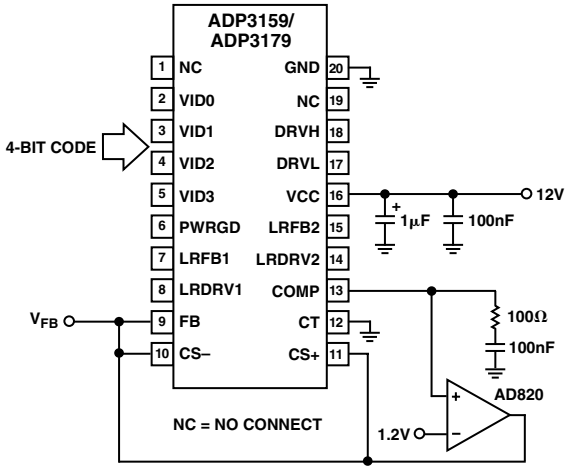


Figure 1. Closed Loop Output Voltage Accuracy Test Circuit

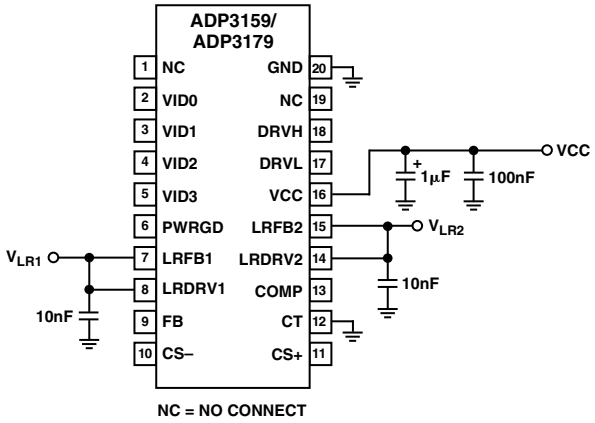


Figure 2. Linear Regulator Output Voltage Accuracy Test Circuit

THEORY OF OPERATION

The ADP3159 and ADP3179 use a current-mode, constant off-time control technique to switch a pair of external N-channel MOSFETs in a synchronous buck topology. Constant off-time operation offers several performance advantages, including that no slope compensation is required for stable operation. A unique feature of the constant off-time control technique is that since the off-time is fixed, the converter's switching frequency is a function of the ratio of input voltage to output voltage. The fixed off-time is programmed by the value of an external capacitor connected to the CT pin. The on-time varies in such a way that a regulated output voltage is maintained as described below in the cycle-by-cycle operation. The on-time does not vary under fixed input supply conditions, and it varies only slightly as a function of load. This means that the switching frequency remains fairly constant in a standard computer application.

Active Voltage Positioning

The output voltage is sensed at the CS– pin. A voltage error amplifier, (g_m), amplifies the difference between the output voltage and a programmable reference voltage. The reference voltage is programmed to between 1.3 V and 2.05 V by an internal 4-bit DAC that reads the code at the voltage identification (VID) pins (Refer to Table I for output voltage vs. VID pin code information). A unique supplemental regulation technique called Analog Devices Optimal Positioning Technology (ADOPT) adjusts the output voltage as a function of the load current so that it is always optimally positioned for a load transient. Standard (passive) voltage positioning, sometimes recommended for use with other architectures, has poor dynamic performance which renders it ineffective under the stringent repetitive transient conditions specified in Intel VRM documents. Consequently, such techniques do not allow the minimum possible number of output capacitors to be used. ADOPT, as used in the ADP3159 and ADP3179, provides a bandwidth for transient response that is limited only by parasitic output inductance. This yields optimal load transient response with the minimum number of output capacitors.

Cycle-by-Cycle Operation

During normal operation (when the output voltage is regulated), the voltage error amplifier and the current comparator are the main control elements. During the on-time of the high-side MOSFET, the current comparator monitors the voltage between the CS+ and CS– pins. When the voltage level between the two pins reaches the threshold level, the DRVH output is switched to ground, which turns off the high-side MOSFET. The timing capacitor CT is then charged at a rate determined by the off-time controller. While the timing capacitor is charging, the DRVL output goes high, turning on the low-side MOSFET. When the voltage level on the timing capacitor has charged to the upper threshold voltage level, a comparator resets a latch. The output of the latch forces the low-side drive output to go low and the high-side drive output to go high. As a result, the low-side switch is turned off and the high-side switch is turned on. The sequence is then repeated. As the load current increases, the output voltage starts to decrease. This causes an increase in the output of the voltage-error amplifier, which, in turn, leads to an increase in the current comparator threshold, thus tracking the load current. To prevent cross conduction of the external MOSFETs, feedback is incorporated to sense the state of the driver output pins. Before the low-side drive output can go high, the high-side drive output must be low. Likewise, the high-side drive output is unable to go high while the low-side drive output is high.

Power Good

The ADP3159 has an internal monitor that senses the output voltage and drives the PWRGD pin of the device. This pin is an open drain output whose high level (when connected to a pull-up resistor) indicates that the output voltage has been within a ±20% regulation band of the targeted value for more than 500 ms. The PWRGD pin will go low if the output is outside the regulation band for more than 500 ms.

Output Crowbar

An added feature of using an N-channel MOSFET as the synchronous switch is the ability to crowbar the output with the same MOSFET. If the output voltage is 20% greater than the targeted value, the controller IC will turn on the lower MOSFET, which will current-limit the source power supply or blow its fuse, pull down the output voltage, and thus save the microprocessor from destruction. The crowbar function releases at approximately 50% of the nominal output voltage. For example, if the output is programmed to 1.5 V, but is pulled up to 1.85 V or above, the crowbar will turn on the lower MOSFET. If in this case the output is pulled down to less than 0.75 V, the crowbar will release, allowing the output voltage to recover to 1.5 V if the fault condition has been removed.

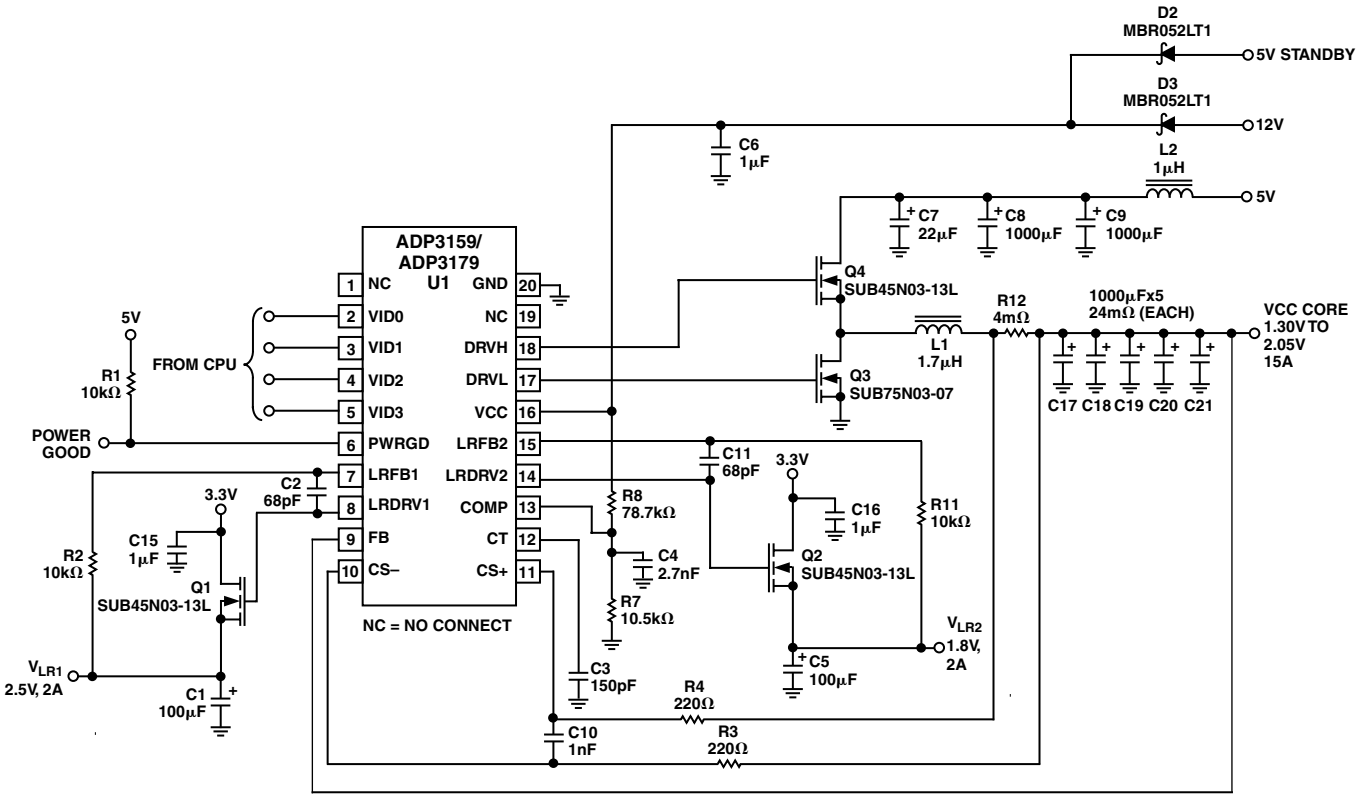


Figure 3. 15 A Pentium III Application Circuit

On-board Linear Regulator Controllers

The ADP3159 and ADP3179 include two linear regulator controllers to provide a low cost solution for generating additional supply rails. In the ADP3159, these regulators are internally set to 2.5 V (LR1) and 1.8 V (LR2) with ±2.5% accuracy. The ADP3179 is designed to allow the outputs to be set externally using a resistor divider. The output voltage is sensed by the high input impedance LRFB(x) pin and compared to an internal fixed reference.

The LRDRV(x) pin controls the gate of an external N-channel MOSFET resulting in a negative feedback loop. The only additional components required are a capacitor and resistor for stability. Higher output voltages can be generated by placing a resistor divider between the linear regulator output and its respective LRFB pin. The maximum output load current is determined by the size and thermal impedance of the external power MOSFET that is placed in series with the supply and controlled by the ADP3159.

The linear regulator controllers have been designed so that they remain active even when the switching controller is in UVLO mode to ensure that the output voltages of the linear regulators will track the 3.3 V supply as required by Intel design specifications. By diode ORing the VCC input of the IC to the 5 VSB and 12 V supplies as shown in Figure 3, the switching output will be disabled in standby mode, but the linear regulators will begin conducting once VCC rises above about 1 V. During start-up the linear outputs will track the 3.3 V supply up until they reach their respective regulation points, regardless of the state of the 12 V supply. Once the 12 V supply has exceeded the 5 VSB supply by more than a diode drop, the controller IC will track the 12 V supply. Once the 12 V supply has risen above the UVLO value, the switching regulator will begin its start-up sequence.

Table I. Output Voltage vs. VID Code

VID3	VID2	VID1	VID0	$V_{OUT(NOM)}$
1	1	1	1	1.30 V
1	1	1	0	1.35 V
1	1	0	1	1.40 V
1	1	0	0	1.45 V
1	0	1	1	1.50 V
1	0	1	0	1.55 V
1	0	0	1	1.60 V
1	0	0	0	1.65 V
0	1	1	1	1.70 V
0	1	1	0	1.75 V
0	1	0	1	1.80 V
0	1	0	0	1.85 V
0	0	1	1	1.90 V
0	0	1	0	1.95 V
0	0	0	1	2.00 V
0	0	0	0	2.05 V

APPLICATION INFORMATION

Specifications for a Design Example

The design parameters for a typical 750 MHz Pentium III application (shown in Figure 3) are as follows:

Input Voltage: (V_{IN}) = 5 V

Auxiliary Input: (V_{CC}) = 12 V

Output Voltage (V_{VID}) = 1.7 V

Maximum Output Current ($I_{O(MAX)}$) = 15 A

Minimum Output Current ($I_{O(MIN)}$) = 1 A

Static tolerance of the supply voltage for the processor core (ΔV_O) = +40 mV (–80 mV) = 120 mV

Transient tolerance (for less than 2 µs) of the supply voltage for the processor core when the load changes between the minimum and maximum values with a di/dt of 20 A/µs ($\Delta V_{O(TRANSIENT)}$) = +80 mV (–130 mV) = 210 mV

Input current di/dt when the load changes between the minimum and maximum values < 0.1 A/µs.

The above requirements correspond to Intel's published power supply requirements based on VRM 8.4 guidelines.

CT Selection for Operating Frequency

The ADP3159 uses a constant off-time architecture with t_{OFF} determined by an external timing capacitor CT. Each time the high-side N-channel MOSFET switch turns on, the voltage across CT is reset to 0 V. During the off-time, CT is discharged by a constant current of 150 µA. Once CT reaches 3.0 V, a new on-time cycle is initiated. The value of the off-time is calculated using the continuous-mode operating frequency. Assuming a nominal operating frequency (f_{NOM}) of 200 kHz at an output voltage of 1.7 V, the corresponding off-time is:

$$t_{OFF} = \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \frac{1}{f_{NOM}}$$
$$t_{OFF} = \left(1 - \frac{1.7\,V}{5\,V}\right) \times \frac{1}{200\,kHz} = 3.3\,\mu s \quad (1)$$

The timing capacitor can be calculated from the equation:

$$C_T = \frac{t_{OFF} \times I_{CT}}{V_{T(TH)}} = \frac{3.3\,\mu s \times 150\,\mu A}{3\,V} \approx 150\,pF \quad (2)$$

The converter only operates at the nominal operating frequency at the above-specified V_{OUT} and at light load. At higher values of V_{OUT}, or under heavy load, the operating frequency decreases due to the parasitic voltage drops across the power devices. The actual minimum frequency at V_{OUT} = 1.7 V is calculated to be 195 kHz (see Equation 3), where:

$R_{DS(ON)HSF}$ is the resistance of the high-side MOSFET (estimated value: 14 mΩ)

$R_{DS(ON)LSF}$ is the resistance of the low-side MOSFET (estimated value: 6 mΩ)

R_{SENSE} is the resistance of the sense resistor (estimated value: 4 mΩ)

R_L is the resistance of the inductor (estimated value: 3 mΩ)

$$f_{MIN} = \frac{1}{t_{OFF}} \times \frac{V_{IN} - I_{O(MAX)} \times (R_{DS(ON)HSF} + R_{SENSE} + R_L) - V_{OUT}}{V_{IN} - I_{O(MAX)} \times (R_{DS(ON)HSF} + R_{SENSE} + R_L - R_{DS(ON)LSF})} \quad (3)$$

Inductance Selection

The choice of inductance determines the ripple current in the inductor. Less inductance leads to more ripple current, which increases the output ripple voltage and the conduction losses in the MOSFETs, but allows using smaller-size inductors and, for a specified peak-to-peak transient deviation, output capacitors with less total capacitance. Conversely, a higher inductance means lower ripple current and reduced conduction losses, but requires larger-size inductors and more output capacitance for the same peak-to-peak transient deviation. The following equation shows the relationship between the inductance, oscillator frequency, peak-to-peak ripple current in an inductor and input and output voltages.

$$L = \frac{V_{OUT} \times t_{OFF}}{I_{L(RIPPLE)}} \quad (4)$$

For 4 A peak-to-peak ripple current, which corresponds to approximately 25% of the 15 A full-load dc current in an inductor, Equation 4 yields an inductance of:

$$L = \frac{1.7\,V \times 3.3\,\mu s}{4\,A} = 1.4\,\mu H$$

A 1.5 µH inductor can be used, which gives a calculated ripple current of 3.8 A at no load. The inductor should not saturate at the peak current of 17 A and should be able to handle the sum of the power dissipation caused by the average current of 15 A in the winding and the core loss.

Designing an Inductor

Once the inductance is known, the next step is either to design an inductor or find a standard inductor that comes as close as possible to meeting the overall design goals. The first decision in designing the inductor is to choose the core material. There are several possibilities for providing low core loss at high frequencies. Two examples are the powder cores (e.g., Kool-Mµ® from Magnetics, Inc.) and the gapped soft ferrite cores (e.g., 3F3 or 3F4 from Philips). Low frequency powdered iron cores should be avoided due to their high core loss, especially when the inductor value is relatively low and the ripple current is high.

Two main core types can be used in this application. Open magnetic loop types, such as beads, beads on leads, and rods and slugs, provide lower cost but do not have a focused magnetic field in the core. The radiated EMI from the distributed magnetic field may create problems with noise interference in the circuitry surrounding the inductor. Closed-loop types, such as pot cores, PQ, U, and E cores, or toroids, cost more, but have much better EMI/RFI performance. A good compromise between price and performance are cores with a toroidal shape.

There are many useful references for quickly designing a power inductor. Table II gives some examples.

Table II. Magnetics Design References

Magnetic Designer Software Intusoft (http://www.intusoft.com)
Designing Magnetic Components for High-Frequency DC-DC Converters McLyman, Kg Magnetics ISBN 1-883107-00-08

Selecting a Standard Inductor

The companies listed in Table III can provide design consultation and deliver power inductors optimized for high power applications upon request.

Table III. Power Inductor Manufacturers

Coilcraft (847) 639-6400 http://www.coilcraft.com
Coiltronics (561) 752-5000 http://www.coiltronics.com
Sumida Electric Company (408) 982-9660 http://www.sumida.com

C_{OUT} Selection—Determining the ESR

The required equivalent series resistance (ESR) and capacitance drive the selection of the type and quantity of the output capacitors. The ESR must be small enough to contain the voltage deviation caused by a maximum allowable CPU transient current within the specified voltage limits, giving consideration also to the output ripple and the regulation tolerance. The capacitance must be large enough that the voltage across the capacitor, which is the sum of the resistive and capacitive voltage deviations, does not deviate beyond the initial resistive deviation while the inductor current ramps up or down to the value corresponding to the new load current. The maximum allowed ESR also represents the maximum allowed output resistance, R_{OUT}.

The cumulative errors in the output voltage regulation cuts into the available regulation window, V_{WIN}. When considering dynamic load regulation this relates directly to the ESR. When considering dc load regulation, this relates directly to the programmed output resistance of the power converter.

Some error sources, such as initial voltage accuracy and ripple voltage, can be directly deducted from the available regulation window, while other error sources scale proportionally to the amount of voltage positioning used, which, for an optimal design, should utilize the maximum that the regulation window will allow. The error determination is a closed-loop calculation, but it can be closely approximated. To maintain a conservative design while avoiding an impractical design, various error sources should be considered and summed statistically.

The output ripple voltage can be factored into the calculation by summing the output ripple current with the maximum output current to determine an effective maximum dynamic current change. The remaining errors are summed separately according to the formula:

$$V_{WIN} = (V_{\Delta} - V_{VID} \times 2\,k_{VID}) \times \left(1 - \frac{I_O}{I_O + I_{O\Delta}} \sqrt{k_{RCS}{}^2 + \left(\frac{k_{CSF}}{2}\right)^2 + k_{RT}{}^2 + k_{EA}{}^2}\right) = 95\,mV \quad (5)$$

where k_{VID} = 0.5% is the initial programmed voltage tolerance from the graph of TPC 6, k_{RCS} = 2% is the tolerance of the current sense resistor, k_{CSF} = 10% is the summed tolerance of the current sense filter components, k_{RT} = 2% is the tolerance of the two termination resistors added at the COMP pin, and k_{EA} = 8% accounts for the IC current loop gain tolerance including the g_m tolerance.

The remaining window is then divided by the maximum output current plus the ripple to determine the maximum allowed ESR and output resistance:

$$R_{E(MAX)} = R_{OUT(MAX)} = \frac{V_{WIN}}{I_O + I_{O\Delta}} = \frac{95\,mV}{15\,A + 3.8\,A} = 5\,m\Omega \quad (6)$$

The output filter capacitor bank must have an ESR of less than 5 mΩ. One can, for example, use five ZA series capacitors from Rubycon which would give an ESR of 4.8 mΩ. Without ADOPT voltage positioning, the ESR would need to be less than 3 mΩ, yielding a 50% increase to eight Rubycon output capacitors.

C_{OUT}—Checking the Capacitance

As long as the capacitance of the output capacitor is above a critical value and the regulating loop is compensated with ADOPT, the actual value has no influence on the peak-to-peak deviation of the output voltage to a full step change in the load current. The critical capacitance can be calculated as follows:

$$C_{OUT(CRIT)} = \frac{I_O}{R_E \times V_{OUT}} \times L = \frac{15\,A}{5\,m\Omega \times 1.7} \times 1.5\,\mu H = 2.6\,mF \quad (7)$$

The critical capacitance for the five ZA series Rubycon capacitors is 2.6 mF while the equivalent capacitance is 5 mF. The capacitance is safely above the critical value.

R_{SENSE}

The value of R_{SENSE} is based on the maximum required output current. The current comparator of the ADP3159 has a minimum current limit threshold of 69 mV. Note that the 69 mV value cannot be used for the maximum specified nominal current, as headroom is needed for ripple current and tolerances.

The current comparator threshold sets the peak of the inductor current yielding a maximum output current, I_O, which equals twice the peak inductor current value less half of the peak-to-peak inductor ripple current. From this the maximum value of R_{SENSE} is calculated as:

$$R_{SENSE} \le \frac{V_{CS(CL)(MIN)}}{I_O + \frac{I_{L(RIPPLE)}}{2}} = \frac{69\ mV}{15\ A + 1.9\ A} = 4\ m\Omega \quad (8)$$

In this case, 4 mΩ was chosen as the closest standard value.

Once R_{SENSE} has been chosen, the output current at the point where current limit is reached, $I_{OUT(CL)}$, can be calculated using the maximum current sense threshold of 87 mV:

$$I_{OUT(CL)} = \frac{V_{CS(CL)(MAX)}}{R_{SENSE}} - \frac{I_{L(RIPPLE)}}{2} = \frac{87\ mV}{4\ m\Omega} - \frac{3.8\ A}{2} \approx 20\ A \quad (9)$$

At output voltages below 450 mV, the current sense threshold is reduced to 54 mV, and the ripple current is negligible. Therefore, at dead short the output current is reduced to:

$$I_{OUT(SC)} = \frac{54\ mV}{4\ m\Omega} = 13.5\ A \quad (10)$$

To safely carry the current under maximum load conditions, the sense resistor must have a power rating of at least:

$$P_{R_{SENSE}} = (I_O)^2 \times R_{SENSE} = (20\ A)^2 \times 4\ m\Omega = 1.6\ W \quad (11)$$

Power MOSFETs

Two external N-channel power MOSFETs must be selected for use with the ADP3159, one for the main switch and an identical one for the synchronous switch. The main selection parameters for the power MOSFETs are the threshold voltage ($V_{GS(TH)}$) and the ON-resistance ($R_{DS(ON)}$).

The minimum input voltage dictates whether standard threshold or logic-level threshold MOSFETs must be used. For V_{IN} > 8 V, standard threshold MOSFETs ($V_{GS(TH)}$ < 4 V) may be used. If V_{IN} is expected to drop below 8 V, logic-level threshold MOSFETs ($V_{GS(TH)}$ < 2.5 V) are strongly recommended. Only logic-level MOSFETs with V_{GS} ratings higher than the absolute maximum value of V_{CC} should be used.

The maximum output current $I_{O(MAX)}$ determines the $R_{DS(ON)}$ requirement for the two power MOSFETs. When the ADP3159 is operating in continuous mode, the simplifying assumption can be made that one of the two MOSFETs is always conducting the average load current. For V_{IN} = 5 V and V_{OUT} = 1.65 V, the maximum duty ratio of the high-side FET is:

$$D_{HSF(MAX)} = 1 - (f_{MIN} \times t_{OFF})$$
$$D_{HSF(MAX)} = 1 - (195\ kHz \times 3.3\ \mu s) = 36\% \quad (12)$$

The maximum duty ratio of the low-side (synchronous rectifier) MOSFET is:

$$D_{LSF(MAX)} = 1 - D_{HSF(MAX)} = 54\% \quad (13)$$

The maximum rms current of the high-side MOSFET is:

$$I_{RMSHSF} = \sqrt{D_{HSF(MAX)} \times \frac{I_{L(VALLEY)}^2 + (I_{L(VALLEY)} \times I_{L(PEAK)}) + I_{L(PEAK)}^2}{3}}$$
$$I_{RMSHSF} = \sqrt{36\% \times \frac{13.1\ A^2 + (13.1\ A \times 16.1\ A) + 16.1\ A^2}{3}} = 8.8\ A\ rms \quad (14)$$

The maximum rms current of the low-side MOSFET is:

$$I_{RMSLSF} = \sqrt{D_{LSF(MAX)} \times \frac{I_{L(VALLEY)}^2 + I_{L(VALLEY)} \times I_{L(PEAK)} + I_{L(PEAK)}^2}{3}}$$
$$I_{RMSLSF} = \sqrt{54\% \times \frac{13.1\ A^2 + (13.1\ A \times 16.1\ A) + 16.1\ A^2}{3}} = 10.8\ A\ rms \quad (15)$$

The $R_{DS(ON)}$ for each MOSFET can be derived from the allowable dissipation. If 10% of the maximum output power is allowed for MOSFET dissipation, the total dissipation will be:

$$P_{D(FETs)} = 0.1 \times V_{OUT} \times I_{OUT(MAX)} = 2.26\ W \quad (16)$$

Allocating half of the total dissipation for the high-side MOSFET and half for the low-side MOSFET and assuming that switching losses are small relative to the dc conduction losses, the required minimum MOSFET resistances will be:

$$R_{DS(ON)HSF} \le \frac{P_{HSF}}{I_{HSF}^2} = \frac{1.13\ W}{8.8 A^2} = 15\ m\Omega \quad (17)$$

$$R_{DS(ON)LSF} \le \frac{P_{LSF}}{I_{LSF}^2} = \frac{1.13\ W}{10.8\ A^2} = 10\ m\Omega \quad (18)$$

Note that there is a trade-off between converter efficiency and cost. Larger MOSFETs reduce the conduction losses and allow higher efficiency, but increase the system cost. If efficiency is not a major concern, a Vishay-Siliconix SUB45N03-13L ($R_{DS(ON)}$ = 10 mΩ nominal, 16 mΩ worst-case) for the high-side and a Vishay-Siliconix SUB75N03-07 ($R_{DS(ON)}$ = 6 mΩ nominal, 10 mΩ worst-case) for the low-side are good choices.

The high-side MOSFET dissipation is:

$$P_{DHSF} = I_{RMSHSF}^2 \times R_{DS(ON)} + \frac{V_{IN} \times I_{L(PEAK)} \times Q_G \times f_{MIN}}{2 \times I_G}$$
$$P_{DHSF} = 8.8\ A^2 \times 16\ m\Omega + \frac{5\ V \times 15\ A \times 70\ nC \times 195\ kHz}{2 \times 1\ A} = 1.75\ W \quad (19)$$

where the second term represents the turn-off loss of the MOSFET. In the second term, Q_G is the gate charge to be removed from the gate for turn-off and I_G is the gate current. From the data sheet, Q_G is 70 nC and the gate drive current provided by the ADP3159 is about 1 A.

The low-side MOSFET dissipation is:

$$P_{DLSF} = I_{RMSLSF}^2 \times R_{DS(ON)}$$
$$P_{DLSF} = 10.8\ A^2 \times 10\ m\Omega = 1.08\ W \quad (20)$$

Note that there are no switching losses in the low-side MOSFET.

Surface mount MOSFETs are preferred in CPU core converter applications due to their ability to be handled by automatic assembly equipment. The TO-263 package offers the power handling of a TO-220 in a surface-mount package. However, this package still needs adequate copper area on the PCB to help move the heat away from the package.

The junction temperature for a given area of 2-ounce copper can be approximated using:

$$T_J = \left(\theta_{JA} \times P_D\right) + T_A \quad (21)$$

assuming:

θ_{JA} = 45°C/W for 0.5 in^2
θ_{JA} = 36°C/W for 1 in^2
θ_{JA} = 28°C/W for 2 in^2

For 1 in^2 of copper area attached to each transistor and an ambient temperature of 50°C:

$$T_{JHSF} = (36°C/W \times 1.48\ W) + 50°C = 103°C$$
$$T_{JLSF} = (36°C/W \times 1.08\ W) + 50°C = 89°C$$

All of the above-calculated junction temperatures are safely below the 175°C maximum specified junction temperature of the selected MOSFETs.

C_{IN} Selection and Input Current di/dt Reduction

In continuous inductor-current mode, the source current of the high-side MOSFET is approximately a square wave with a duty ratio equal to V_{OUT}/V_{IN} and an amplitude of one-half of the maximum output current. To prevent large voltage transients, a low ESR input capacitor sized for the maximum rms current must be used. The maximum rms capacitor current is given by:

$$I_{C(RMS)} = I_O \sqrt{D_{HSF} - D_{HSF}^2} =$$
$$15\,A \sqrt{0.36 - 0.36^2} = 7.2\,A \quad (22)$$

For a ZA-type capacitor with 1000 µF capacitance and 6.3 V voltage rating, the ESR is 24 mΩ and the maximum allowable ripple current at 100 kHz is 2 A. At 105°C, at least four such capacitors must be connected in parallel to handle the calculated ripple current. At 50°C ambient, however, a higher ripple current can be tolerated, so three capacitors in parallel are adequate.

The ripple voltage across the three paralleled capacitors is:

$$V_{C(IN)RIPPLE} = I_O \times \left(\frac{ESR_{C(IN)}}{n_C} + \frac{D_{HSF}}{n_C \times C_{IN} \times f_{MAX}}\right)$$
$$V_{C(IN)RIPPLE} = 15\,A \times \left(\frac{24\,m\Omega}{3} + \frac{36\%}{3 \times 1000\,\mu F \times 195\,kHz}\right) = 129\,mV \quad (23)$$

To further reduce the effect of the ripple voltage on the system supply voltage bus, and to reduce the input-current di/dt to below the recommended maximum of 0.1 A/ms, an additional small inductor (L > 1 µH @ 10 A) should be inserted between the converter and the supply bus.

Feedback Compensation for Active Voltage Positioning

Optimized compensation of the ADP3159 allows the best possible containment of the peak-to-peak output voltage deviation. Any practical switching power converter is inherently limited by the inductor in its output current slew rate to a value much less than the slew rate of the load. Therefore, any sudden change of load current will initially flow through the output capacitors, and this will produce an output voltage deviation equal to the ESR of the output capacitor array times the load current change.

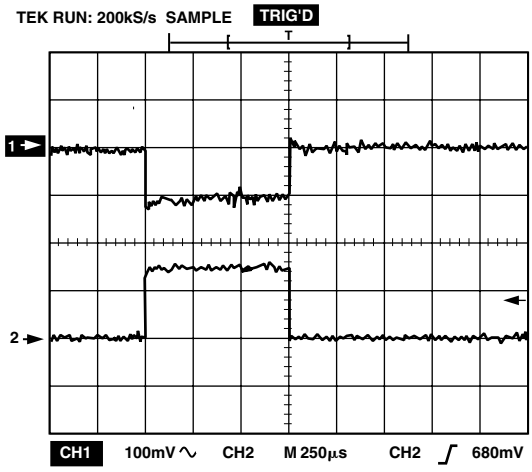


Figure 4. Transient Response of the Circuit of Figure 3

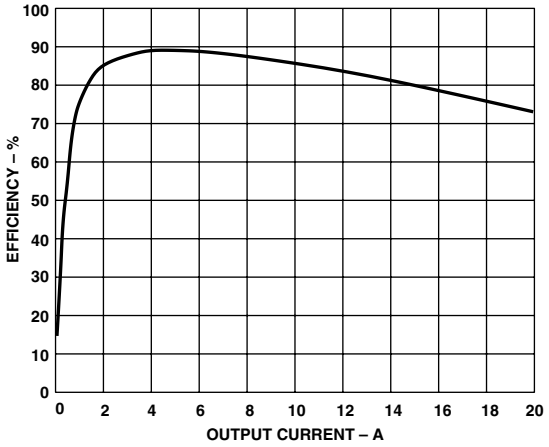


Figure 5. Efficiency vs. Load Current of the Circuit of Figure 3

To correctly implement active voltage positioning, the low frequency output impedance (i.e., the output resistance) of the converter should be made equal to the maximum ESR of the output capacitor array. This can be achieved by having a single-pole roll-off of the voltage gain of the g_m error amplifier, where the pole frequency coincides with the ESR zero of the output capacitor. A gain with single-pole roll-off requires that the g_m amplifier output pin be terminated by the parallel combination of a resistor and capacitor. The required resistor value can be calculated from the equation:

$$R_{COMP} = \frac{R_{OGM} \times R_{TOTAL}}{R_{OGM} - R_{TOTAL}} = \frac{1\,M\Omega \times 9.1\,k\Omega}{1\,M\Omega - 9.1\,k\Omega} = 9.2\,k\Omega \quad (24)$$

where:

$$R_{TOTAL} = \frac{n_I \times R_{SENSE}}{g_m \times R_{E(MAX)}} = \frac{25 \times 4\,m\Omega}{2.2\,mmho \times 5\,m\Omega} = 9.1\,k\Omega \quad (25)$$

In Equations 24 and 25, R_{OGM} is the internal resistance of the g_m amplifier, n_I is the division ratio from the output voltage to signal of the g_m amplifier to the PWM comparator, and g_m is the transconductance of the g_m amplifier itself.

Although a single termination resistor equal to R_{COMP} would yield the proper voltage positioning gain, the dc biasing of that resistor would determine how the regulation band is centered (i.e., offset). Note that sometimes the specified regulation band is asymmetrical with respect to the nominal VID voltage. With the ADP3159, the offset is already considered part of the design procedure—no special provision is required. To accomplish the dc biasing, it is simplest to use two resistors to terminate the g_m amplifier output, with the lower resistor (R_B) tied to ground and the upper resistor (R_A) to the 12 V supply of the IC. The values of these resistors can be calculated using:

$$R_A = \frac{V_{DIV}}{g_m \times (V_{OUT(OS)} + K)} = \frac{12\,V}{2.2\,mmho \times (22\,mV + 4.7 \times 10^{-2})} = 79.1\,k\Omega \quad (26)$$

where K is a constant determined by internal characteristics of the ADP3159, peak-to-peak inductor current ripple (I_{RIPPLE}), and the current sampling resistor (R_{SENSE}). K can be calculated using Equations 28 and 29. V_{DIV} is the resistor divider supply voltage (e.g., the recommended 12 V supply) and $V_{OUT(OS)}$ is the output voltage offset from the nominal VID-programmed value under no load condition. This offset is given by Equation 30.

The closest 1% value for R_A is 78.7 kΩ. This value is then used to solve for R_B:

$$R_B = \frac{R_A \times R_{COMP}}{R_A - R_{COMP}} = \frac{78.7\,k\Omega \times 9.2\,k\Omega}{78.7\,k\Omega - 9.2\,k\Omega} = 10.4\,k\Omega \quad (27)$$

The nearest 1% value of 10.5 kΩ was chosen for R_B.

$$K = \left(\frac{I_{L(RIPPLE)}}{2} \times \frac{(R_{SENSE} \times n_I)}{g_m \times R_{TOTAL}}\right) + \frac{V_{GNL}}{g_m \times R_{TOTAL}} - \frac{V_{CC}}{2 \times g_m \times R_{OGM}}$$

$$K = \left(\frac{3.8\,A}{2} \times \frac{4\,m\Omega \times 25}{2.2\,mmho \times 9.1\,k\Omega}\right) + \frac{1.174}{2.2\,mmho \times 9.1\,k\Omega} - \frac{12\,V}{2 \times 2.2\,mmho \times 130\,k\Omega} \quad (28)$$

$$= 4.7 \times 10^{-2}$$

$$V_{GNL} = V_{GNLO} + \frac{I_{L(RIPPLE)} \times R_{SENSE} \times n_I}{2} - \left(\frac{V_{IN} - V_{VID}}{L} \times t_D \times R_{SENSE} \times n_I\right)$$

$$V_{GNL} = 1V + \frac{3.8\,A \times 4\,m\Omega \times 25}{2} - \left(\frac{5\,V - 1.7\,V}{1.5\,\mu H} \times 75\,ns \times 4\,m\Omega \times 25\right) = 1.174\,V \quad (29)$$

$$V_{OUT(OS)} = \left(V_{OUT(MAX)} - V_{VID}\right) - \frac{R_{E(MAX)} \times I_{L(RIPPLE)}}{2} - V_{VID} \times k_{VID}$$

$$V_{OUT(OS)} = 40\,mV - \frac{5\,m\Omega \times 3.8\,A}{2} - 1.7\,V \times 5 \times 10^{-3} = 22\,mV \quad (30)$$

Finally, the compensating capacitance is determined from the equality of the pole frequency of the error amplifier gain and the zero frequency of the impedance of the output capacitor:

$$C_{OC} = \frac{C_{OUT} \times ESR}{R_{TOTAL}} = \frac{5\,mF \times 4.8\,m\Omega}{9.1\,k\Omega} = 2.6\,nF \quad (31)$$

The closest standard value for C_{OC} is 2.7 nF

Trade-Offs Between DC Load Regulation and AC Load Regulation

Casual observation of the circuit operation—e.g., with a voltmeter—would make it appear that the dc load regulation appears to be rather poor compared to a conventional regulator (see Figure 4). This would be especially noticeable under very light or very heavy loads where the voltage is "positioned" near one of the extremes of the regulation window rather than near the nominal center value. It must be noted and understood that this low gain characteristic (i.e., loose dc load regulation) is inherently required to allow improved transient containment (i.e., to achieve tighter ac load regulation). That is, the dc load regulation is intentionally sacrificed (but kept within specification) in order to minimize the number of capacitors required to contain the load transients produced by the CPU.

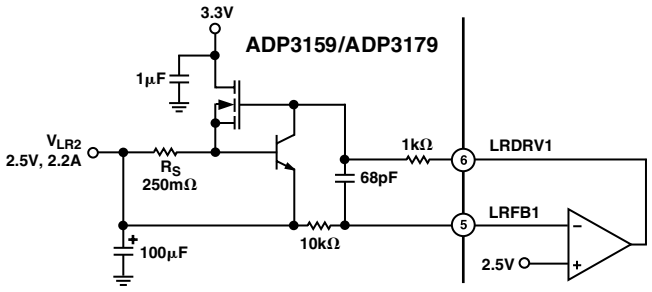


Figure 6. Adding Overcurrent Protection to the Linear Regulator

Linear Regulators

The two linear regulators provide a low cost, convenient and versatile solution for generating additional supply rails. The maximum output load current is determined by the size and thermal impedance of the external N-channel power MOSFET that is placed in series with the supply. The output voltage is sensed at the LRFB pin and compared to an internal reference voltage in a negative feedback loop which keeps the output voltage in regulation. If the load is reduced or increased, the MOSFET drive will also be reduced or increased by the controller IC to provide a well-regulated ±2.5% accurate output voltage.

The LRFB threshholds of the ADP3159 are internally set at 2.5 V(LRFB1) and 1.8 V(LRFB2), while the LRFB pins of the ADP3179 are compared to an internal 1 V reference. This allows the use of an external resistor divider network to program the linear regulator output voltage. The correct resistor values for setting the output voltage of the linear regulators in the ADP3179 can be determined using:

$$V_{OUT(LR)} = V_{LRFB} \times \frac{R_U + R_L}{R_L} \quad (32)$$

Assuming that R_L =10 kΩ, $V_{OUT(LR)}$ = 1.2 V and rearranging equation 32 to solve for R_U yields:

$$R_U = \frac{10\,k\Omega \times \left(V_{OUT(LR)} - V_{LRFB}\right)}{V_{LRFB}} \quad (33)$$

$$R_U = \frac{10\,k\Omega \times \left(1.2V - 1V\right)}{1V} = 2\,k\Omega$$

Efficiency of the Linear Regulators

The efficiency and corresponding power dissipation of each of the linear regulators are not determined by the controller IC. Rather, these are a function of input and output voltage and load current. Efficiency is approximated by the formula:

$$\eta = 100\% \times \frac{V_{OUT}}{V_{IN}} \quad (34)$$

The corresponding power dissipation in the MOSFET, together with any resistance added in series from input to output, is given by:

$$P_{LDO} = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (35)$$

Minimum power dissipation and maximum efficiency are accomplished by choosing the lowest available input voltage that exceeds the desired output voltage. However, if the chosen input source is itself generated by a linear regulator, its power dissipation will be increased in proportion to the additional current it must now provide.

Implementing Current Limit for the Linear Regulators

The circuit of Figure 6 gives an example of a current limit protection circuit that can be used in conjunction with the linear regulators. The output voltage is internally set by the LRFB pin. The value of the current sense resistor may be calculated as follows:

$$R_S \cong \frac{540\ mV}{I_{O(MAX)}} = \frac{540\ mV}{2.2\ A} = 250\ m\Omega \quad (36)$$

The power rating of the current sense resistor must be at least:

$$P_{D(R_S)} = R_S \times I_{O(MAX)}{}^2 = 1.2\ W \quad (37)$$

The maximum linear regulator MOSFET junction temperature with a shorted output is:

$$T_{J(MAX)} = T_A + (\theta_{JC} \times V_{IN} \times I_{O(MAX)})$$
$$T_{J(MAX)} = 50°C + (1.4°C/W \times (3.3V \times 2.2\ A) = 60°C \quad (38)$$

which is within the maximum allowed by the MOSFET's data sheet specification. The maximum MOSFET junction temperature at nominal output is:

$$T_{J(NOM)} = T_A + (\theta_{JC} \times (V_{IN} - V_{OUT}) \times I_{O(NOM)})$$
$$T_{J(NOM)} = 50°C + (1.4°C/W \times (3.3V - 2.5\ V) \times 2\ A) = 52°C \quad (39)$$

This example assumes an infinite heatsink. The practical limitation will be based on the actual heatsink used.

LAYOUT AND COMPONENT PLACEMENT GUIDELINES

The following guidelines are recommended for optimal performance of a switching regulator in a PC system:

General Recommendations

1. For best results, a four-layer PCB is recommended. This should allow the needed versatility for control circuitry interconnections with optimal placement, a signal ground plane, power planes for both power ground and the input power (e.g., 5 V), and wide interconnection traces in the rest of the power delivery current paths.
2. Whenever high currents must be routed between PCB layers, vias should be used liberally to create several parallel current paths so that the resistance and inductance introduced by these current paths is minimized and the via current rating is not exceeded.
3. If critical signal lines (including the voltage and current sense lines of the controller IC) must cross through power circuitry, it is best if a ground plane can be interposed between those signal lines and the traces of the power circuitry. This serves as a shield to minimize noise injection into the signals at the cost of making signal ground a bit noisier.
4. The GND pin of the controller IC should connect first to a ceramic bypass capacitor (on the VCC pin) and then into the power ground plane. However, the ground plane should not extend under other signal components, including the ADP3159 itself.
5. The output capacitors should also be connected as closely as possible to the load (or connector) that receives the power (e.g., a microprocessor core). If the load is distributed, the capacitors should also be distributed, and generally in proportion to where the load tends to be more dynamic. It is also advised to keep the planar interconnection path short (i.e., have input and output capacitors close together).
6. Absolutely avoid crossing any signal lines over the switching power path loop, described below.

Power Circuitry

7. The switching power path should be routed on the PCB to encompass the smallest possible area in order to minimize radiated switching noise energy (i.e., EMI). Failure to take proper precaution often results in EMI problems for the entire PC system as well as noise-related operational problems in the power converter control circuitry. The switching power path is the loop formed by the current path through the input capacitors, the two FETs, and the power Schottky diode, if used, including all interconnecting PCB traces and planes. The use of short and wide interconnection traces is especially critical in this path for two reasons: it minimizes the inductance in the switching loop, which can cause high-energy ringing, and it accommodates the high current demand with minimal voltage loss.

8. A power Schottky diode (1 ~ 2 A dc rating) placed from the lower MOSFET's source (anode) to drain (cathode) will help to minimize switching power dissipation in the upper MOSFET. In the absence of an effective Schottky diode, this dissipation occurs through the following sequence of switching events. The lower MOSFET turns off in advance of the upper MOSFET turning on (necessary to prevent cross-conduction). The circulating current in the power converter, no longer finding a path for current through the channel of the lower MOSFET, draws current through the inherent body-drain diode of the MOSFET. The upper MOSFET turns on, and the reverse recovery characteristic of the lower MOSFET's body-drain diode prevents the drain voltage from being pulled high quickly. The upper MOSFET then conducts very large current while it momentarily has a high voltage forced across it, which translates into added power dissipation in the upper MOSFET. The Schottky diode minimizes this problem by carrying a majority of the circulating current when the lower MOSFET is turned off, and by virtue of its essentially nonexistent reverse recovery time.
9. Whenever a power-dissipating component (e.g., a power MOSFET) is soldered to a PCB, the liberal use of vias, both directly on the mounting pad and immediately surrounding it, is recommended. Two important reasons for this are: improved current rating through the vias (if it is a current path), and improved thermal performance—especially if the vias extend to the opposite side of the PCB where a plane can more readily transfer the heat to the air.
10. The output power path, though not as critical as the switching power path, should also be routed to encompass a small area. The output power path is formed by the current path through the inductor, the current sensing resistor, the output capacitors, and back to the input capacitors.
11. For best EMI containment, the ground plane should extend fully under all the power components. These are: the input capacitors, the power MOSFETs and Schottky diode, the inductor, the current sense resistor, any snubbing elements that might be added to dampen ringing, and the output capacitors.

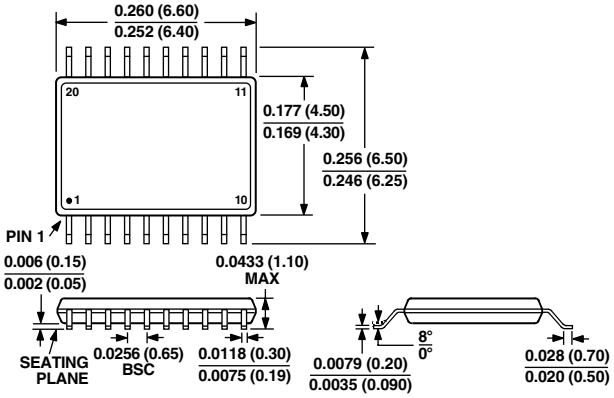
Signal Circuitry

12. The output voltage is sensed and regulated between the GND pin (which connects to the signal ground plane) and the CS– pin. The output current is sensed (as a voltage) and regulated between the CS– pin and the CS+ pin. In order to avoid differential mode noise pickup in those sensed signals, their loop areas should be small. Thus the CS– trace should be routed atop the signal ground plane, and the CS+ and CS– traces should be routed as a closely coupled pair (CS+ should be over the signal ground plane as well).
13. The CS+ and CS– traces should be Kelvin-connected to the current sense resistor so that the additional voltage drop due to current flow on the PCB at the current sense resistor connections does not affect the sensed voltage. It is desirable to have the ADP3159 close to the output capacitor bank and not in the output power path, so that any voltage drop between the output capacitors and the GND pin is minimized, and voltage regulation is not compromised.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

20-Lead TSSOP
(RU-20)



Revision History

Location	Page
Global change from ADP3159 to ADP3159/ADP3179	
Data Sheet changed from REV. 0 to REV. A.	
Edits to GENERAL DESCRIPTION	1
Edits to FUNCTIONAL BLOCK DIAGRAM	1
Addition to LINEAR REGULATORS section of the SPECIFICATIONS	2
Edit to ERROR AMPLIFIER section	2
Addition to ORDERING GUIDE	3
Edits to the On-board Linear Regulator Controllers section	5
Edits to Figure 3	6
Edits to Equation 24	10
Edits to Feedback Compensation for Active Voltage Positioning section	10
Edit to Equation 27	11
Addition of new text to Linear Regulators section	11

C02190–1–7/01(A)

PRINTED IN U.S.A.