FEATURES
Single +5V Operation with External Positive
 Reference
Fast Conversion Time: 10µs
No Missed Codes Over Full Temperature Range
Microprocessor Compatible
Low Cost
Low Power (15mW)
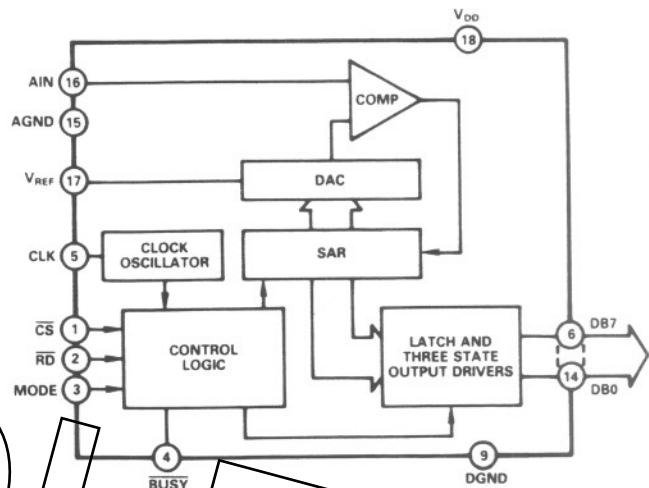100ns Data Access Time

AD7576 FUNCTIONAL BLOCK DIAGRAM

GENERAL DESCRIPTION

The AD7576 is a low cost, low power, microprocessor compatible 8-bit analog-to-digital converter, which uses the successive approximation technique to achieve a fast conversion time of 10µs. The device is designed to operate with an external reference of +1.23V (standard bandgap reference) and converts input signals from 0V to $2V_{REF}$.

The part is designed for ease of microprocessor interface with three control inputs ($\overline{CS}$, $\overline{RD}$ and MODE) controlling all ADC operations such as starting conversion and reading data. The interface logic allows the part to be easily configured as a memory mapped device. All data outputs use latched, three-state output buffer circuitry to allow direct connection to a microprocessor data bus or system input port. The output latches serve to make the conversion process transparent to the microprocessor.

The part is designed for single +5V operation, has on-board comparator, interface logic, and internal/external clock option. This makes the AD7576 ideal for most ADC/µP interface applications.

The AD7576 is fabricated in an advanced, all ion-implanted high speed Linear Compatible CMOS (LC²MOS) process and is available in either a small, 0.3″ wide, 18-pin DIP or in 20-terminal surface mount packages.

PRODUCT HIGHLIGHTS

1. Single Supply Operation
Operation from a single +5V supply with a +1.23V reference allows operation of the AD7576 with microprocessor systems without any additional power supplies.

2. Low Power
CMOS fabrication of the AD7576 results in a very low power dissipation figure of 15mW typical.

3. Versatile Interface Logic
The AD7576 can be configured to perform continuous conversions or to convert on command. It can be interfaced as SLOW-MEMORY or ROM, allowing versatile interfacing to most microprocessors.

4. Fast Conversion Time
The fabrication of the AD7576 on Analog Devices' Linear Compatible CMOS (LC²MOS) process enables fast conversion times of 10µs, eliminating the need for expensive Sample-and-Holds in many low frequency applications.

ORDERING INFORMATION[1]

Relative Accuracy (LSB)	Temperature Range and Package Options[2]		
	0 to +70°C	−25°C to +85°C	−55°C to +125°C
	Plastic DIP (N-18)	Hermetic DIP (Q-18)	Hermetic DIP (Q-18)
±1	AD7576JN	AD7576AQ	AD7576SQ
±1/2	AD7576KN	AD7576BQ	AD7576TQ
	PLCC[3] (P-20A)		LCCC[4] (E-20A)
±1	AD7576JP		AD7576SE
±1/2	AD7576KP		AD7576TE

NOTES
[1]To order MIL-STD-883, Class B processed parts, add/883B to part number.
 Contact your local sales office for military data sheet.
[2]See Section 13 for package outline information.
[3]PLCC: Plastic Leaded Chip Carrier.
[4]LCCC: Leadless Ceramic Chip Carrier.

SPECIFICATIONS

($V_{DD} = +5V$; $V_{REF} = +1.23V$; AGND = DGND = 0V; $f_{CLK} = 2MHz$ external; All specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	J, A[1] Versions	K, B Versions	S Version	T Version	Units	Conditions/Comments
ACCURACY						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error	± 2	± 1	± 2	± 1	LSB max	
Relative Accuracy	± 1	± ½	± 1	± ½	LSB max	
Minimum Resolution for which						
No Missing Codes is Guaranteed	8	8	8	8	Bits max	
Full Scale Error						
25°C	± 1	± 1	± 1	± 1	LSB max	Full Scale TC is typically 5ppm/°C
T_{min} to T_{max}	± 1	± 1	± 1	± 1	LSB max	
Offset Error[2]						
25°C	± ½	± ½	± ½	± ½	LSB max	Offset TC is typically 5ppm/°C
T_{min} to T_{max}	± ½	± ½	± ½	± ½	LSB max	
ANALOG INPUT						
Voltage Range	0 to $2V_{REF}$	0 to $2V_{REF}$	0 to $2V_{REF}$	0 to $2V_{REF}$	Volts	$1LSB = 2V_{REF}/256$; See Figure 4
DC Input Impedance	10	10	10	10	MΩ min	
REFERENCE INPUT						
V_{REF} (For specified Performance)	1.23	1.23	1.23	1.23	Volts	± 5%
I_{REF}	500	500	500	500	µA max	
LOGIC INPUTS						
$\overline{CS}$, $\overline{RD}$, MODE						
V_{INL}, Input Low Voltage	0.8	0.8	0.8	0.8	V max	
V_{INH}, Input High Voltage	2.4	2.4	2.4	2.4	V min	
I_{IN}, Input Current						
25°C	± 1	± 1	± 1	± 1	µA max	$V_{IN} = 0$ or V_{DD}
T_{min} to T_{max}	± 10	± 10	± 10	± 10	µA max	$V_{IN} = 0$ or V_{DD}
C_{IN}, Input Capacitance[3]	10	10	10	10	pF max	
CLK						
V_{INL}, Input Low Voltage	0.8	0.8	0.8	0.8	V max	
V_{INH}, Input High Voltage	2.4	2.4	2.4	2.4	V min	
I_{INL}, Input Low Current	700	700	800	800	µA max	$V_{INL} = 0V$
I_{INH}, Input High Current	700	700	800	800	µA max	$V_{INH} = V_{DD}$
LOGIC OUTPUTS						
$\overline{BUSY}$, DB0 to DB7						
V_{OL}, Output Low Voltage	0.4	0.4	0.4	0.4	V max	$I_{SINK} = 1.6mA$
V_{OH}, Output High Voltage	4.0	4.0	4.0	4.0	V min	$I_{SOURCE} = 40µA$
DB0 to DB7						
Floating State Leakage Current	± 1	± 1	± 10	± 10	µA max	$V_{OUT} = 0$ to V_{DD}
Floating State Output Capacitance[3]	10	10	10	10	pF max	
CONVERSION TIME[4]						
With External Clock	10	10	10	10	µs	$f_{CLK} = 2MHz$
With Internal Clock, $T_A = 25°C$	10	10	10	10	µs min	Using recommended clock
	30	30	30	30	µs max	components shown in Figure 3.
POWER REQUIREMENTS[5]						
V_{DD}	+ 5	+ 5	+ 5	+ 5	Volts	± 5% for Specified Performance
I_{DD}	6	6	7	7	mA max	Typically 3mA with $V_{DD} = +5V$
Power Dissipation	15	15	15	15	mW typ	
Power Supply Rejection	± ¼	± ¼	± ¼	± ¼	LSB max	$4.75V \leq V_{DD} \leq 5.25V$

NOTES

[1]Temperature Ranges are as follows:

    J, K Versions; 0 to +70°C

    A, B Versions; −25°C to +85°C

    S, T Versions; −55°C to +125°C

[2]Offset error is measured with respect to an ideal first code transition which occurs at 1/2LSB.

[3]Sample tested at 25°C to ensure compliance.

[4]Accuracy may degrade at conversion times other than those specified.

[5]Power supply current is measured when AD7576 is inactive i.e. when $\overline{CS} = \overline{RD} = MODE = \overline{BUSY} = $ logic HIGH.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} TO AGND . . . . −0.3V, +7V
V_{DD} TO DGND . . . . −0.3V, +7V
AGND TO DGND . . . . −0.3V, V_{DD}
Digital Input Voltage to DGND . . . . . −0.3V, V_{DD} +0.3V
Digital Output Voltage to DGND . . . . −0.3V, V_{DD} +0.3V
CLK Input Voltage to DGND . . . . . . −0.3V, V_{DD} +0.3V
V_{REF} to AGND . . . . −0.3V, V_{DD}
AIN TO AGND . . . . −0.3V, V_{DD}
Operating Temperature Range
 Commercial (J, K Version) . . . . 0 to +70°C

Industrial (A, B Version) . . . . −25°C to +85°C
 Extended (S, T Version) . . . . −55°C to +125°C
Storage Temperature Range . . . . −65°C to +150°C
Lead Temperature (soldering, 10 secs) . . . . 300°C
Power Dissipation (Any Package) to +75°C 450mW
Derates above 75°C by . . . . 6mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are Zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

PIN CONFIGURATIONS

NC = NO CONNECT
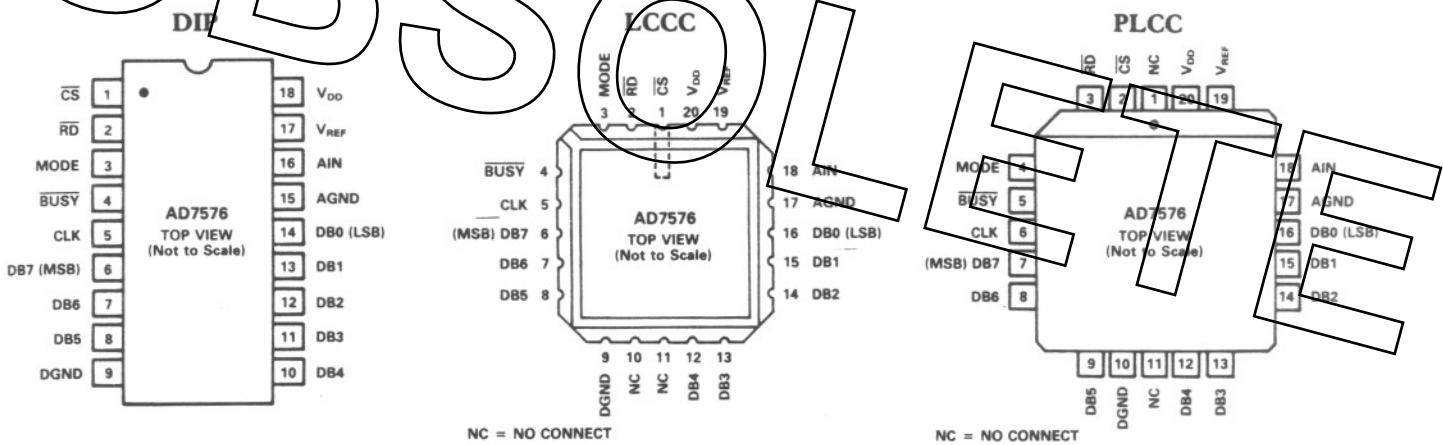
A SAMPLED-DATA INPUT

The AD7576 makes use of a sampled-data comparator. The equivalent input circuit is shown in Figure 1. When a conversion starts, switch S1 is closed and the equivalent input capacitance is charged to V_{IN}. With a switch resistance of typically 500Ω and an input capacitance of typically 2pF the input time constant is 1ns. Thus C_{IN} becomes charged to within ±¼ LSB in 6.9 time constants or about 7ns. Since the comparator switches are operating at one half the input clock frequency of 2MHz, there is ample time for the input voltage to settle before the comparator decision is made (at the end of a clock period). Increasing the source resistance increases the settling time required. Input bypass capacitors placed directly at the analog input act to average the input charging currents. This average current flowing through any source impedance can cause full-scale errors.
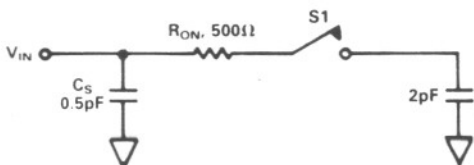

Figure 1. AD7576 Equivalent Input Circuit

REFERENCE INPUT

The reference input impedance on the AD7576 is code dependent and varies by a ratio of approximately 3-to-1 over the digital code range. The typical resistance range is from 6kΩ to 18kΩ. As a result of the code dependent input impedance, the V_{REF} input must be driven from a low impedance source. Figure 2 shows how an AD589 can be configured to produce a nominal reference voltage of +1.23V.
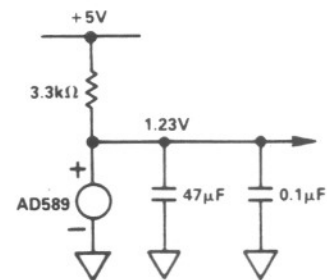

Figure 2. Reference Circuit

Unipolar/Bipolar Considerations

UNIPOLAR OPERATION

The basic operation for the AD7576 is in the unipolar single supply mode. Figure 3 shows the circuit connections to achieve this while the nominal transfer characteristic for unipolar operation is given in Figure 4. Since the offset and full-scale errors on the AD7576 are very small, in many cases it will not be necessary to adjust out these errors. If calibration is required the procedure is as follows:

Offset Adjust

Offset error adjustment in single-supply systems is easily achievable by means of the offset null facility of an op-amp when used as a voltage follower for the analog input signal, AIN. The op-amp chosen should be able to operate from a single supply and allow a common-mode input voltage range that includes 0V (e.g., TLC271). To adjust for zero offset the input signal source is set to +4.8mV (i.e., 1/2LSB) while the op-amp offset is varied until the ADC output code flickers between 000 . . . 00 and 000 . . . 01.

Full Scale Adjust

The full scale or gain adjustment is made by forcing the analog input AIN to +2.445V (i.e., Full-Scale Voltage −3/2LSB). The magnitude of the reference voltage is then adjusted until the ADC output code flickers between 111 . . . 10 and 111 . . . 11.
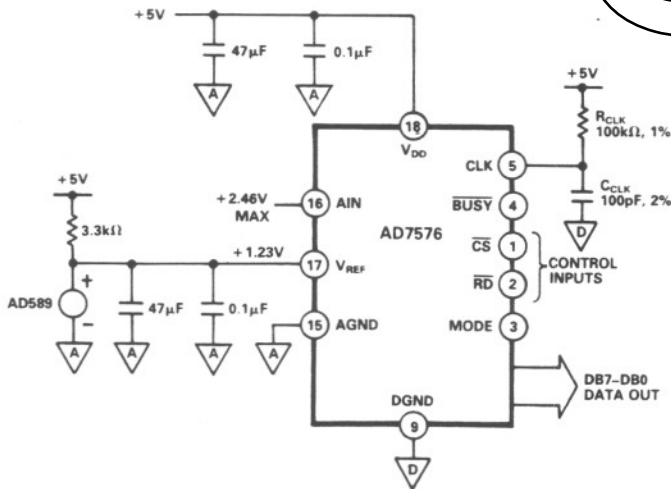
BIPOLAR OPERATION

The circuit of Figure 5 shows how the AD7576 can be configured for bipolar operation. The output code provided by the AD7576 is offset binary. The analog input voltage range is ±5V, although the voltage appearing at the AIN pin of the AD7576 is in the range 0V to +2.46V. Figure 6 shows the transfer function for bipolar operation. The LSB size is now 39.06mV. Calibration of the bipolar operation is outlined below. Once again, because the errors are small it may not be necessary to adjust them. To maintain specified performance without the calibration all resistors should be 0.1% tolerance with R4 and R5 replaced by one 3.3kΩ resistor and R2 and R3 replaced by one 2.5kΩ resistor.

Offset Adjust

Offset error adjustment is achieved by applying an analog input voltage of −4.9805V (−FS/2 +1/2LSB). Resistor R3 is then adjusted until the output code flickers between 000 . . . 00 and 000 . . . 01.

Full Scale Adjust

Full scale or gain adjustment is made by applying an analog input voltage of +4.9414V (+FS/2 −3/2LSB). Resistor R4 is then adjusted until the output code flickers between 111 . . . 10 and 111 . . . 11.

Figure 3. AD75765 Unipolar Configuration

Figure 5. AD7576 Bipolar Configuration

Figure 4. Nominal Transfer Characteristic for Unipolar Operation
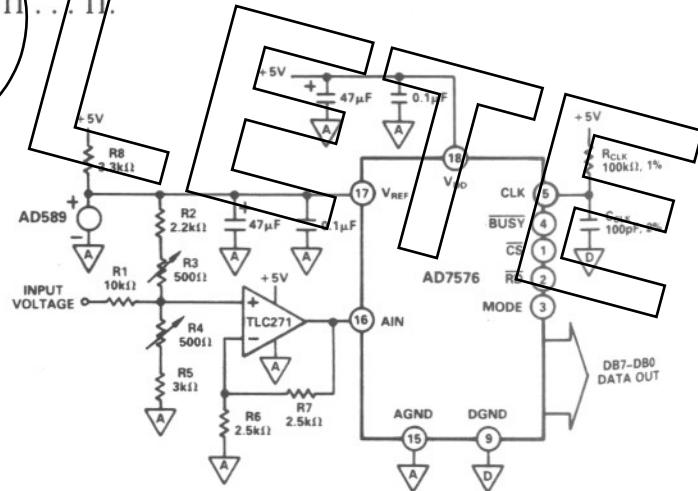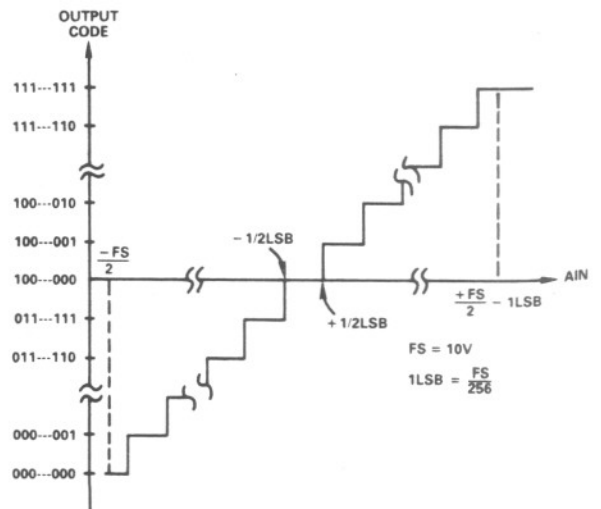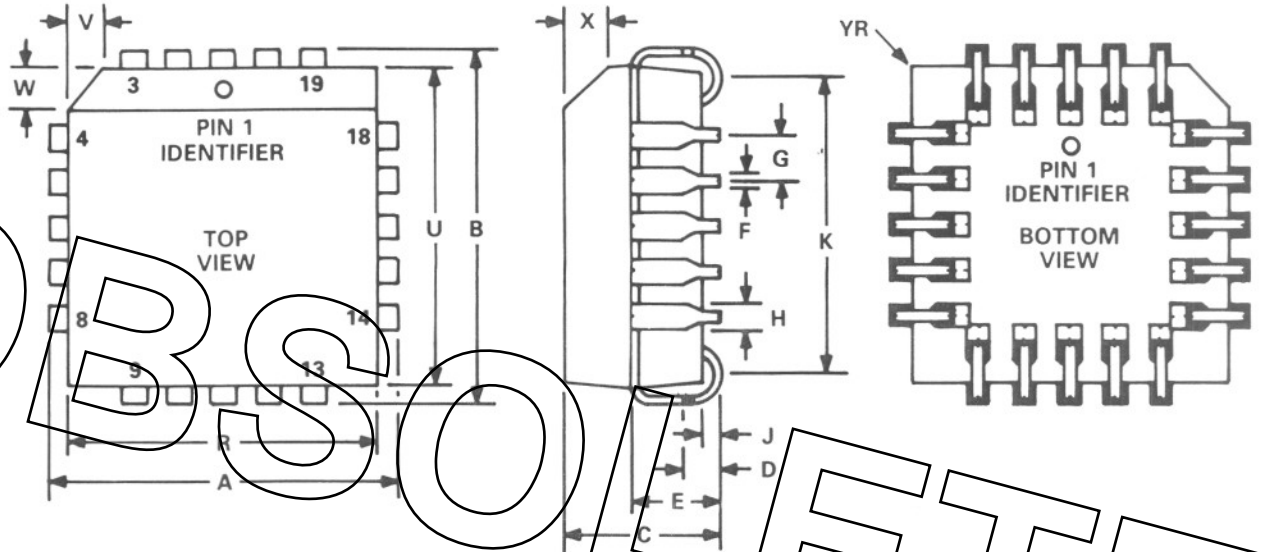

Figure 6. Nominal Transfer Characteristic for Bipolar Operation

P-20A
20-Lead Plastic Leaded Chip Carrier (PLCC)

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.02
B	0.385	0.395	9.78	10.02
C	0.165	0.180	4.19	4.57
D	0.025	0.040	0.64	1.01
E	0.085	0.110	2.16	2.79
F	0.013	0.021	0.33	0.53
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.015	0.025	0.38	0.63
K	0.290	0.330	7.37	8.38
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y		0.020		0.50