1.1 Scope.

This specification covers the detail requirements for a hybrid quad 12-bit voltage output CMOS D/A converter with individual DAC reference inputs.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
−1	AD394SD/883B
−2	AD394TD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000: package outline: DH-28A.

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

$+V_S$ to DGND	−0.3V to +17V
$-V_S$ to DGND	+0.3V to −17V
Digital Inputs (Pins 1–16) to DGND	−0.3V to +7V
V_{REFIN} to DGND	±25V
AGND to DGND	−0.3V to $+V_S$
Analog Outputs (Pins 18, 21, 24, 27)	Indefinite
	Short to AGND or DGND Momentary Short to $\pm V_S$
Operating Temperature Range (Ambient)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10secs)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 8°C/W typ
θ_{JA} = 25°C/W typ

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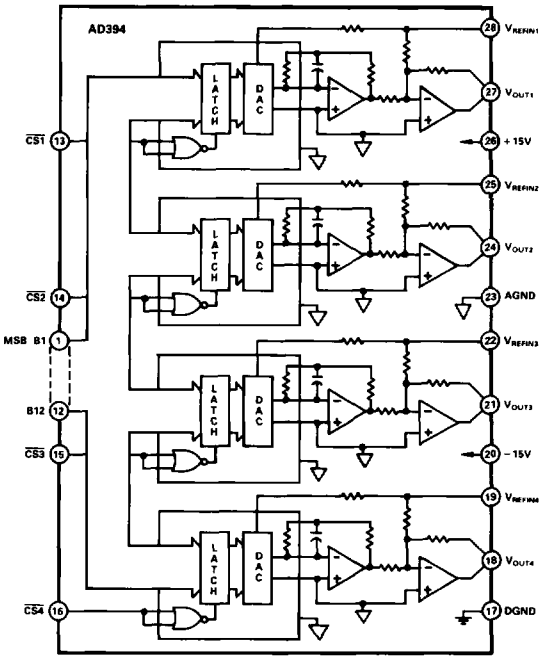
Table 1.

Test	Symbol	Device	Design Limit @ 25°C/(−55°C to +125°C)	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition[1]	Units
Data Input Voltage High	V_{IH}	−1, 2	2.4/(2.4)			2.4	Test Limits Apply	+V min
			5.5/(5.5)				to Pins 1–12. Design	+V max
End Point Electrical		−1, 2		2.4			Limits Apply to Pins 13–16.	+V min
Data Input Voltage Low	V_{IL}	−1, 2	0.0/(0.0)				Test Limits Apply	+V min
			0.8/(0.8)			0.8	to Pins 1–12. Design	+V max
End Point Electrical		−1, 2		0.8			Limits Apply to Pins 13–16.	+V min
Input Current High	I_{IH}	−1, 2	40/(40)			40	V_{IN} = 0V or +5V	±μA max
Input Current Low	I_{IL}	−1, 2	40/(40)			40	V_{IN} = 0V or +5V	±μA max
End Point Electrical	I_{IH}, I_{IL}	−1, 2		40				
Output Voltage Range[2]	V_{OUT}	−1, 2	11/(11)			10	Output Voltage	−V min
			11/(11)			10	Equals −REFIN to +REFIN	+V max
Output Current Range	I_{OR}	−1, 2	5/(5)					±mA min
Gain Error	A_E	−1	0.1	0.1			External +10.000V REF	±%FSR[3] max
		−2	0.05			0.05	Bit Code = 1111 1111 1111	
End Point Electrical		−1, 2		0.2				
Gain Error Temperature Coefficient	TC_{AE}	−1	/(10)		10		External +10.000V REF	±ppm/°C max
		−2	/(5)		5		Bit Code = 1111 1111 1111	
Offset Error	V_{OS}	−1	0.05	0.05			External +10.000V REF	±%FSR max
		−2	0.025			0.025	Bit Code = 0000 0000 0000	
End Point Electrical		−1, 2		0.1				
Offset Temperature Coefficient	TC_{BPZ}	−1	/(10)		10		External +10.000V REF	±ppm/°C max
		−2	/(5)		5		Bit Code = 0000 0000 0000	
Differential Linearity Error[4]	DLE	−1	3/4	3/4	1			±LSB max
		−2	1/2		1	1/2		
End Point Electrical		−1, 2		1.5				
Linearity Error[5]	TC_{LE}	−1	3/4	3/4	3/4			±LSB max
		−2	1/2	1/2	1/2			
End Point Electrical		−1, 2		1				
Power Supply Voltages[2]	V_S	−1, 2	13.5/(13.5)	15	15			−V min
		−1, 2	16.5/(16.5)	15	15			V max
Power Supply Currents	I_{CC}	−1, 2	28/(35)			28	Data Input Bits = 1111 1111 1111 $R_L = \infty$	−mA max
	I_{EE}		22/(22)			22	Data Input Bits = 1111 1111 1111 $R_L = \infty$	+mA max
Power Supply Gain Sensitivity Δ Gain/ ΔV_S(+V_S and −V_S)	PSRR	−1, 2	0.006			0.006	Input Bits = 1111 1111 1111 V_S = ±15V ±10%	±%FS/%
Timing Specifications Chip Select	t_{CS}	−1, 2	170				See Figure 1	ns min
Data Access Time	t_{DA}	−1, 2	0				See Figure 1	ns min
Data Setup Time	t_{DS}	−1, 2	150				See Figure 1	ns min
Data Hold Time	t_{DH}	−1, 2	5				See Figure 1	ns min

NOTES
[1] T_A = +25°C and ±V_S = ±15V, V_{REFIN} = +10V.
[2] The AD394 can be used with supplies as low as ±11.4V. See page 6, Figure 10 of product data sheet.
[3] FSR means Full-Scale Range and is equal to 20V for a ±10V bipolar range and 10V for 0 to 10V unipolar range.
[4] Monotonicity is tested for over the full military temperature.
[5] Integral nonlinearity is a measure of the maximum deviation from a straight line passing through the end points of the transfer function.

3.2.1 Functional Block Diagram and Terminal Assignments.



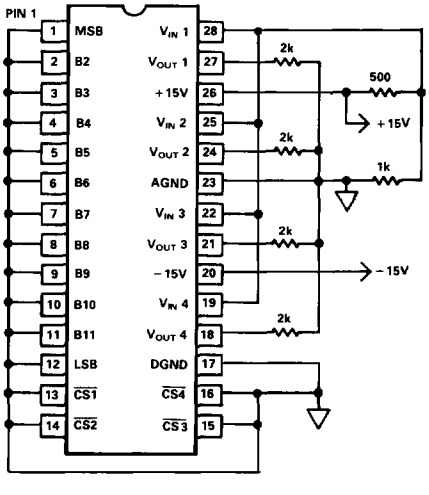
AD394 Functional Block Diagram

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (I).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



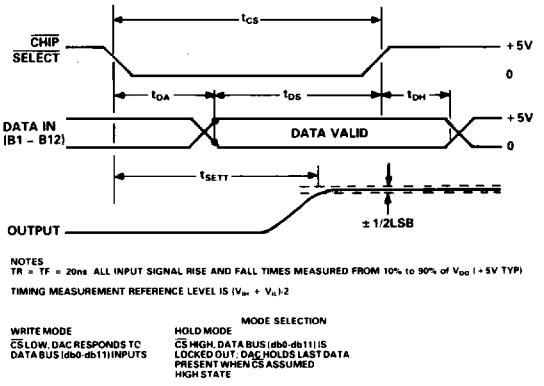


Figure 1. Timing Diagram

Table 2. DAC Select Matrix

$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$	$\overline{CS4}$	Operation
1	1	1	1	All DACs Latched
0	1	1	1	Load DAC 1 From Data Bus
1	0	1	1	Load DAC 2 From Data Bus
1	1	0	1	Load DAC 3 From Data Bus
1	1	1	0	Load DAC 4 From Data Bus
0	0	0	0	All DACs Simultaneously Loaded

Table 3. AD394 Bipolar Code Table

DATA INPUT			ANALOG OUTPUT	ANALOG OUTPUT VOLTAGE V_{REFIN} = +10 VOLTS	
1111	1111	1111	$+1 \cdot (V_{REFIN}) \left\{\frac{2047}{2048}\right\}$	+9.9951V	+FULL SCALE − 1LSB
1100	0000	0000	$+1 \cdot (V_{REFIN}) \left\{\frac{1024}{2048}\right\}$	+5.000V	+1/2 SCALE
1000	0000	0001	$+1 \cdot (V_{REFIN}) \left\{\frac{1}{2048}\right\}$	+4.88mV	+1LSB
1000	0000	0000	$+1 \cdot (V_{REFIN}) \left\{\frac{0}{2048}\right\}$	+0.000V	ZERO
0111	1111	1111	$-1 \cdot (V_{REFIN}) \left\{\frac{1}{2048}\right\}$	−4.88mV	−1LSB
0100	0000	0000	$-1 \cdot (V_{REFIN}) \left\{\frac{1024}{2048}\right\}$	−5.000V	−1/2 SCALE
0000	0000	0000	$-1 \cdot (V_{REFIN}) \left\{\frac{2048}{2048}\right\}$	−10.000V	−FULL SCALE