

- ★ Green Device Available
- ★ Super Low Gate Charge
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology
- ★ 100% EAS Guaranteed

Product Summary

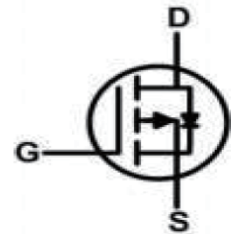


BVDSS	R <sub>DS(on)</sub>	I <sub>D</sub>
-40V	13.5mΩ	-40A

Description

The 40P04 is the high cell density trenched P-ch MOSFETs, which provides excellent R<sub>DS(on)</sub> and gate charge for most of the the synchronous buck converter applications. The 40P04 meets the RoHS and Green Product requirement 100% EAS Guaranteed with full function reliability approved.

TO252 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V <sub>DSS</sub>	Drain-Source Voltage	-40	V
V <sub>GSS</sub>	Gate-Source Voltage	±20	V
I <sub>D</sub>	Continuous Drain Current	T <sub>C</sub> = 25°C	-40
		T <sub>C</sub> = 100°C	-22
I <sub>DM</sub>	Pulsed Drain Current <small>note1</small>	-140	A
EAS	Single Pulsed Avalanche Energy <small>note2</small>	57.8	mJ
P <sub>D</sub>	Power Dissipation	T <sub>C</sub> = 25°C	40.3
R <sub>θJC</sub>	Thermal Resistance, Junction to Case	3.1	°C/W
R <sub>θJA</sub>	Thermal Resistance from Junction-to-Ambient <small>note3</small>	66	°C/W
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to 150	°C

**Electrical Characteristics ( $T_J = 25^\circ\text{C}$  unless otherwise specified)**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Units
<b>Static Characteristics</b>						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = -250\mu A$	-40	-	-	V
$I_{GSS}$	Gate-Body Leakage Current	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	-	$\pm 100$	nA
$I_{DSS}$	Zero Gate Voltage Drain Current	$T_J = 25^\circ\text{C}$	-	-	-1	$\mu A$
		$T_J = 100^\circ\text{C}$	-	-	-100	
$V_{GS(th)}$	Gate-Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1	-1.5	-2.2	V
$R_{DS(on)}$	Drain-Source on-Resistance <sup>4</sup>	$V_{GS} = 10V, I_D = -20A$	-	13.5	19	m $\Omega$
		$V_{GS} = -4.5V, I_D = -15A$	-	19.5	25	
$g_{fs}$	Forward Transconductance <sup>4</sup>	$V_{DS} = -10V, I_D = -20A$	-	44	-	S
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = -20V, V_{GS} = 0V,$ $f = 1\text{MHz}$	-	2525	-	pF
$C_{oss}$	Output Capacitance		-	190	-	
$C_{rss}$	Reverse Transfer Capacitance		-	172	-	
$R_G$	Gate Resistance	$f = 1\text{MHz}$	-	10	-	$\Omega$
<b>Switching Characteristics</b>						
$Q_g$	Total Gate Charge	$V_{GS} = -10V, V_{DD} = -20V,$ $I_D = -20A$	-	22	-	nC
$Q_{gs}$	Gate-Source Charge		-	4.2	-	
$Q_{gd}$	Gate-Drain Charge		-	6.9	-	
$t_{d(on)}$	Turn-on Delay Time	$V_{GS} = -10V, V_{DD} = -20V,$ $R_G = 3\Omega, I_D = -20A$	-	6.4	-	ns
$t_r$	Rise Time		-	15.3	-	
$t_{d(off)}$	Turn-off Delay Time		-	25	-	
$t_f$	Fall Time		-	7.6	-	
<b>Drain-Source Body Diode Characteristics</b>						
$V_{SD}$	Diode Forward Voltage <sup>4</sup>	$I_S = -20A, V_{GS} = 0V$	-	-	-1.2	V
$I_S$	Continuous Source Current	$T_C = 25^\circ\text{C}$	-	-	-40	A

**Notes:**

1. Repetitive rating, pulse width limited by junction temperature  $T_{J(MAX)} = 150^\circ\text{C}$ .
2. The EAS data shows Max. rating. The test condition is  $V_{DD} = -25V, V_{GS} = -10V, L = 0.1\text{mH}, I_{AS} = -34A$ .
3. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed, pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$ .
5. This value is guaranteed by design hence it is not included in the production test.

Typical Electrical and Thermal Characteristics (Curves)

Figure 1: Output Characteristics

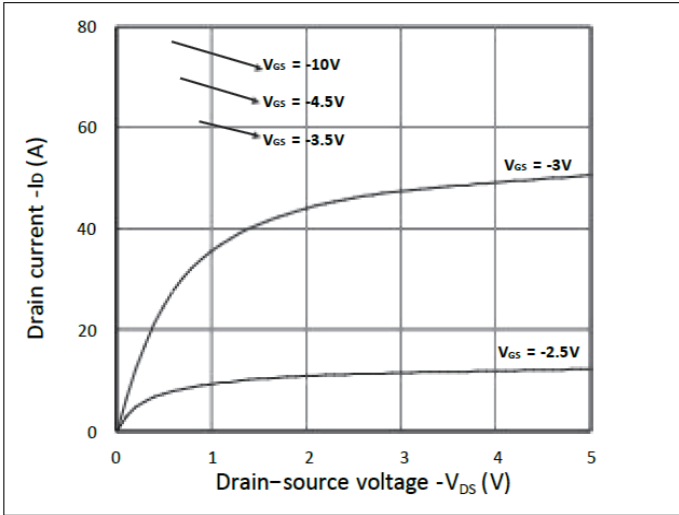


Figure 2: Transfer Characteristics

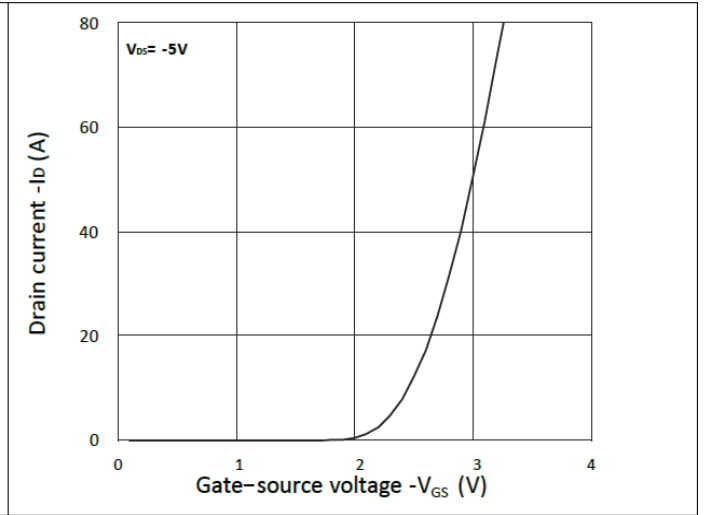


Figure 3: Forward Characteristics of Reverse

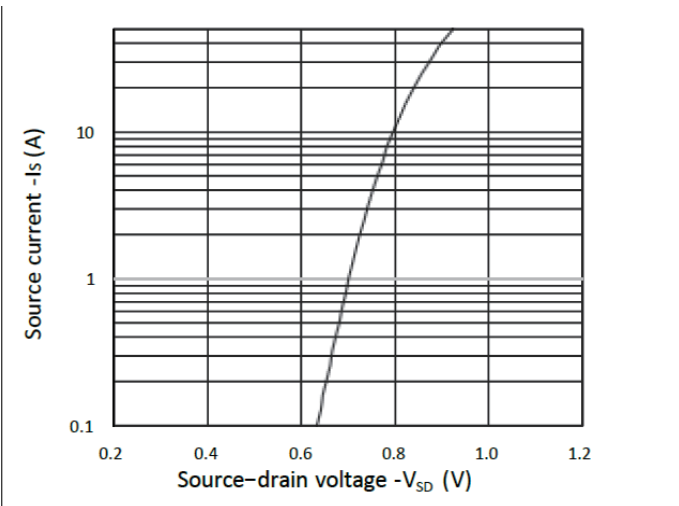


Figure 4: RDS(ON) vs . VGS

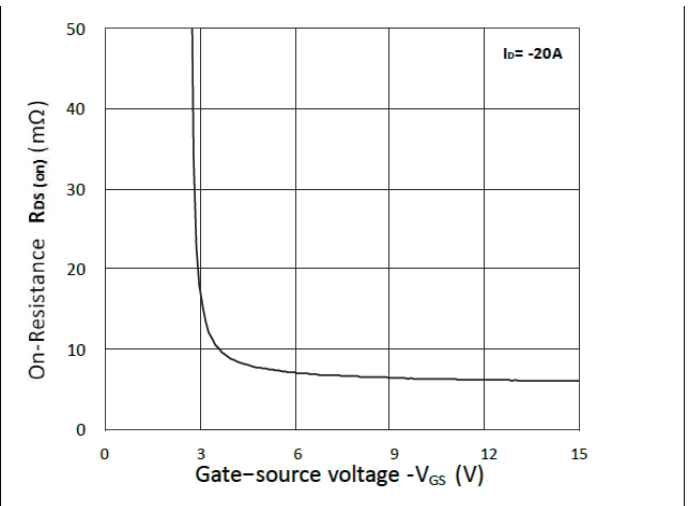


Figure 5: RDS(ON) vs . ID

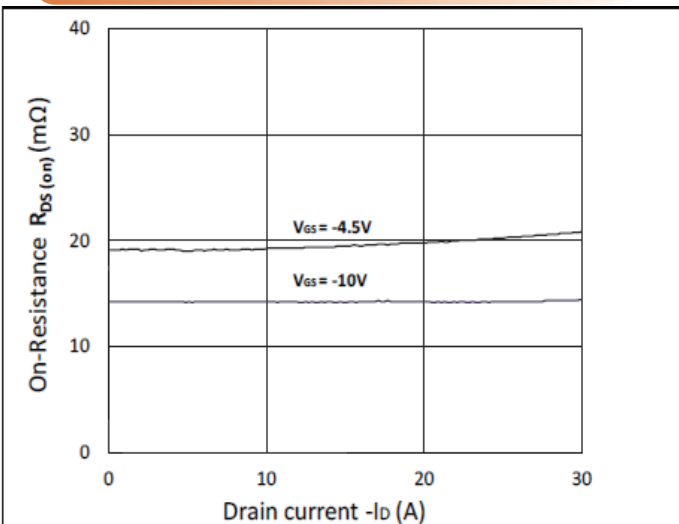
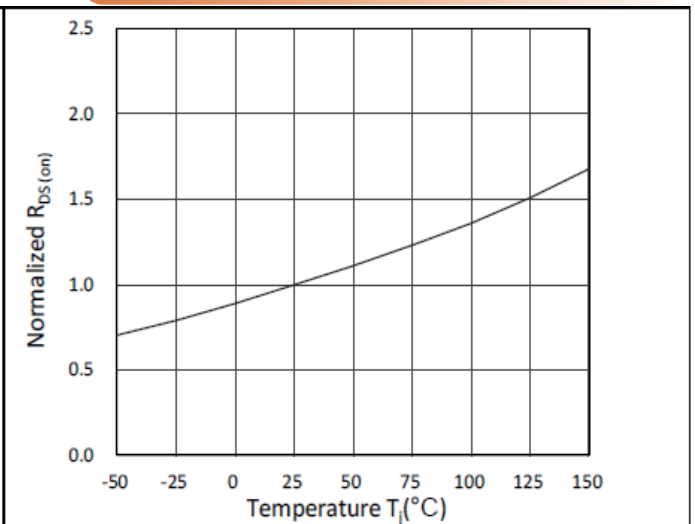


Figure 6: Normalized RDS( on) vs . Temper



Typical Performance Characteristics

Figure 7: Capacitance Characteristics

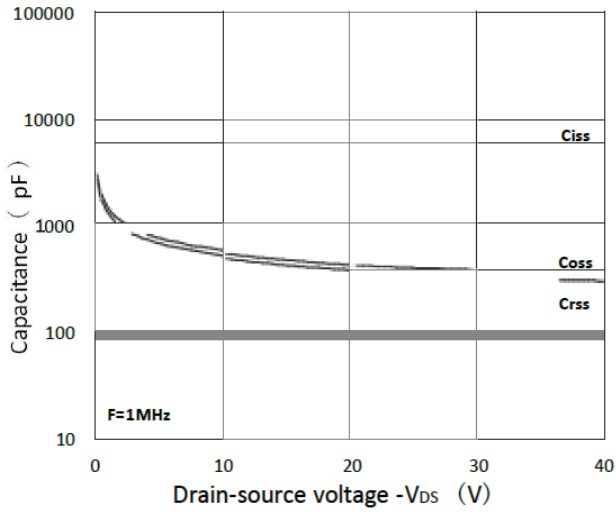


Figure 8: Gate Charge Characteristics

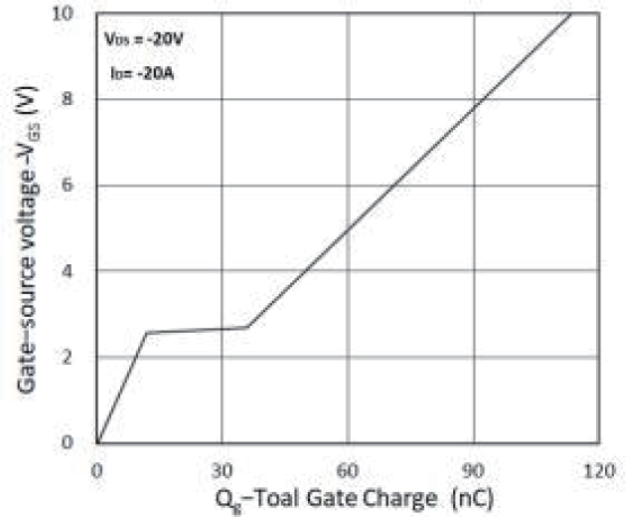


Figure 9: Power Dissipational Impedance

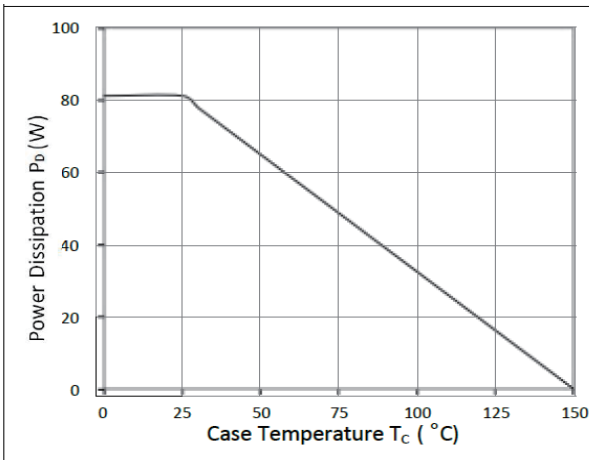


Figure 10: Safe Operating Area

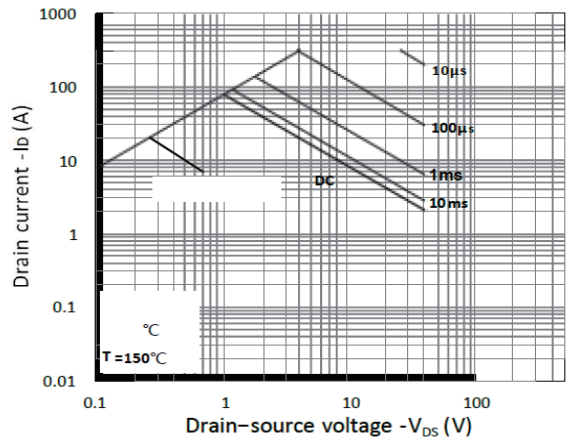
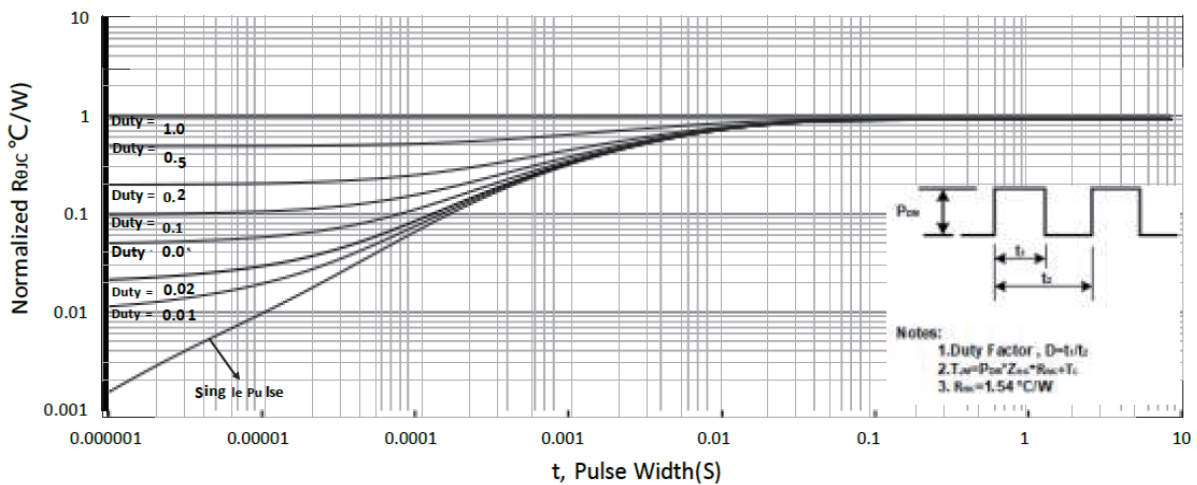


Figure 11: Normalized Maximum Transient Thermal Impedance



Test Circuit

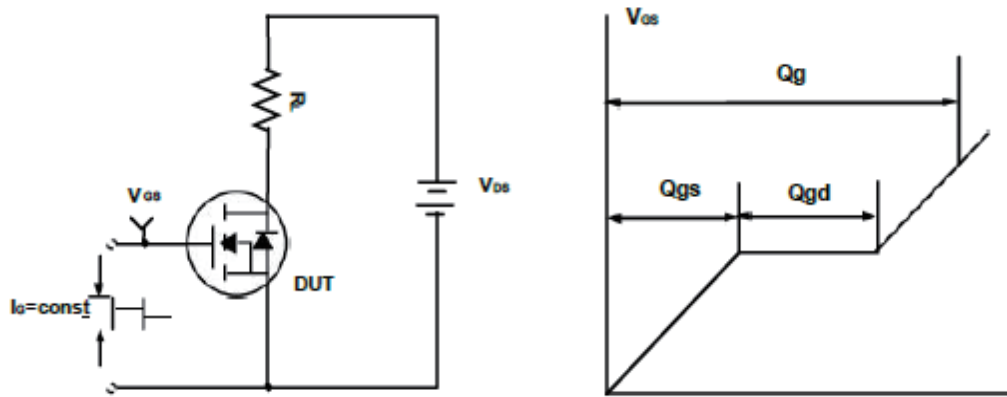


Figure A. Gate Charge Test Circuit & Waveforms

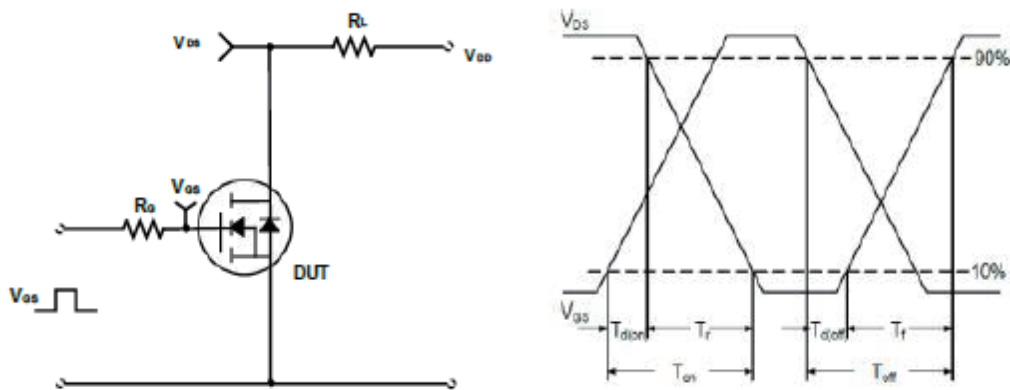


Figure B. Switching Test Circuit & Waveforms

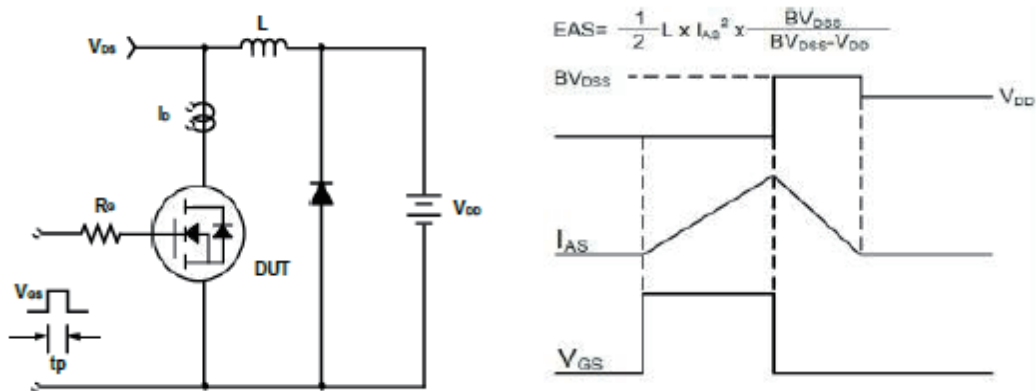
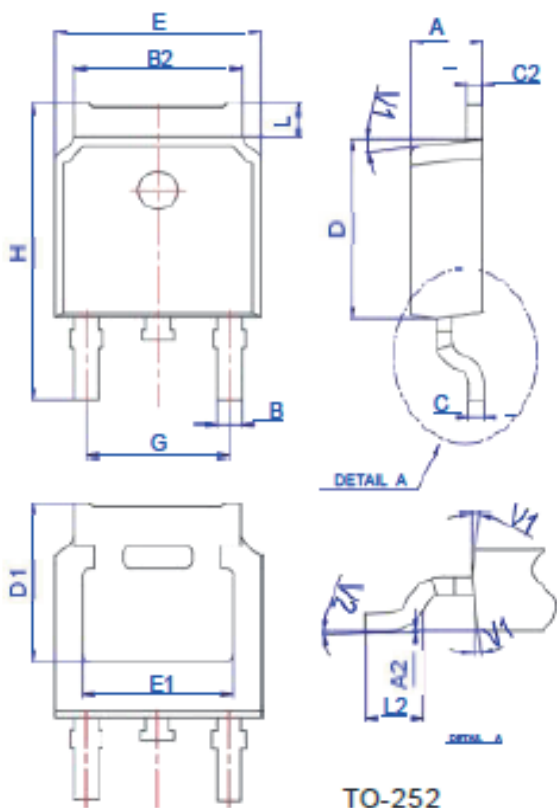


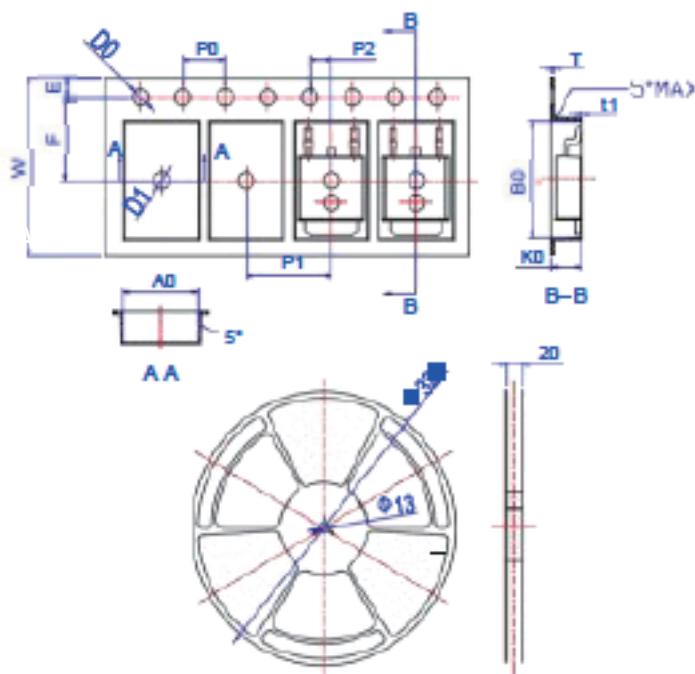
Figure C. Unclamped Inductive Switching Circuit & Waveforms

Package Mechanical Data-TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Reel Specification-TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583