Discontinued

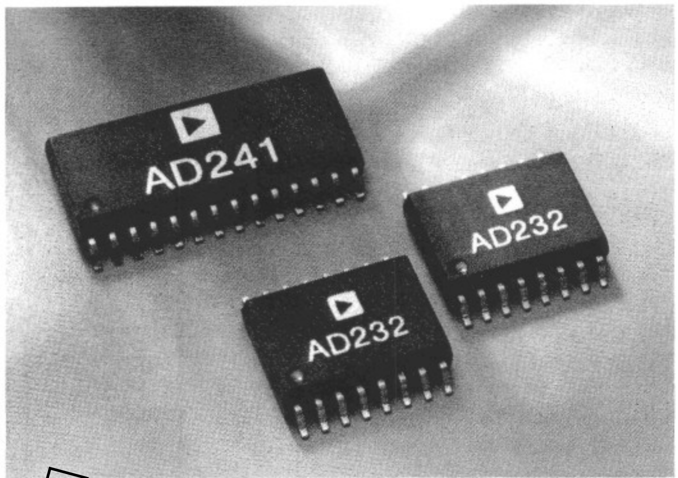
ANALOG DEVICES

+5 V Powered CMOS RS-232 Drivers/Receivers

AD230–AD241

FEATURES
- Single 5 V Power Supply
- Meets All RS-232-C and V.28 Specifications
- Multiple Drivers and Receivers
- On-Board DC-DC Converters
- ±9 V Output Swing with +5 V Supply
- Low Power CMOS: 5 mA Operation
- Low Power Shutdown ≤1 μA
- 3-State TTL/CMOS Receiver Outputs
- ±30 V Receiver Input Levels
- Plug-In Replacement for MAX230-241

APPLICATIONS
- Computers
- Peripherals
- Modems
- Printers
- Instruments



GENERAL DESCRIPTION

The AD230 family of 5 V only, RS-232 line drivers/receivers provides a variety of configurations to fit most communication needs, especially in applications where ±12 V is not available. The AD230, AD235, AD236 and AD241 feature a low power shutdown mode which reduces power dissipation to less than 5 μW making them ideally suited for battery powered equipment. The AD233 and AD235 do not require any external components and are particularly useful in applications where printed circuit board space is critical.

All members of the AD230 family, except the AD231 and the AD239, include two internal charge pump voltage converters which allow operation from a single +5 V supply. These converters convert the +5 V input power to the ±10 V required for RS-232 output levels. The AD231 and AD239 are designed to operate from +5 V and +12 V supplies. An internal +12 V to −12 V charge pump voltage converter generates the −12 V supply.

In order to minimize the package count in all applications, a wide selection of driver/receiver combinations is available (see table below).

SELECTION TABLE

Part Number	Power Supply Voltage	No. of RS-232 Drivers	No. of RS-232 Receivers	External Capacitors	Low Power Shutdown (SD)	TTL Three-State $\overline{EN}$	No. of Pins
AD230	+5 V	5	0	4	Yes	No	20
AD231	+5 V & +7.5 V to 13.2V	2	2	2	No	No	14
AD232	+5 V	2	2	4	No	No	16
AD233	+5 V	2	2	None	No	No	20
AD234	+5 V	4	0	4	No	No	16
AD235	+5 V	5	5	None	Yes	Yes	24
AD236	+5 V	4	3	4	Yes	Yes	24
AD237	+5 V	5	3	4	No	No	24
AD238	+5 V	4	4	4	No	No	24
AD239	+5 V & +12 V	3	5	2	No	Yes	24
AD241	+5 V	4	5	4	Yes	Yes	28

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SPECIFICATIONS

(V_{CC} = +5 V ± 10% (AD231, AD232, AD234, AD236, AD238, AD239, AD241); V_{CC} = +5 V ± 5% (AD233, AD235); V+ = 7.5 V to 13.2 V (AD231) & V+ = 12 V ± 10% (AD239); All Specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
Output Voltage Swing	± 5	± 9		Volts	All Transmitter Outputs Loaded with 3 kΩ to Ground
V_{CC} Power Supply Current		4	10	mA	No Load, T_A = 25°C
		0.4	1	mA	AD231, AD239
V+ Power Supply Current		5	10	mA	No Load, V+ = 12 V AD231 & AD239 Only
Shutdown Supply Current		1	10	μA	T_A = +25°C
Input Logic Threshold Low, V_{INL}			0.8	V	T_{IN}, $\overline{EN}$, SD
Input Logic Threshold High, V_{INH}	2.0			V	T_{IN}, $\overline{EN}$, SD
Logic Pullup Current		15	200	μA	T_{IN} = 0 V
RS-232 Input Voltage Range	−30		+30	V	
RS-232 Input Threshold Low	0.8	1.2		V	V_{CC} = 5 V, T_A = +25°C
RS-232 Input Threshold High		1.7	2.4	V	V_{CC} = 5 V, T_A = +25°C
RS-232 Input Hysteresis	0.2	0.5	1.0	V	V_{CC} = 5 V
RS-232 Input Resistance	3	5	7	kΩ	V_{CC} = 5V, T_A = +25°C
TTL/CMOS Output Voltage Low, V_{OL}			0.4	V	I_{OUT} = 3.2 mA
TTL/CMOS Output Voltage High, V_{OH}	3.5			V	I_{OUT} = −1.0 mA
TTL/CMOS Output Leakage Current		0.05	±10	μA	$\overline{EN}$ = V_{CC}, 0 V ≤ R_{OUT} ≤ V_{CC}
Output Enable Time (T_{EN})		400		ns	AD235, AD236, AD239, AD241 (Figure 25. R_L = 1 kΩ, C_L = 150 pF)
Output Disable Time (T_{DIS})		250		ns	AD235, AD236, AD239, AD241 (Figure 25. R_L = 1 kΩ, C_L = 150 pF)
Propagation Delay		0.5		μs	RS-232 to TTL
Instantaneous Slew Rate[1]			30	V/μs	C_L = 10 pF, R_L = 3-7 kΩ, T_A = +25°C
Transition Region Slew Rate		3		V/μs	R_L = 3 kΩ, C_L = 2500 pF Measured from +3 V to −3 V or −3 V to +3 V
Output Resistance	300			Ω	V_{CC} = V+ = V− = 0 V, V_{OUT} = ±2 V
RS-232 Output Short Circuit Current		±10		mA	

NOTE
[1]Sample tested to ensure compliance.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*
(T_A = 25°C unless otherwise noted)

V_{CC} . . . . −0.3 V to +6 V
V+ . . . . (V_{CC} −0.3 V) to +13 V
V− . . . . +0.3 V to −13 V
Input Voltages
  T_{IN} . . . . −0.3 V to (V_{CC} +0.3 V)
  R_{IN} . . . . ±30 V
Output Voltages
  T_{OUT} . . . . (V+, +0.3 V) to (V−, −0.3 V)
  R_{OUT} . . . . −0.3 V to (V_{CC} +0.3 V)
Short Circuit Duration
  T_{OUT} . . . . Continuous

Power Dissipation
  Cerdip (Derate 9.5 mW/°C above +70°C) . . . . 675 mW
  Plastic DIP (Derate 7 mW/°C above +70°C) . . . . . 375 mW
  SOIC (Derate 7 mW/°C above +70°C) . . . . 375 mW
Operating Temperature Range
  Commercial (J Version) . . . . 0 to +70°C
  Industrial (A Version) . . . . −40°C to +85°C
  Extended (S Version) . . . . −55°C to +125°C
Storage Temperature Range . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . +300°C

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

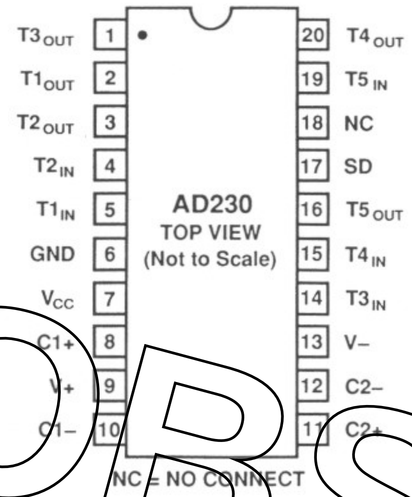
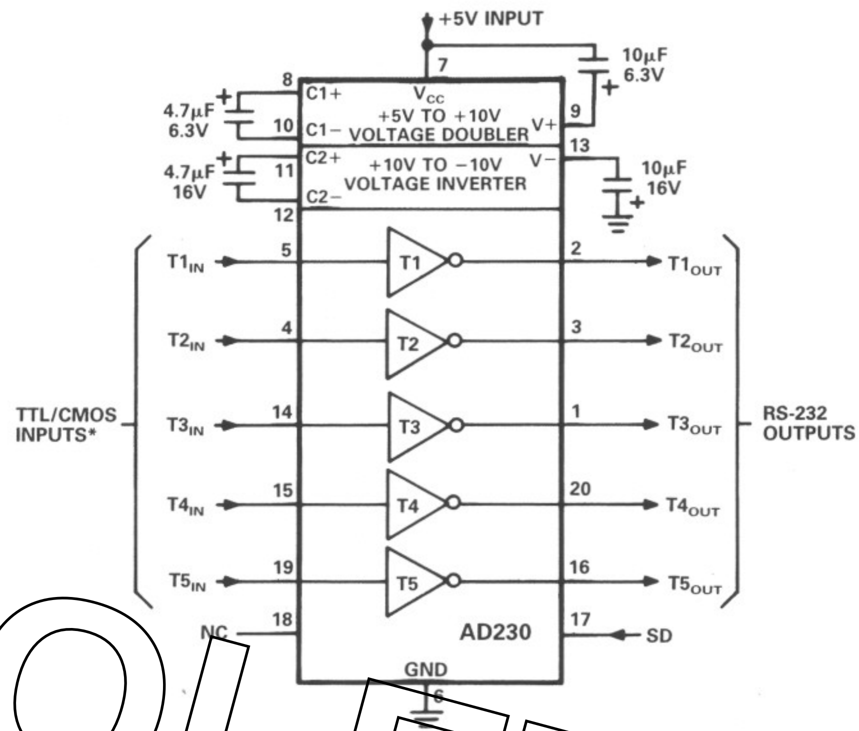


Figure 1. AD230 DIP/SOIC Pin Configuration



*INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT

Figure 2. AD230 Typical Operating Circuit

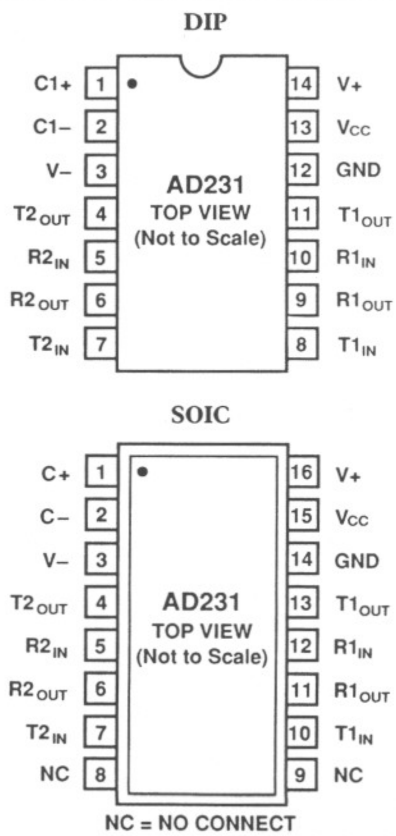
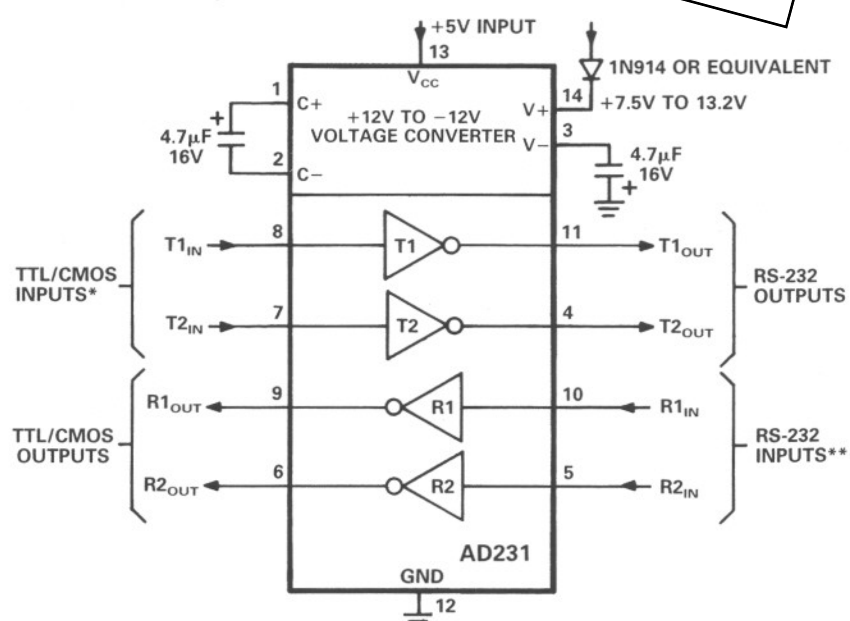


Figure 3. AD231 DIP & SOIC Pin Configurations



*INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT
**INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT

Figure 4. AD231 Typical Operating Circuit

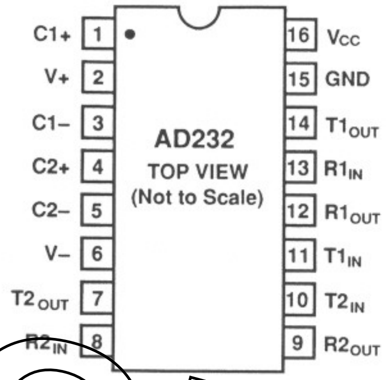
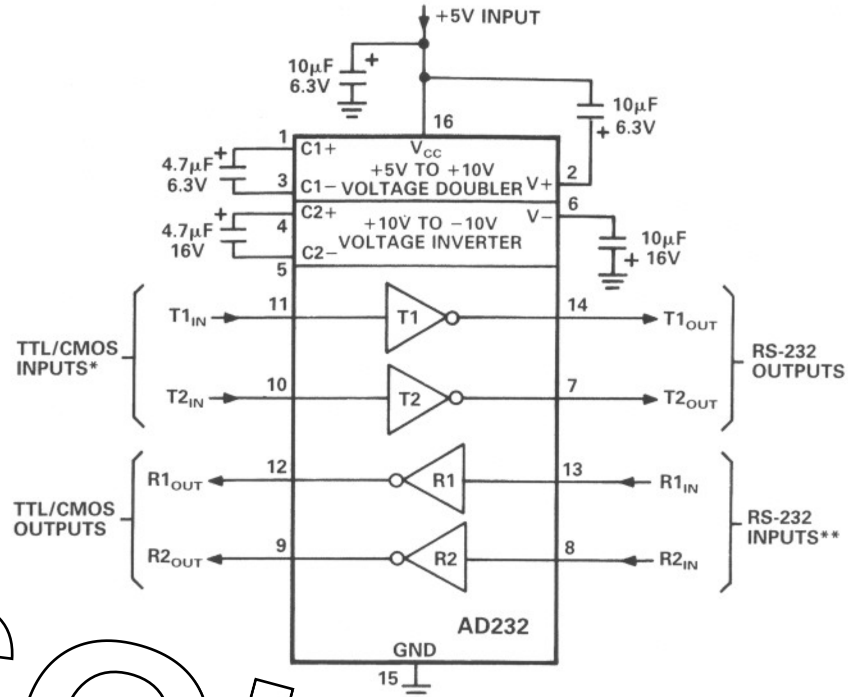


Figure 5. AD232 DIP/SOIC Pin Configuration



*INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT
**INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT

Figure 6. AD232 Typical Operating Circuit

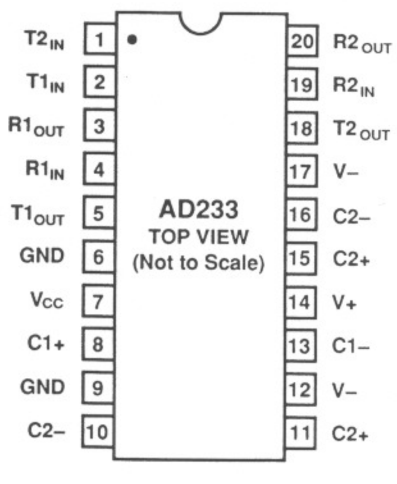
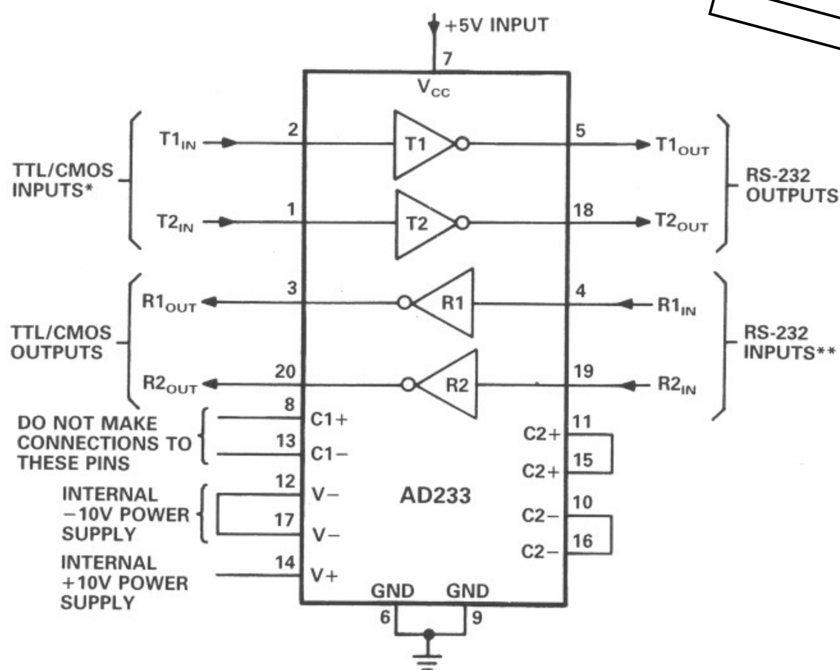


Figure 7. AD233 DIP Pin Configuration



*INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT
**INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT

Figure 8. AD233 Typical Operating Circuit

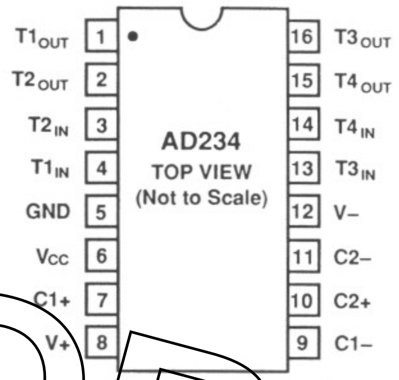
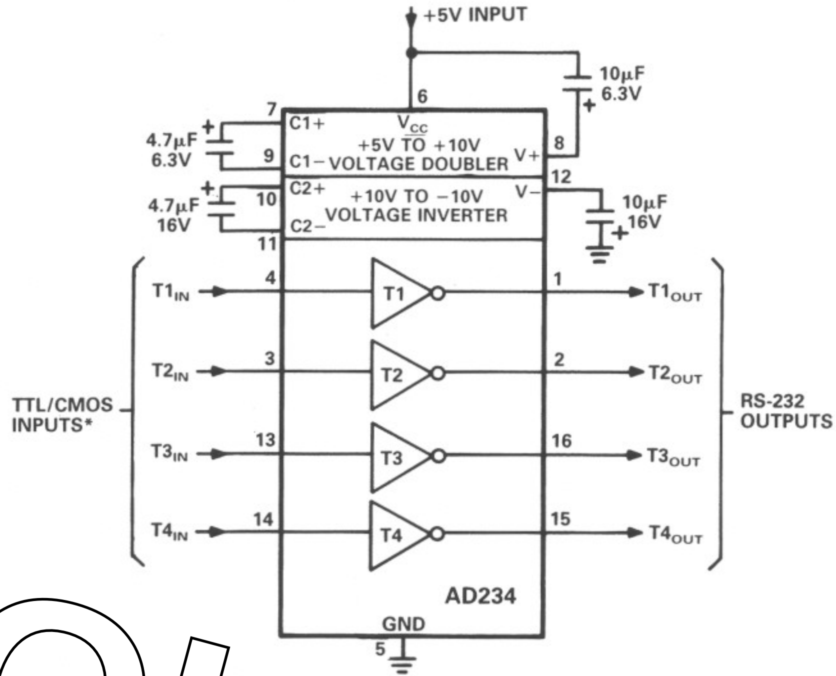


Figure 9. AD234 DIP/SOIC Pin Configuration



*INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT

Figure 10. AD234 Typical Operating Circuit

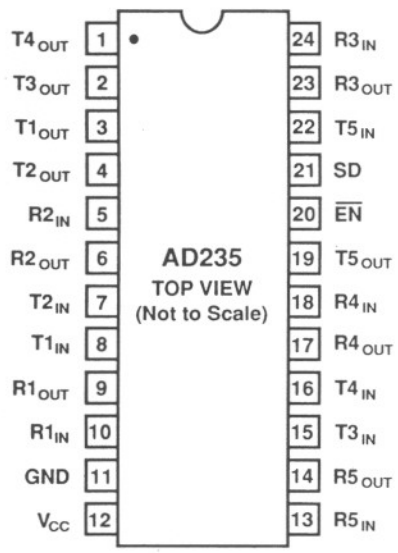
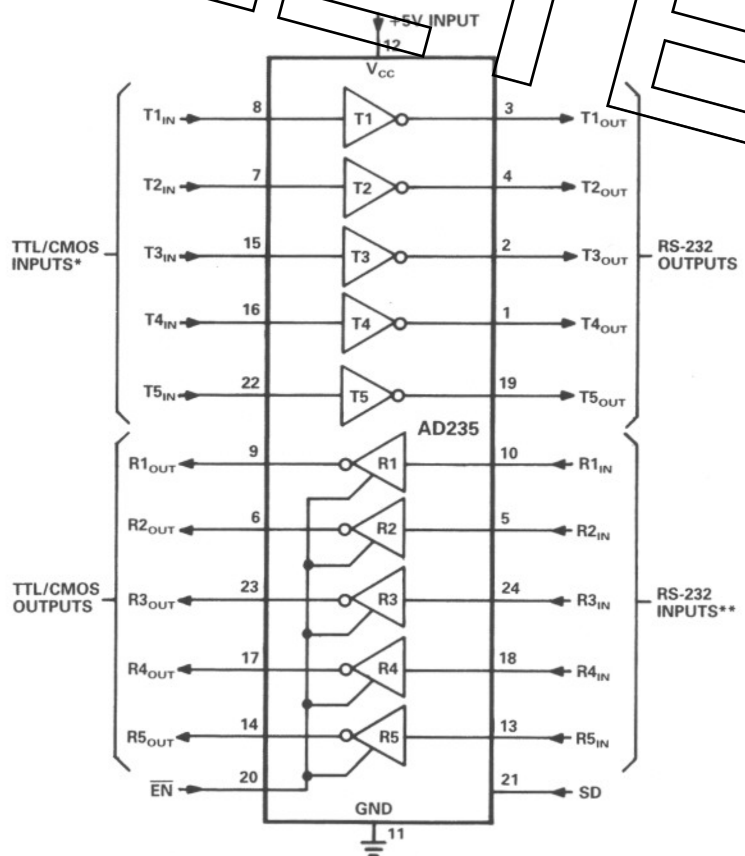


Figure 11. AD235 DIP Pin Configuration



*INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT
**INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT

Figure 12. AD235 Typical Operating Circuit

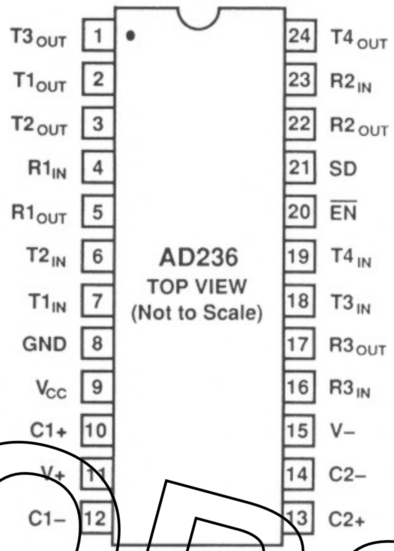
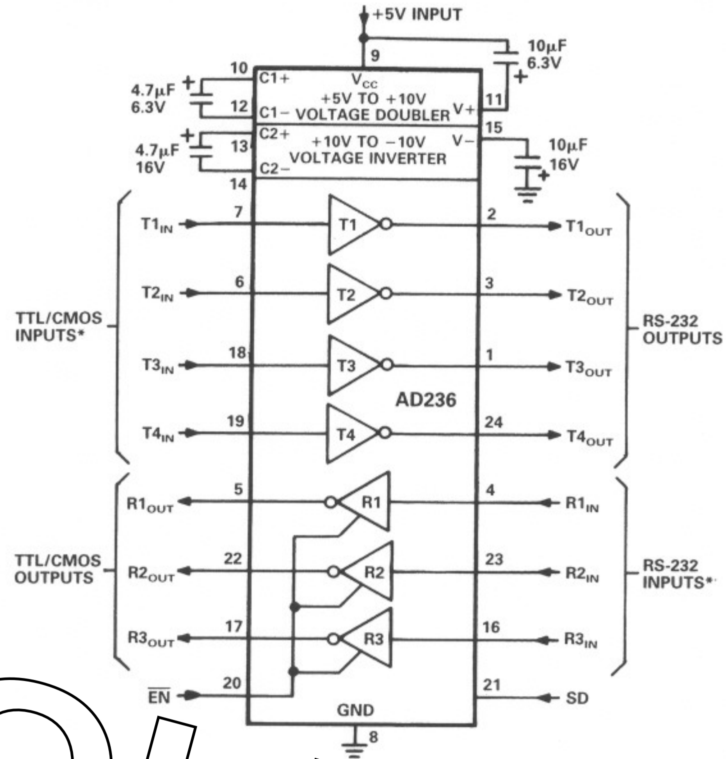


Figure 13. AD236 DIP/SOIC Pin Configuration



*INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT
**INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT

Figure 14. AD236 Typical Operating Circuit

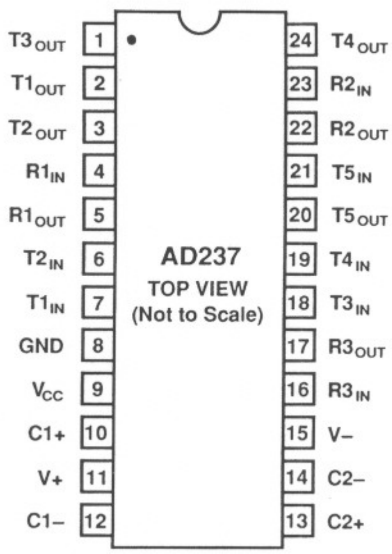
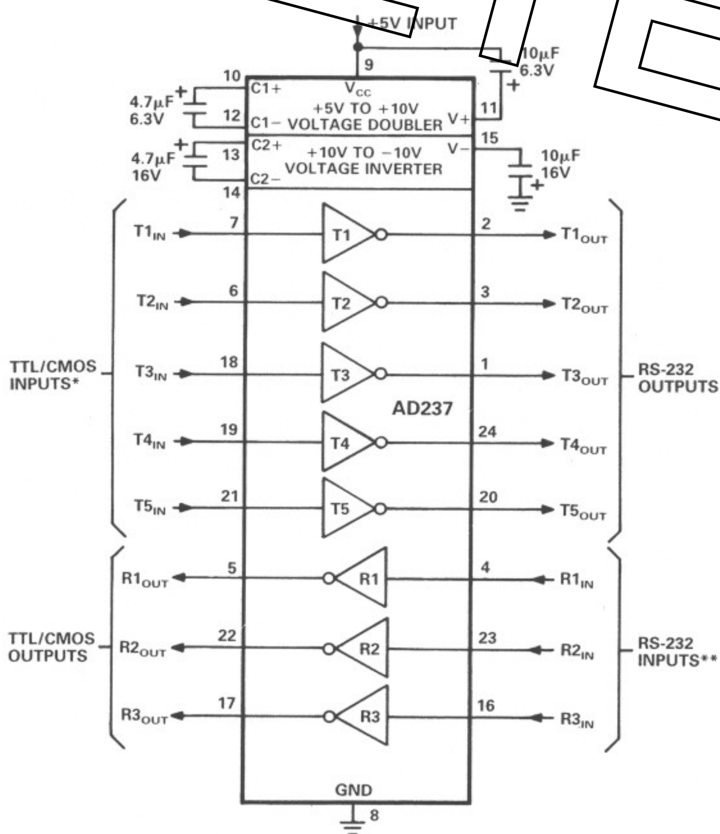


Figure 15. AD237 DIP/SOIC Pin Configuration



*INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT
**INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT

Figure 16. AD237 Typical Operating Circuit

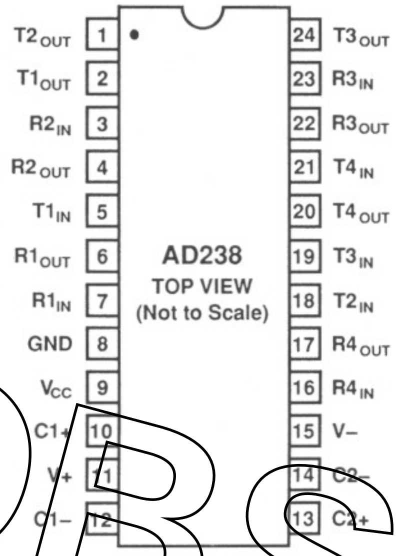
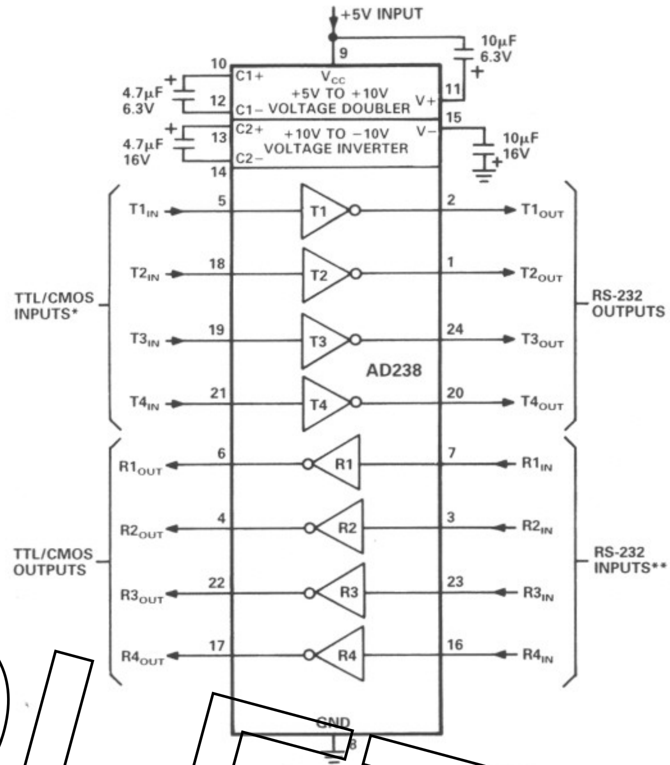


Figure 17. AD238 DIP/SOIC Pin Configuration



*INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT
**INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT

Figure 18. AD238 Typical Operating Circuit

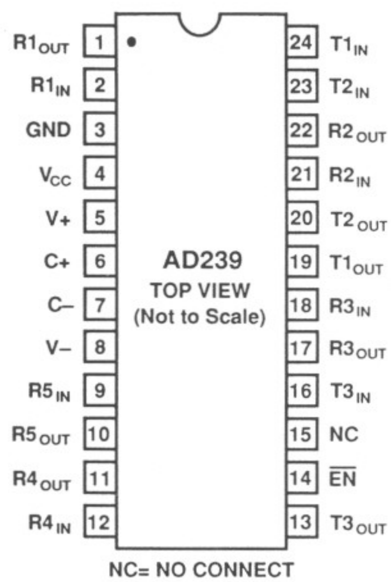
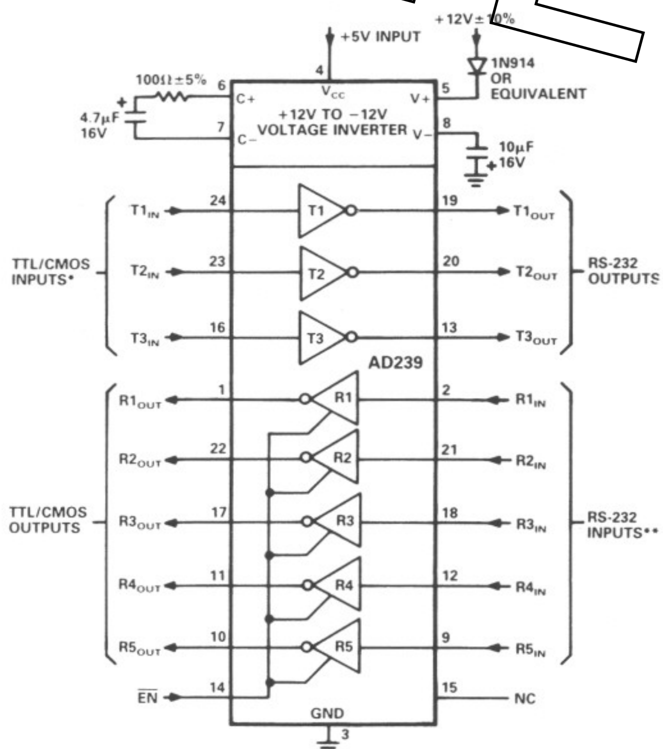


Figure 19. AD239 DIP/SOIC Pin Configuration



*INTERNAL 400kΩ PULL-UP RESISTOR ON EACH TTL/CMOS INPUT
**INTERNAL 5kΩ PULL-DOWN RESISTOR ON EACH RS-232 INPUT

Figure 20. AD239 Typical Operating Circuit

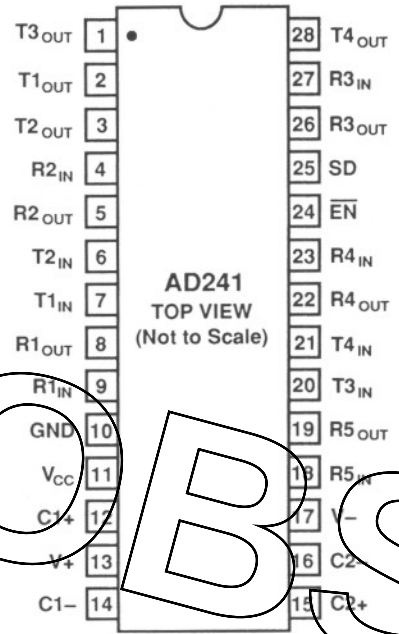


Figure 21. AD241 SOIC Pin Configuration

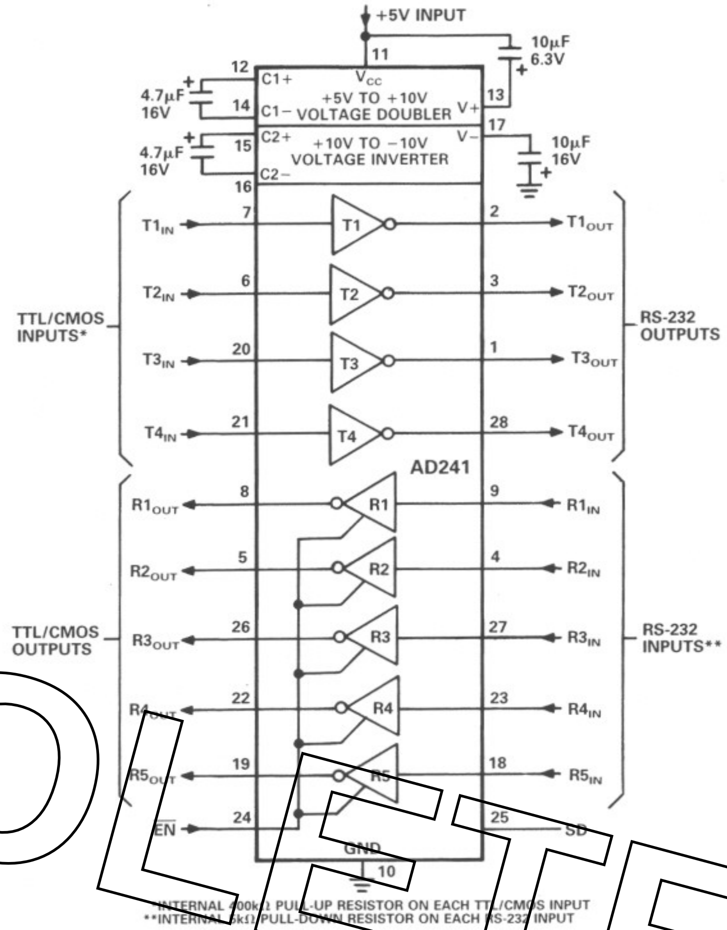


Figure 22. AD241 Typical Operating Circuit

PIN FUNCTION DESCRIPTION

Mnemonic	Function
V_{CC}	Power Supply Input 5 V ± 10% (AD231, AD232, AD234, AD236, AD238, AD239, AD241). 5 V± 5% (AD233, AD235).
V+	Internally generated positive supply (+10 V nominal) on all parts except AD231 and AD239. AD231 requires external 7.5 V to 13.2 V supply; AD239 requires external 10.8 V to 13.2 V supply.
V−	Internally generated negative supply (−10 V nominal).
GND	Ground pin. Must be connected to 0 V.
C+	(AD231 and AD239 only). External capacitor (+ terminal) is connected to this pin.
C−	(AD231 and AD239 only). External capacitor (− terminal) is connected to this pin.
C1+	(AD230, AD232, AD234, AD236, AD237, AD238, AD241) External capacitor (+ terminal) is connected to this pin. (AD233) The capacitor is connected internally and no external connection to this pin is required.
C1−	(AD230, AD232, AD234, AD236, AD237, AD238, AD241) External capacitor (− terminal) is connected to this pin. (AD233) The capacitor is connected internally and no external connection to this pin is required.
C2+	(AD230, AD232, AD234, AD236, AD237, AD238, AD241) External capacitor (+ terminal) is connected to this pin. (AD233) The capacitor is connected internally and no external connection to this pin is required.
C2−	(AD230, AD232, AD234, AD236, AD237, AD238, AD241) External capacitor (− terminal) is connected to this pin. (AD233) The capacitor is connected internally and no external connection to this pin is required.
T_{IN}	Transmitter (Driver) Inputs. These inputs accept TTL/CMOS levels. An internal 400 kΩ pull-up resistor to V_{CC} is connected on each input.
T_{OUT}	Transmitter (Driver) Outputs. These are RS-232 levels (typically ±10 V).
R_{IN}	Receiver Inputs. These inputs accept RS-232 signal levels. An internal 5 kΩ pull-down resistor to GND is connected on each input.
R_{OUT}	Receiver outputs. These are TTL/CMOS levels.
$\overline{EN}$	Enable Input (AD235, AD236, AD239, AD241). This is an active low input which is used to enable the receiver outputs. With $\overline{EN}$ = 0 V, the receiver outputs are enabled. With $\overline{EN}$ = 5 V, the outputs are placed in a high impedance state. This facility is useful for connecting to microprocessor systems.
SD	Shutdown input. (AD230, AD235, AD236, AD241). With SD = 5 V, the charge pump is disabled, the receiver outputs are placed in a high impedance state and the driver outputs are turned off. The supply current reduces to <5 μA making these parts ideally suited for battery operation.
NC	No Connect. No connections are required to this pin.

GENERAL INFORMATION

The AD230–AD241 family of RS-232 drivers/receivers are designed to solve interface problems by meeting the RS-232-C specifications while using a single digital +5 V supply. The RS-232-C standard requires transmitters which will deliver ±5 V minimum on the transmission channel and receivers which can accept signal levels down to ±3 V. The AD230–AD241 meet these requirements by integrating step up voltage converters and level shifting transmitters and receivers onto the same chip. CMOS technology is used to keep the power dissipation to an absolute minimum. A comprehensive range of transmitter/receiver combinations is available to cover most communications needs.

The AD230, AD235, AD236 and AD241 are particularly useful in battery powered systems as they feature a low power shutdown mode which reduces power dissipation to less than 5 μW.

The AD233 and AD235 are designed for applications where space saving is important as the charge pump capacitors are molded into the package.

The AD231 and AD239 include only a negative charge pump converter and are intended for applications where a positive 12 V is available.

To facilitate sharing a common line or for connection to a microprocessor data bus the AD235, AD236, AD239 and AD241 feature an enable ($\overline{EN}$) function. When disabled, the receiver outputs are placed in a high impedance state.

CIRCUIT DESCRIPTION

The internal circuitry in the AD230–AD241 consists of three main sections. These are:

(a) A charge pump voltage converter
(b) RS-232 to TTL/CMOS receivers
(c) TTL/CMOS to RS-232 transmitters

Charge Pump DC-DC Voltage Converter

The charge pump voltage converter consists of an oscillator and a switching matrix. The converter generates a ±10 V supply from the input 5 V level. This is done in two stages using a switched capacitor technique as illustrated in Figures 23 and 24. First, the 5 V input supply is doubled to 10 V using capacitor C1 as the charge storage element. The 10 V level is then inverted to generate −10 V using C2 as the storage element.

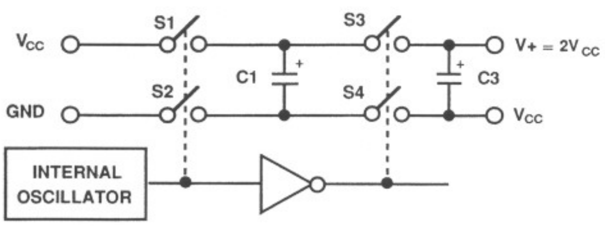


Figure 23. Charge-Pump Voltage Doubler

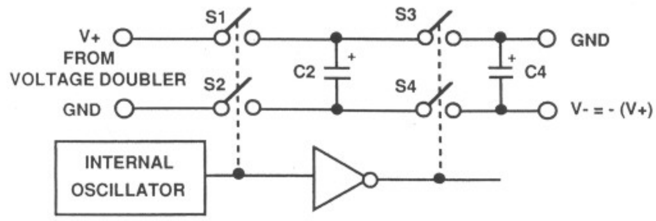


Figure 24. Charge-Pump Voltage Inverter

Capacitors C3 and C4 are used to reduce the output ripple. Their values are not critical and can be reduced if higher levels of ripple are acceptable. The charge pump capacitors C1 and C2 may also be reduced at the expense of higher output impedance on the V+ and V− supplies.

The V+ and V− supplies may also be used to power external circuitry if the current requirements are small.

Transmitter (Driver) Section

The drivers convert TTL/CMOS input levels into RS-232-C output levels. With V_{CC} = +5 V and driving a typical RS-232-C load, the output voltage swing is ±9 V. Even under worst case conditions the drivers are guaranteed to meet the ±5 V RS-232-C minimum requirement.

The input threshold levels are both TTL and CMOS compatible with the switching threshold set at $V_{CC}/4$. With a nominal V_{CC} = 5 V the switching threshold is 1.25 V typical. Unused inputs may be left unconnected, as an internal 400 kΩ pull-up resistor pulls them high forcing the outputs into a low state.

As required by the RS-232-C standard, the slew rate is limited to less than 30 V/μs without the need for an external slew limiting capacitor and the output impedance in the power-off state is greater than 300 Ω.

Receiver Section

The receivers are inverting level shifters which accept RS-232-C input levels (±5 V to ±15 V) and translate them into 5 V TTL/CMOS levels. The inputs have internal 5 kΩ pull-down resistors to ground and are also protected against overvoltages of up to ±30 V. The guaranteed switching thresholds are 0.8 V minimum and 2.4 V maximum which are well within the ±3 V RS-232 requirement. The low level threshold is deliberately positive as it ensures that an unconnected input will be interpreted as a low level.

The receivers have Schmitt trigger inputs with a hysteresis level of 0.5 V. This ensures error-free reception for both noisy inputs and for inputs with slow transition times.

Shutdown (SD)

The AD230, AD235, AD236 and AD241 feature a control input which may be used to disable the part and reduce the power consumption to less than 5 μW. This is very useful in battery operated systems. With SD = 5 V, the charge pump is disabled, the receiver outputs are placed in a high impedance state and the driver outputs are turned off.

Enable Input

The AD235, AD236, AD239 and AD241 feature an enable input ($\overline{EN}$). It is used to enable the receiver outputs. With $\overline{EN}$ = 0 V the outputs are enabled. With $\overline{EN}$ = 5 V the outputs are placed in a high impedance state. This function allows the outputs to be connected directly to a microprocessor data bus. It can also be used to allow receivers from different devices to share a common data line. The timing diagram for the enable function is shown in Figure 25.

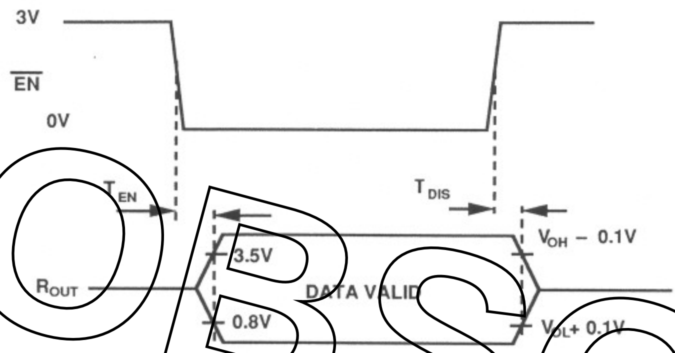


Figure 25. Enable Timing

APPLICATION HINTS

Protection for Shorts to ±15 V Supplies

The driver outputs are internally protected against shorting to ground, to other driver outputs, to V+ or to V−. In practice, these are the highest voltages likely to be encountered in an application. If the possibility exists for shorting to ±15 V, then it is recommended that external protection be provided. This may be done by connecting a series 220 Ω resistor on each transmitter output.

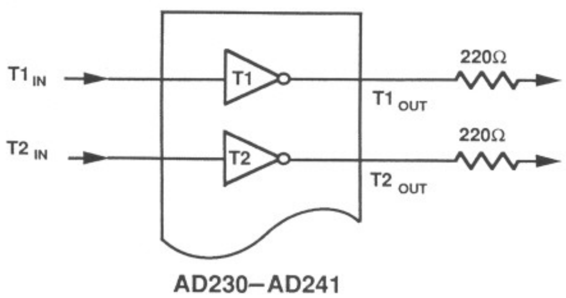


Figure 26. Protection for Shorts to ±15 V

Over-Voltage Protection for AD231, AD239

The AD231 and AD239 require an external +12 V supply as they do not contain an internal V+ generator. It is important that this supply be switched on before the 5 V, V_{CC} supply.

If there is a possibility that the V_{CC} supply will be switched on first, or if the 12 V supply may be inadvertently shorted to ground, then it is recommended that a diode (1N914 or equivalent) be connected in series with the 12 V input. This will not affect normal operation but it ensures that under fault conditions, the device will be protected.

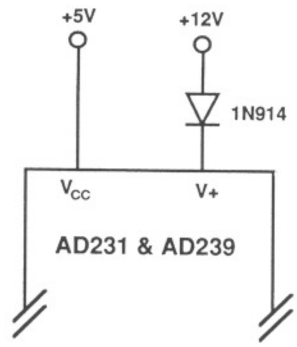


Figure 27. Diode Protection Scheme for AD231 and AD239

High Baud Rate Operation

The RS-232-C standard requires that *"For Data and Timing interchange Circuits, the time for the signal to pass through the transition region shall not exceed one millisecond or four percent of the nominal duration of the signal element on that interchange circuit, whichever is the lesser."* With the maximum transmission rate of 19.2 kbaud, this translates into a minimum slew rate of 3 V/μs. The typical slew rate of the AD230–AD241 is 3 V/μs under maximum loading conditions and therefore meets the standard.

The V.28 standard is more stringent and requires a transition time which will not exceed three percent of the nominal signal duration. This translates into a slew rate of 4 V/μs at the maximum 19.2 kbaud rate. In practice, less than ideal slew rates will have negligible affect on the data transmission. The result is that the valid mark/space duration is slightly shorter than the optimum because the signal spends more time in the transition region. The valid duration remains more than adequate for error-free reception even at maximum transmission rates and under worst case load conditions.

Driving Long Cables

In accordance with the RS-232-C standard, long cables are permissible provided that the total load capacitance does not exceed 2500 pF. For longer cables which do exceed this, then it is possible to trade off baud rate vs. cable length. Large load capacitances cause a reduction in slew rate, and hence the maximum transmission baud rate is decreased. The AD230–AD241 are designed so that the slew rate reduction with increasing load capacitance is minimized.

For the receivers, it is important that a high level of noise immunity be inbuilt so that slow rise and fall times do not cause multiple output transitions as the signal passes slowly through the transition region. The AD230–AD241 have 0.5 V of hysteresis to guard against this. This ensures that, even in noisy environments, error-free reception can be achieved.

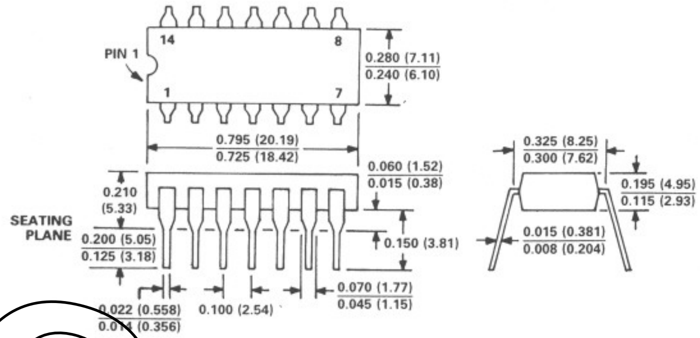
ORDERING INFORMATION

Part	Temperature Range	Package	Part	Temperature Range	Package	Part	Temperature Range	Package
AD230			**AD231**			**AD232**		
AD230JN	0 to +70°C	20-Lead Plastic DIP	AD231JN	0 to +70°C	14-Lead Plastic DIP	AD232JN	0 to +70°C	16-Lead Plastic DIP
AD230JR	0 to +70°C	20-Lead SOIC	AD231JR	0 to +70°C	16-Lead SOIC	AD232JR	0 to +70°C	16-Lead SOIC
AD230AN	−40°C to +85°C	20-Lead Plastic DIP	AD231AN	−40°C to +85°C	14-Lead Plastic DIP	AD232AN	−40°C to +85°C	16-Lead Plastic DIP
AD230AR	−40°C to +85°C	20-Lead SOIC	AD231AR	−40°C to +85°C	16-Lead SOIC	AD232AR	−40°C to +85°C	16-Lead SOIC
AD230AQ	−40°C to +85°C	20-Lead Cerdip	AD231AQ	−40°C to +85°C	14-Lead Cerdip	AD232AQ	−40°C to +85°C	16-Lead Cerdip
			AD231SQ	−55°C to +125°C	14-Lead Cerdip	AD232SQ	−55°C to +125°C	16-Lead Cerdip
AD233			**AD234**			**AD235**		
AD233JN	0 to +70°C	20-Lead Plastic DIP	AD234JN	0 to +70°C	16-Lead Plastic DIP	AD235JN	0 to +70°C	24-Lead Plastic DIP*
AD233AN	−40°C to +85°C	20-Lead Plastic DIP	AD234JR	0 to +70°C	16-Lead SOIC	AD235AN	−40°C to +85°C	24-Lead Plastic DIP*
			AD234AN	−40°C to +85°C	16-Lead Plastic DIP	AD235AQ	−40°C to +85°C	24-Lead Ceramic*
			AD234AR	−40°C to +85°C	16-Lead SOIC			
			AD234AQ	−40°C to +85°C	16-Lead Cerdip			
			AD234SQ	−55°C to +125°C	16-Lead Cerdip			
AD236			**AD237**			**AD238**		
AD236JN	0 to +70°C	24-Lead Plastic DIP	AD237JN	0 to +70°C	24-Lead Plastic DIP	AD238JN	0 to +70°C	24-Lead Plastic DIP
AD236JR	0 to +70°C	24-Lead SOIC	AD237JR	0 to +70°C	24-Lead SOIC	AD238JR	0 to +70°C	24-Lead SOIC
AD236AN	−40°C to +85°C	24-Lead Plastic DIP	AD237AN	−40°C to +85°C	24-Lead Plastic DIP	AD238AN	−40°C to +85°C	24-Lead Plastic DIP
AD236AR	−40°C to +85°C	24-Lead SOIC	AD237AR	−40°C to +85°C	24-Lead SOIC	AD238AR	−40°C to +85°C	24-Lead SOIC
AD236AQ	−40°C to +85°C	24-Lead Cerdip	AD237AQ	−40°C to +85°C	24-Lead Cerdip	AD238AQ	−40°C to +85°C	24-Lead Cerdip
AD236SQ	−55°C to +125°C	24-Lead Cerdip				AD238SQ	−55°C to +125°C	24-Lead Cerdip
AD239			**AD241**					
AD239JN	0 to +70°C	24-Lead Plastic DIP	AD241JR	0 to +70°C	28-Lead SOIC			
AD239JR	0 to +70°C	24-Lead SOIC	AD241AR	−40°C to +85°C	28-Lead SOIC			
AD239AN	−40°C to +85°C	24-Lead Plastic DIP						
AD239AR	−40°C to +85°C	24-Lead SOIC						
AD239AQ	−40°C to +85°C	24-Lead Cerdip						
AD239SQ	−55°C to +125°C	24-Lead Cerdip						

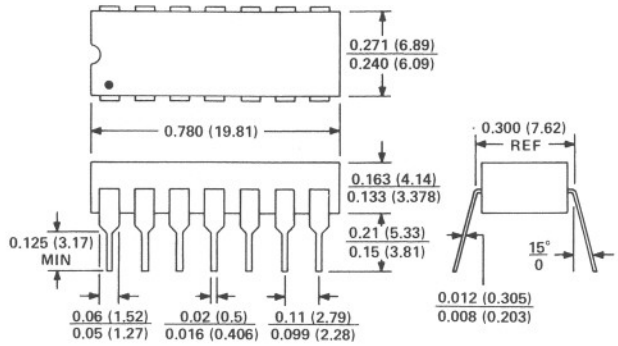
*= 0.6″ DIP package (all other DIP packages = 0.3″)

OUTLINE DIMENSIONS

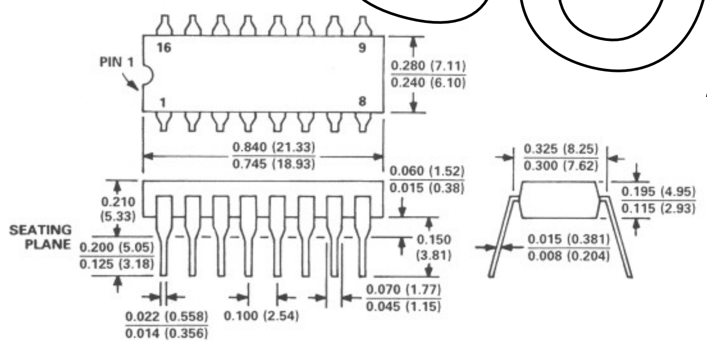
14-Lead Plastic DIP (N-14)



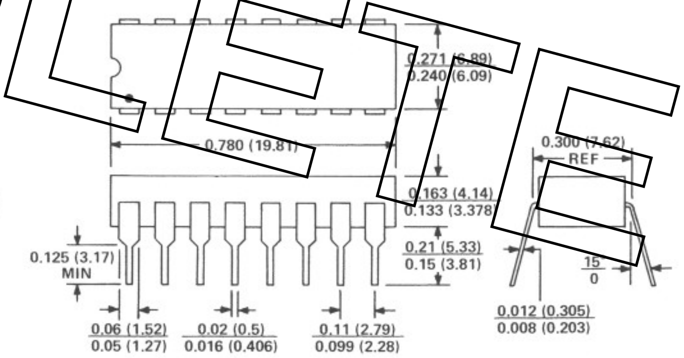
14-Lead Cerdip (Q-14)



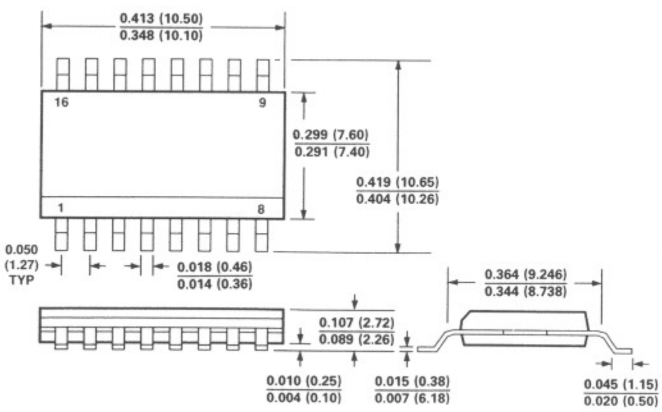
16-Lead Plastic DIP (N-16)



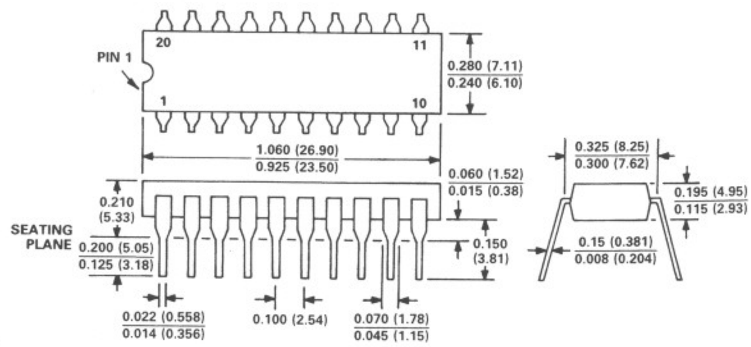
16-Lead Cerdip (Q-16)



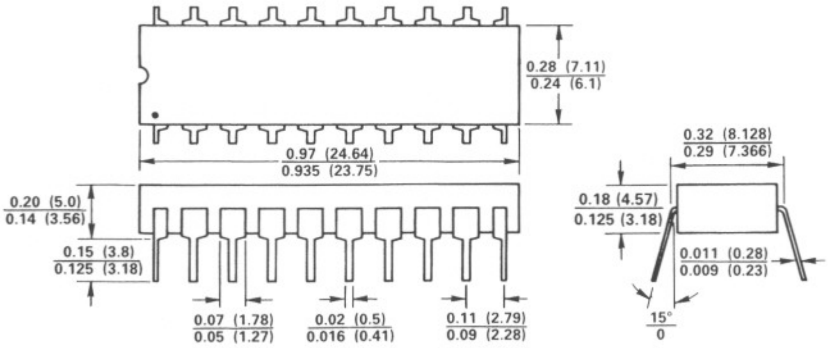
16-Lead SOIC (R-16)



20-Lead Plastic DIP (N-20)

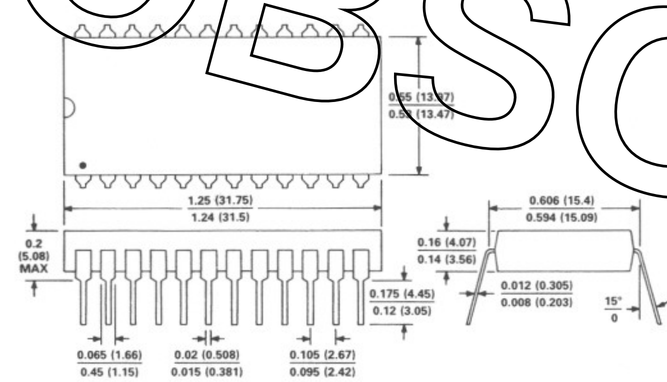


20-Lead Cerdip (Q-20)

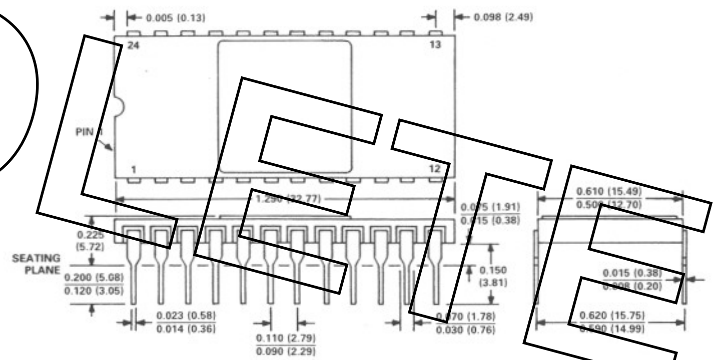


LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42

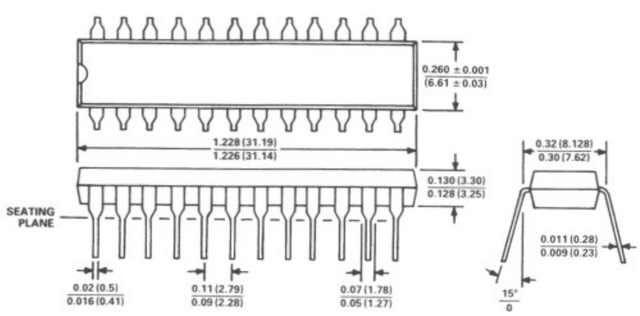
24-Lead Plastic DIP (N-24A)



24-Lead Ceramic DIP (D-24)

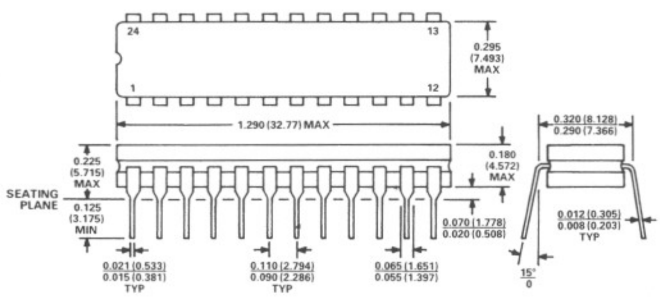


24-Lead Plastic DIP (N-24)



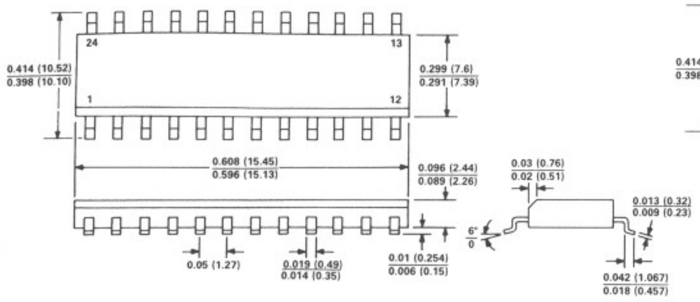
NOTES
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. PLASTIC LEADS WILL BE EITHER SOLDER DIPPED OR TIN LEAD PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

24-Lead Cerdip (Q-24)



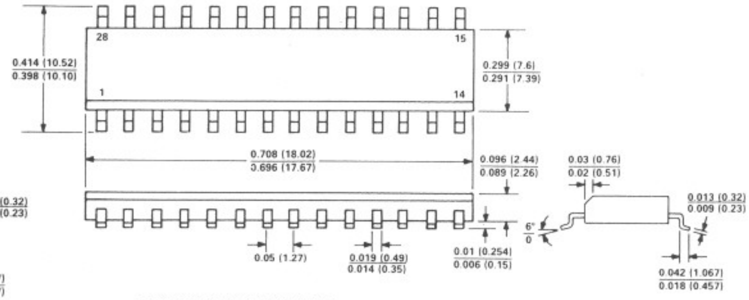
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. CERDIP LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

24-Lead SOIC (R-24)



1. LEAD NO. 1 IDENTIFIED BY A DOT.
2. SOIC LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

28-Lead SOIC (R-28)



1. LEAD NO. 1 IDENTIFIED BY A DOT.
2. SOIC LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.