ANALOG DEVICES

Ultralow Noise, High Speed, BiFET Op Amp

AD745

FEATURES
ULTRALOW NOISE PERFORMANCE
2.9 nV/√Hz at 10 kHz
0.38 μV p–p, 0.1 Hz to 10 Hz
6.9 fA/√Hz Current Noise at 1 kHz

EXCELLENT AC PERFORMANCE
12.5 V/μs Slew Rate
20 MHz Gain Bandwidth Product
THD = 0.0002% @ 1 kHz
Internally Compensated for Gains of +5 (or −4) or Greater

EXCELLENT DC PERFORMANCE
0.5 mV max Offset Voltage
250 pA max Input Bias Current
2000 V/mV min Open Loop Gain
Available in Tape and Reel in Accordance with EIA-481A Standard

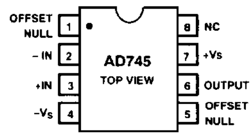
APPLICATIONS
Sonar
Photodiode and IR Detector Amplifiers
Accelerometers
Low Noise Preamplifiers
High Performance Audio

PRODUCT DESCRIPTION

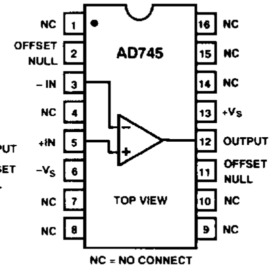
The AD745 is an ultralow noise, high speed, FET input operational amplifier. It offers both the ultralow voltage noise and high speed generally associated with bipolar input op amps and the very low input currents of FET input devices. Its 20 MHz bandwidth and 12.5 V/μs slew rate makes the AD745 an ideal amplifier for high speed applications demanding low noise and high dc precision. Furthermore, the AD745 does not exhibit an output phase reversal.

CONNECTION DIAGRAMS

8-Pin Plastic Mini-DIP (N) & 8-Pin Cerdip (Q) Packages



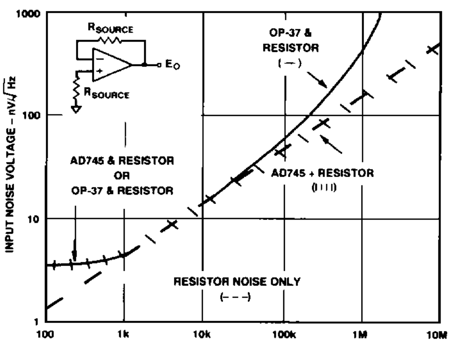
16-Pin SOIC (R) Package

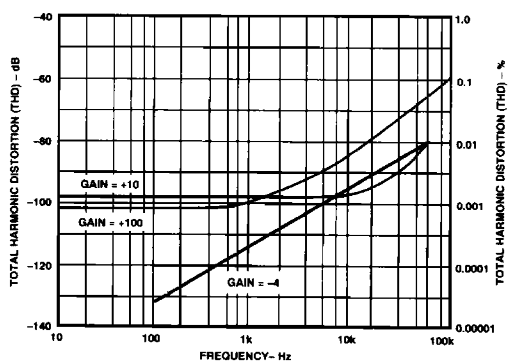


The AD745's guaranteed, tested maximum input voltage noise of 4 nV/√Hz at 10 kHz is unsurpassed for a FET-input monolithic op amp, as is its maximum 1.0 μV p–p noise in a 0.1 to 10 Hz bandwidth. The AD745 also has excellent dc performance with 250 pA maximum input bias current and 0.5 mV maximum offset voltage.

The internal compensation of the AD745 is optimized for higher gains, providing a much higher bandwidth and a faster slew rate. This makes the AD745 especially useful as a preamplifier where low level signals require an amplifier that provides both high amplification and wide bandwidth at these higher gains. The AD745 is available in five performance grades. The AD745J and AD745K are rated over the commercial temperature range of 0°C to +70°C. The AD745A and AD745B are rated over the industrial temperature range of −40°C to +85°C. The AD745S is rated over the military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev. C.

The AD745 is available in 8-pin plastic mini-DIP, 8-pin cerdip, 16-pin SOIC, or in chip form.





This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD745J/A Min	Typ	Max	AD745K/B Min	Typ	Max	AD745S Min	Typ	Max	Units
INPUT OFFSET VOLTAGE[1]											
Initial Offset			0.25	1.0/0.8		0.1	0.5/0.25		0.25	1.0	mV
Initial Offset	T_{min} to T_{max}			1.5			1.0/0.50			2.0	mV
vs. Temp.	T_{min} to T_{max}		2			2			2		μV/°C
vs. Supply (PSRR)	12 V to 18 V[2]	90	96		100	106		90	96		dB
vs. Supply (PSRR)	T_{min} to T_{max}	88			98	105		88			dB
INPUT BIAS CURRENT[3]											
Either Input	$V_{CM} = 0$ V		150	400		150	250		150	400	pA
Either Input @ T_{max}	$V_{CM} = 0$ V			8.8/25.6			5.5/16			413	nA
Either Input	$V_{CM} = +10$ V		250	600		250	400		300	600	pA
Either Input, $V_S = \pm 5$ V	$V_{CM} = 0$ V		30	200		30	125		30	200	pA
INPUT OFFSET CURRENT	$V_{CM} = 0$ V		40	150		30	75		40	150	pA
Offset Current @ T_{max}	$V_{CM} = 0$ V			2.2/6.4			1.1/3.2			102	nA
FREQUENCY RESPONSE											
Gain BW, Small Signal	$G = -4$		20			20			20		MHz
Full Power Response	$V_O = 20$ V p-p		120			120			120		kHz
Slew Rate	$G = -4$		12.5			12.5			12.5		V/μs
Settling Time to 0.01%			5			5			5		μs
Total Harmonic Distortion[4]	f = 1 kHz, $G = -4$		0.0002			0.0002			0.0002		%
INPUT IMPEDANCE											
Differential			$1 \times 10^{10} \parallel 20$			$1 \times 10^{10} \parallel 20$			$1 \times 10^{10} \parallel 20$		Ω‖pF
Common Mode			$3 \times 10^{11} \parallel 18$			$3 \times 10^{11} \parallel 18$			$3 \times 10^{11} \parallel 18$		Ω‖pF
INPUT VOLTAGE RANGE											
Differential[5]			±20			±20			±20		V
Common-Mode Voltage			+13.3, −10.7			+13.3, −10.7			+13.3, −10.7		V
Over Max Operating Range[6]		−10		+12	−10		+12	−10		+12	V
Common-Mode Rejection Ratio	$V_{CM} = \pm 10$ V	80	95		90	102		80	95		dB
	T_{min} to T_{max}	78			88			78			dB
INPUT VOLTAGE NOISE	0.1 to 10 Hz		0.38			0.38	1.0		0.38		μV p-p
	f = 10 Hz		5.5			5.5	10.0		5.5		nV/√Hz
	f = 100 Hz		3.6			3.6	6.0		3.6		nV/√Hz
	f = 1 kHz		3.2	5.0		3.2	5.0		3.2	5.0	nV/√Hz
	f = 10 kHz		2.9	4.0		2.9	4.0		2.9	4.0	nV/√Hz
INPUT CURRENT NOISE	f = 1 kHz		6.9			6.9			6.9		fA/√Hz
OPEN LOOP GAIN	$V_O = \pm 10$ V										
	$R_{LOAD} \geq 2$ kΩ	1000	4000		2000	4000		1000	4000		V/mV
	T_{min} to T_{max}	800			1800			800			V/mV
	$R_{LOAD} = 600$ Ω		1200			1200			1200		V/mV
OUTPUT CHARACTERISTICS											
Voltage	$R_{LOAD} \geq 600$ Ω	+13, −12			+13, −12			+13, −12			V
	$R_{LOAD} \geq 600$ Ω		+13.6, −12.6			+13.6, −12.6			+13.6, −12.6		V
	T_{min} to T_{max}	+12, −10			+12, −10			+12, −10			V
	$R_{LOAD} \geq 2$ kΩ	±12	+13.8, −13.1		±12	+13.8, −13.1		±12	+13.8, −13.1		V
Current	Short Circuit	20	40		20	40		20	40		mA
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		±4.8		±18	±4.8		±18	±4.8		±18	V
Quiescent Current			8	10.0		8	10.0		8	10.0	mA
TRANSISTOR COUNT	# of Transistors		50			50			50		

NOTES
[1]Input offset voltage specifications are guaranteed after 5 minutes of operation at $T_A = +25°C$.
[2]Test conditions: $+V_S = 15$ V, $-V_S = 12$ V to 18 V and $+V_S = 12$ V to +18 V, $-V_S = 15$ V.
[3]Bias current specifications are guaranteed maximum at either input after 5 minutes of operation at $T_A = +25°C$. For higher temperature, the current doubles every 10°C.
[4]Gain = −4, $R_L = 2$ kΩ, $C_L = 10$ pF.
[5]Defined as voltage between inputs, such that neither exceeds ±10 V from common.
[6]The AD745 does not exhibit an output phase reversal when the negative common-mode limit is exceeded.

All min and max specifications are guaranteed.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . ± 18 V
Internal Power Dissipation[2]
  Plastic Package . . . . 1.3 W
  Cerdip Package . . . . 1.1 W
  SOIC Package . . . . 1.2 W
Input Voltage . . . . $\pm V_S$
Output Short Circuit Duration . . . . Indefinite
Differential Input Voltage . . . . $+V_S$ and $-V_S$
Storage Temperature Range (Q) . . . . $-65°C$ to $+150°C$
Storage Temperature Range (N, R) . . . . $-65°C$ to $+125°C$
Operating Temperature Range
  AD745J/K . . . . 0°C to +70°C
  AD745A/B . . . . $-40°C$ to $+85°C$
  AD745S . . . . $-55°C$ to $+125°C$
Lead Temperature Range (Soldering 60 seconds) . . . . . . 300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

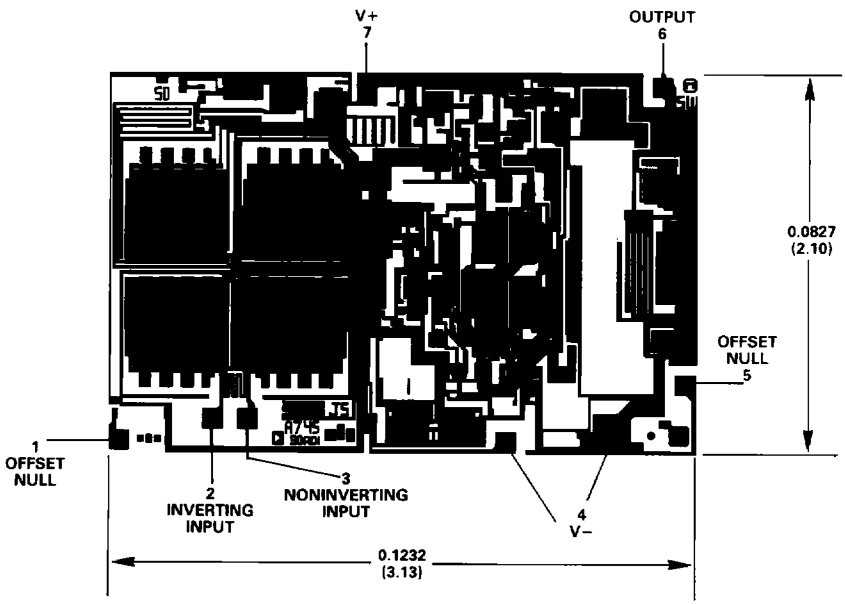
[2]8-pin plastic package: θ_{JA} = 100°C/Watt, θ_{JC} = 50°C/Watt
8-pin cerdip package: θ_{JA} = 110°C/Watt, θ_{JC} = 30°C/Watt
16-pin plastic SOIC package: θ_{JA} = 100°C/Watt, θ_{JC} = 30°C/Watt

ESD SUSCEPTIBILITY

An ESD classification per method 3015.6 of MIL STD 883C has been performed on the AD745, which is a class 1 device. Using an IMCS 5000 automated ESD tester, the two null pins will pass at voltages up to 1000 volts, while all other pins will pass at voltages exceeding 2500 volts.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



ORDERING GUIDE

Model	Temperature Range	Package Options*
AD745JN	0°C to +70°C	N-8
AD745KN	0°C to +70°C	N-8
AD745AN	−40°C to +85°C	N-8
AD745JR-16	0°C to +70°C	R-16
AD745AR-16	−40°C to +85°C	R-16
AD745AQ	−40°C to +85°C	Q-8
AD745BQ	−40°C to +85°C	Q-8
AD745SQ	−55°C to +125°C	Q-8
AD745SQ/883B	−55°C to +125°C	Q-8
AD745J Chips	0°C to +70°C	

*N = Plastic DIP; R = Small Outline IC; Q = Cerdip. For outline information see Package Information section.