General Description:

The LWS6T7AM uses SGT technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications. The package form is SOT23, which accords with the ROHS standard and Halogen Free standard.

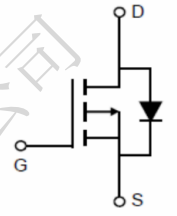
V_{DSS}	-60	V
I_D	-2.5	A
P_D	1.5	W
$R_{DS(ON)\ TYPE}$	90	mΩ

Marking and Pin Assignment

Features:

- Fast Switching
- Low Gate Charge and $R_{DS(ON)}$
- Low Reverse transfer capacitances

Inner Equivalent Principium Chart



Applications:

- DC-DC Converter
- Portable Equipment
- Power Management

Package Marking and Ordering Information:

Marking	Part Number	Package	Packing	Qty.
S6T7A	LWS6T7AM	SOT23	Reel	3000 Pcs

Absolute Maximum Ratings:

Symbol	Parameter		Value	Units
V_{DSS}	Drain-to-Source Voltage		-60	V
I_D	Continuous Drain Current	T_C=25℃	-2.5	A
	Continuous Drain Current	T_C=100℃	-1.6	A
I_{DM}[a1]	Pulsed Drain Current		-10	A
V_{GS}	Gate-to-Source Voltage		±20	V
P_D	Power Dissipation		1.5	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range		150, -55 to 150	℃
T_L	Maximum Temperature for Soldering		260	℃

Thermal Characteristics:

Symbol	Parameter	Value	Units
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	80	℃/W

Electrical Characteristic (T_A = 25 °C, unless otherwise specified)**:**

Static Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA	-60	--	--	V
I_{DSS}	Drain to Source Leakage Current	V_{DS}=-60V, V_{GS}=0V	--	--	1.0	μA
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS}=-20V, V_{DS}=0V	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS}=+20V, V_{DS}=0V	--	--	-100	nA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250μA	-1.2	-1.6	-2.0	V
$R_{DS(ON)1}$	Drain-to-Source On-Resistance	V_{GS}=-10V, I_D=-3.0A	--	90	110	mΩ
$R_{DS(ON)2}$	Drain-to-Source On-Resistance	V_{GS}=-4.5V, I_D=-2.0A	--	110	150	mΩ

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
C_{iss}	Input Capacitance	V_{GS} = 0V V_{DS} =-30V f = 1.0MHz	--	315	--	pF
C_{oss}	Output Capacitance		--	58.6	--	
C_{rss}	Reverse Transfer Capacitance		--	2.98	--	

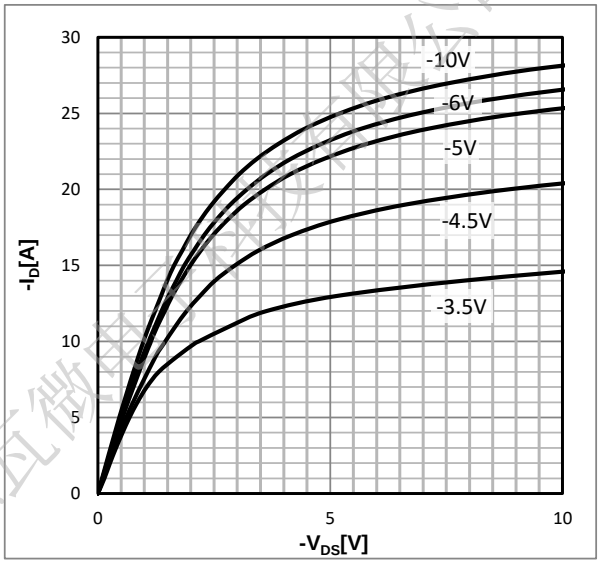
Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	I_D =-2.0A V_{DS} =-30V V_{GS} =-10V R_G =5.0Ω	--	6.8	--	ns
t_r	Rise Time		--	8	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	16	--	
t_f	Fall Time		--	4	--	
Q_g	Total Gate Charge	V_{GS} =-10V V_{DS} = -50V I_D =-5.0A	--	6.03	--	nC
Q_{gs}	Gate Source Charge		--	0.97	--	
Q_{gd}	Gate Drain Charge		--	0.72	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
I_S	Diode Forward Current	T_C =25 °C	--	--	-2.5	A
V_{SD}	Diode Forward Voltage	I_S=-2.0A, V_{GS}=0V	--	--	-1.2	V

a1：Repetitive rating; pulse width limited by maximum junction temperature

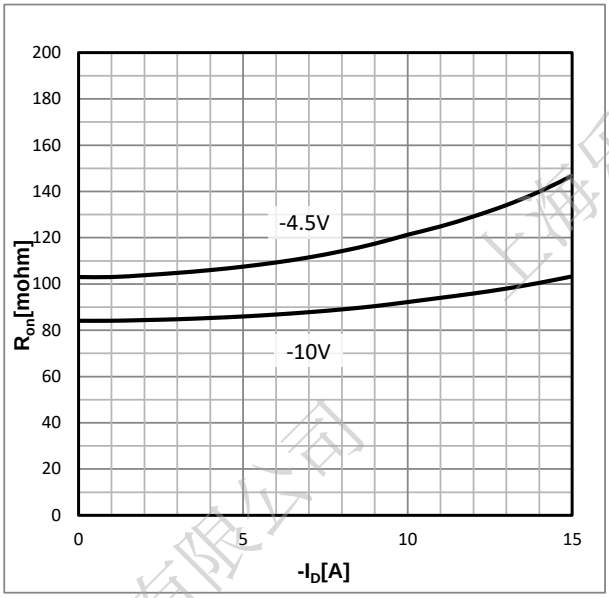
Characteristics Curve：

Figure 1: Typ. output characteristics



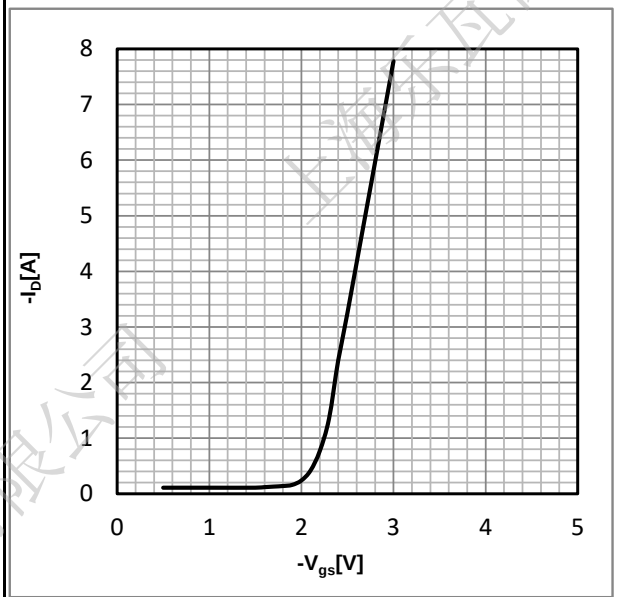
$I_D=f(V_{DS})$, T_j=25 °C; parameter: V_{GS}

Figure 2: Typ. drain-source on resistance



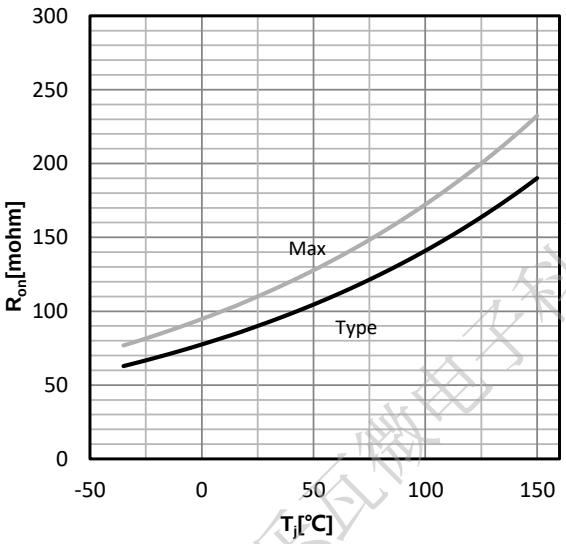
$R_{DS(on)}=f(I_D)$, T_j=25 °C; parameter: V_{GS}

Figure 3: Typ. transfer characteristics



$I_D=f(V_{GS})$, $|V_{DS}|>2|I_D|R_{DS}(on)max$;

Figure 4: drain-source on resistance



$R_{DS(on)}=f(T_j)$, I_D=-3.0A, V_{GS}=-10V;

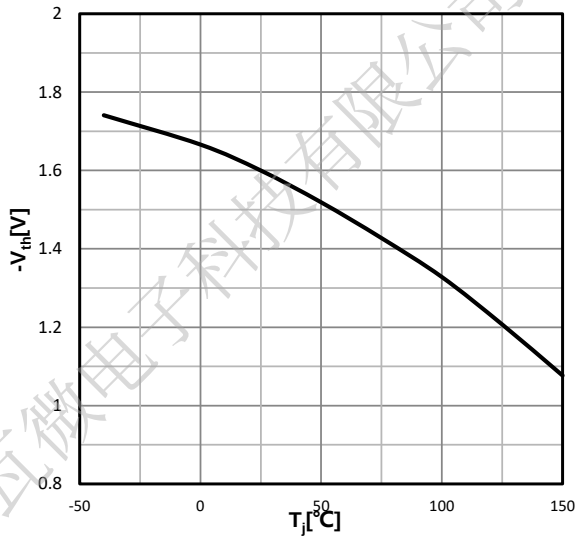
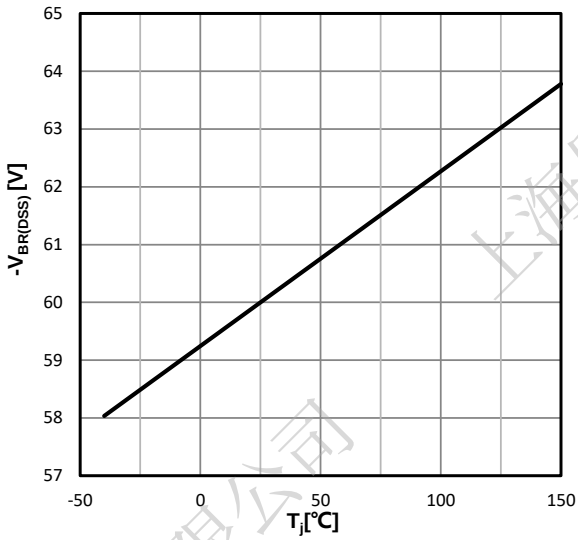
Figure 5: Typ. gate threshold voltage	Figure 6: Drain-source breakdown voltage
	
$V_{GS}=f(T_j)$,I $V_{GS}=V_{DS}$,I_D=-250μA;	$V_{BR(DSS)}=f(T_j)$; I_D=-250μA;

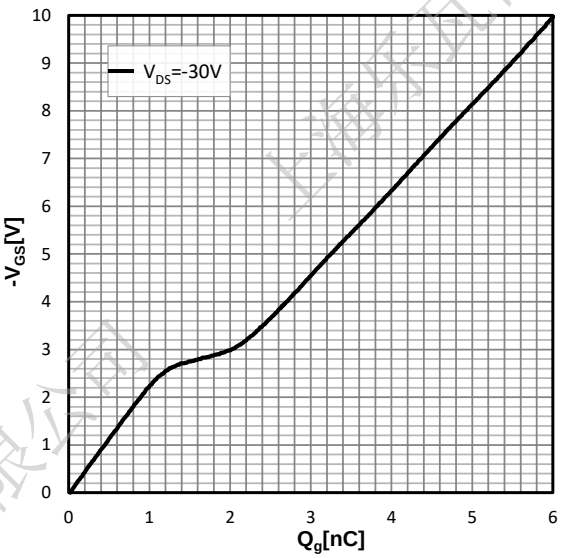
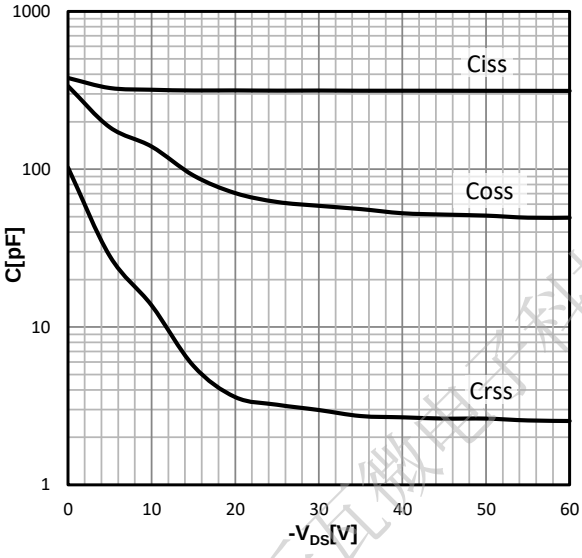
Figure 7: Typ. gate charge	Figure 8: Typ. Capacitances
	
$V_{GS}=f(Q_g)$, I_D=-5.0A, T_j=25 °C; parameter: V_{DS}	$C=f(V_{DS})$; V_{GS}=0V; f=1.0 MHz;

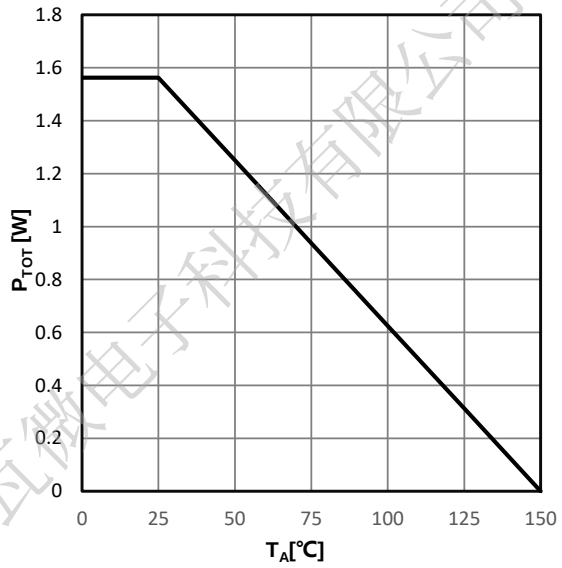
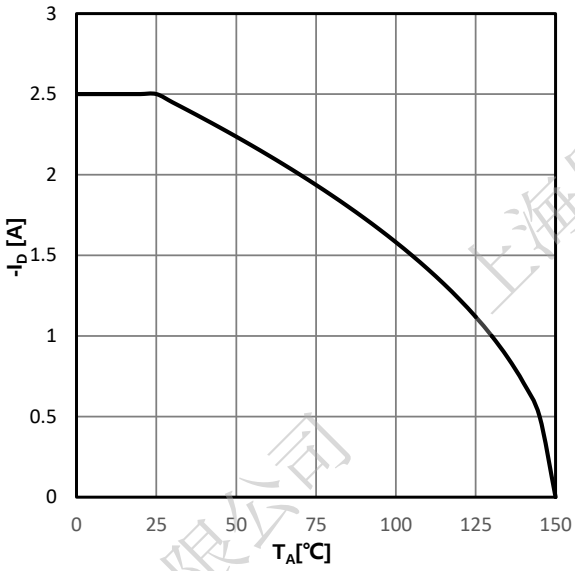
Figure 9: Power dissipation	Figure 10:Drain current
	
$P_{tot}=f(T_A)$;	$I_D=f(T_A)$;

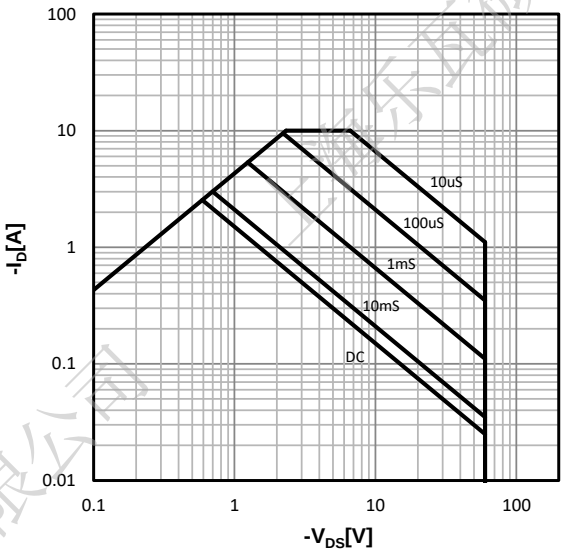
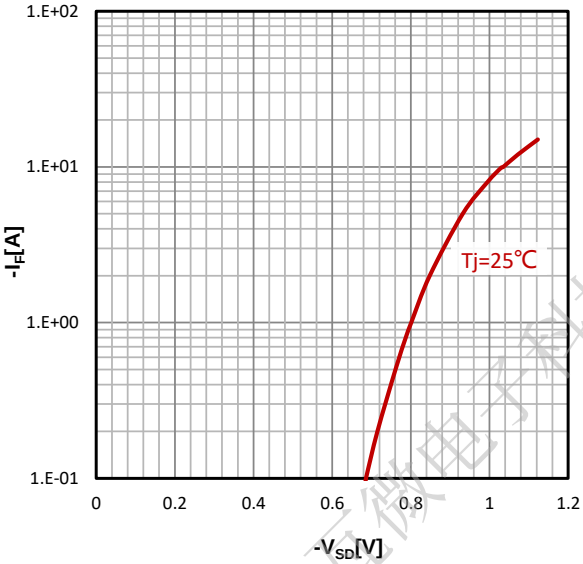
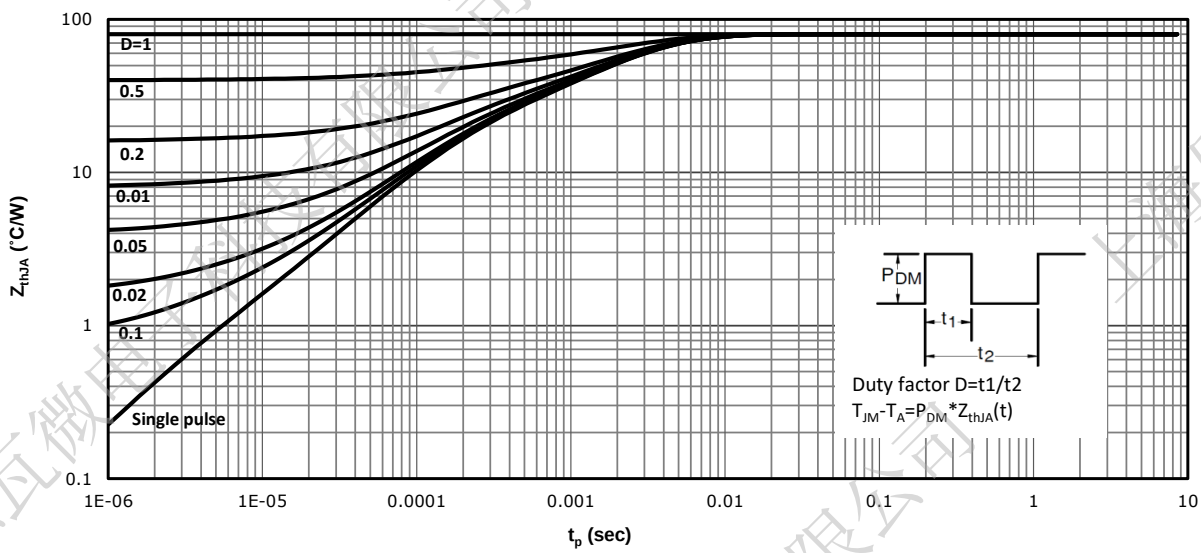
Figure 11: Safe operating area	Figure 12: Typ. forward characteristics
	
$I_D=f(V_{DS})$; T_A=25 °C; D=0; parameter: tp	$I_F=f(V_{SD})$;

Figure 13: Max. Transient Thermal Impedance



$Z_{thJA}=f(t_p)$; parameter: D

Test Circuit & Waveform:

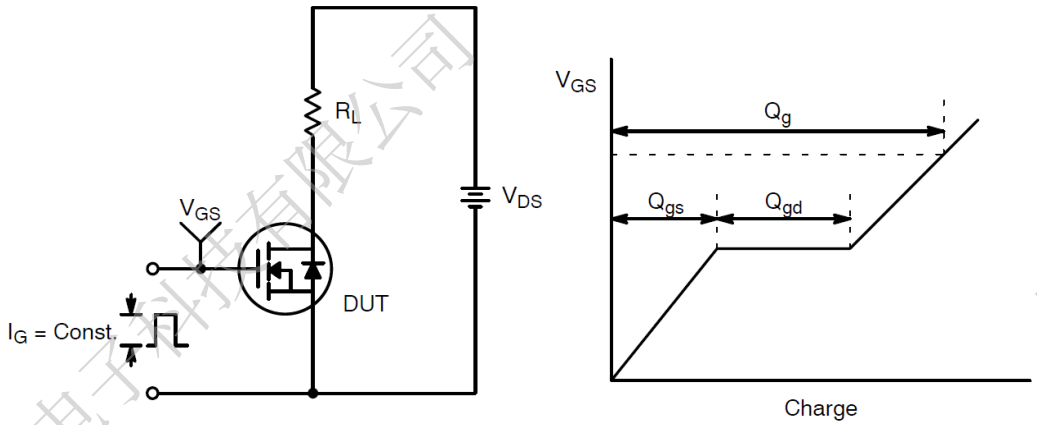


Figure 14: Gate Charge Test Circuit & Waveform

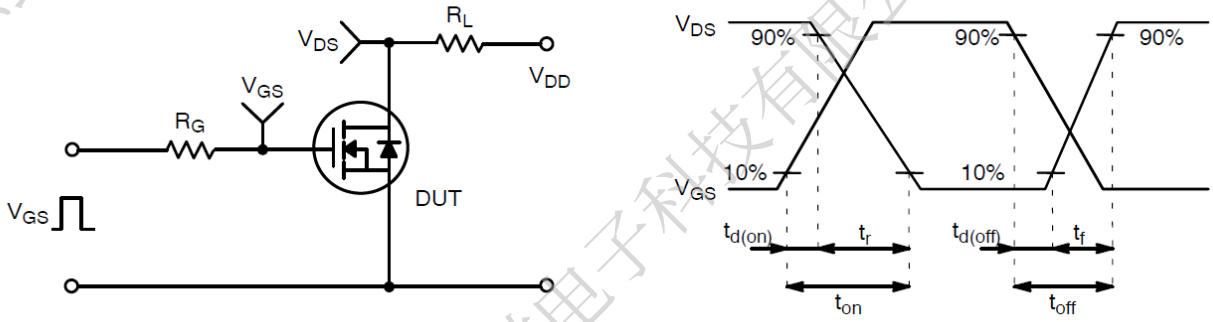


Figure 15: Resistive Switching Test Circuit & Waveforms

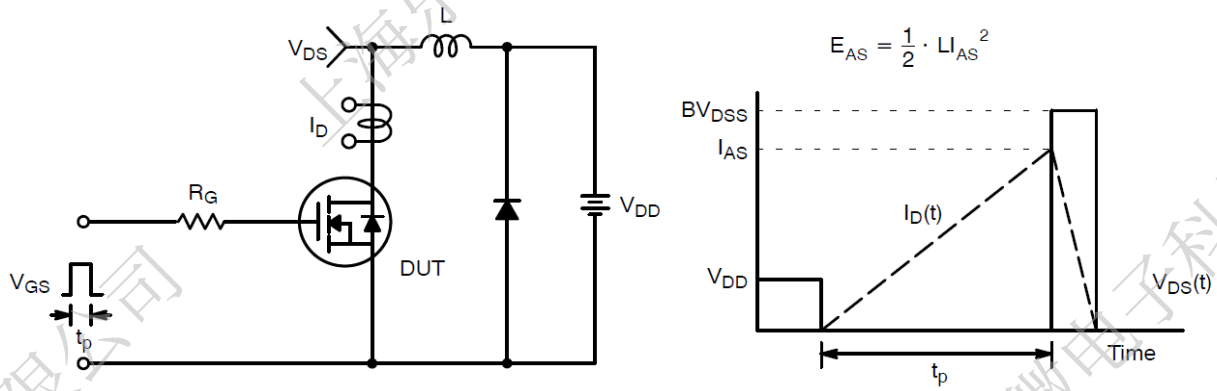
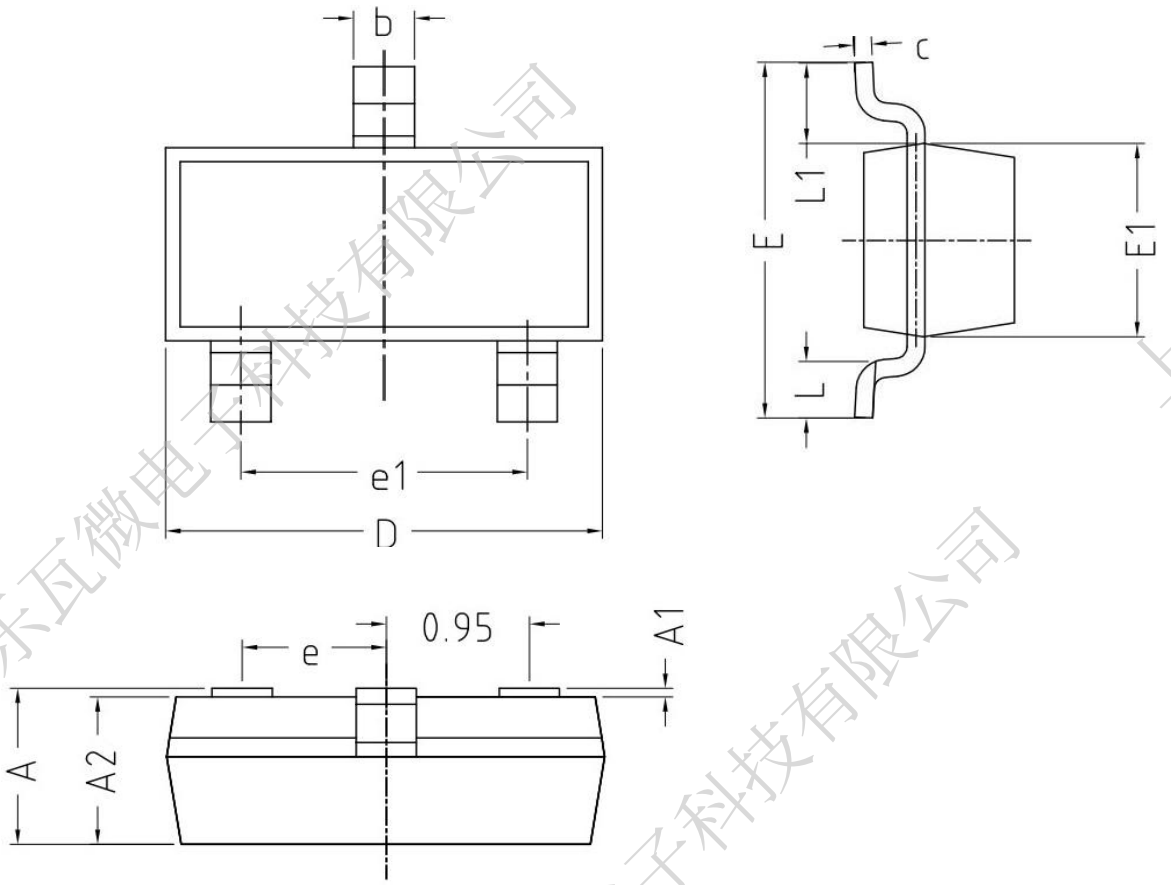


Figure 16: Unclamped Inductive Switching Test Circuit & Waveforms

Package Outline:



COMMON IN DIMENSION (MM)			
Symbol	**Min.**	**Nom.**	**Max.**
A	0.900	1.050	1.150
A1	0.000	0.050	0.100
A2	0.900	1.000	1.050
b	0.300	0.400	0.500
C	0.100	0.130	0.200
D	2.800	2.900	3.000
E	2.250	2.400	2.550
E1	1.200	1.300	1.400
e	0.950 TYP		
e1	1.800	1.900	2.000
L	0.290	0.390	0.490
L1	0.550REF		

Revision History:

Revison	Date	Descriptions
Rev 1.0	Apr.2023	Initial Version

Disclaimer:

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