1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 12×12-bit digital multiplier integrated circuit.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number[1]
−1	ADSP-1012AS(X)/883B
−2	ADSP-1012AT(X)/883B

NOTE
[1]See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-64A	64-Pin DIP
E	E-68A	68-Contact LCC
G	G-68A	68-Lead Pin Grid Array

1.3 Absolute Maximum Ratings.

Supply Voltage . . . . . −0.3 V to 7 V
Input Voltage . . . . . −0.3 V to V_{DD}
Output Voltage . . . . . −0.3 V to V_{DD}
Operating Temperature Range (Ambient) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering 10 sec) . . . . . +300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 25°C/W for D-64A
25°C/W for E-68A
25°C/W for G-68A

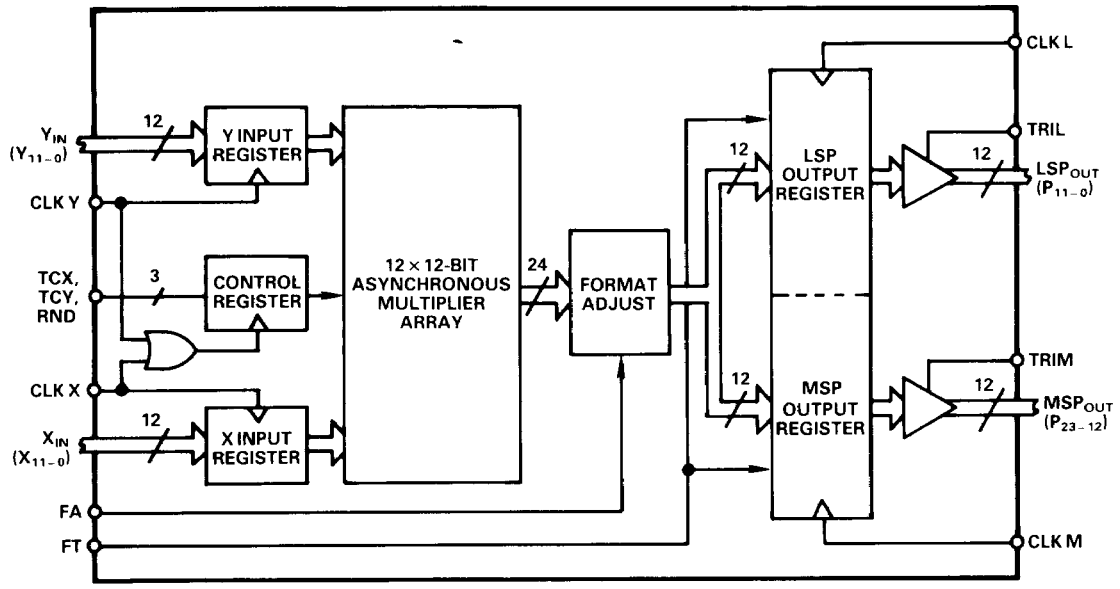
ADSP-1012A – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition[1]	Units
Digital Input High Voltage	V_{IH}	−1, 2	2.0	2.2	2.2			V_{DD} = max	V min
Digital Input Low Voltage	V_{IL}	−1, 2	0.8	0.8	0.8			V_{DD} = min	V max
Digital Output High Voltage	V_{OH}	−1, 2	2.4	2.4	2.4			V_{DD} = min I_{OH} = −1.0 mA	V min
Digital Output Low Voltage*	V_{OL}	−1, 2	0.4	0.5	0.5			V_{DD} = min I_{OL} = +4 mA	V max
Digital Input High Current	I_{IH}	−1, 2	10	10	10			V_{DD} = max V_{IN} = +5.0 V	μA max
Digital Input Low Current	I_{IL}	−1, 2	10	10	10			V_{DD} = max V_{IN} = 0.0 V	μA max
Three-State Leakage Current Low	I_{OZL}	−1, 2	50	50	50			V_{DD} = max V_{IL} = 0 V (High Z)	μA max
Three-State Leakage Current High	I_{OZH}	−1, 2	50	50	50			V_{DD} = max V_{IH} = max (High Z)	μA max
Supply Current*	I_{DD1}	−1, 2	60	70	70			V_{DD} = max; TTL Inputs; f = max	mA max
	I_{DD2}	−1, 2	30	35	35			V_{DD} = max All V_{IN} = 2.4 V	mA max
Output Delay*	t_D	−1, 2	30			40	40	Note 2	ns max
Three-State Enable* (High Z to Low)	t_{ENA}	−1, 2	30			35	35	Notes 2 and 3	ns max
Three-State Disable* (Low to High Z)	t_{DIS}	−1, 2	30			35	35	Notes 2 and 3	ns max
Clock Pulse Width	t_{PW}	−1, 2	20			25	25	Note 2	ns min
Input Setup Time*	t_S	−1, 2	15			20	20	Note 2	ns min
Input Hold Time	t_H	−1, 2	3			3	3	Note 2	ns min
Unclocked Multiply Time*	t_{MUC}	−1	105			125	125	Note 2	ns max
		−2	80			95	95		
Clocked Multiply Time*	t_{MC}	−1	75			90	90	Note 2	ns max
		−2	50			60	60		

NOTES
*Indicates that a limit for this parameter has changed from REV. D.
[1]T_A = +25°C; V_{DD} = +4.5 V min to +5.5 V max (unless otherwise noted).
[2]TTL inputs of 0 V and +3.0 V; V_{DD} = +4.5 V, rise time = 5 ns, and timing transitions, per Figure 1, measured at +1.5 V (unless otherwise noted).
[3]Transitions measured per Figure 2.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.



Pin Assignments

DIP

PIN	FUNCTION	PIN	FUNCTION
1	X7	33	P16
2	X6	34	P17
3	X5	35	P18
4	X4	36	P19
5	X3	37	P20
6	X2	38	P21
7	X1	39	P22
8	X0	40	P23
9	P0	41	TCY
10	P1	42	Y11
11	P2	43	Y10
12	P3	44	Y9
13	P4	45	Y8
14	P5	46	Y7
15	P6	47	Y6
16	P7	48	$+V_{DD}$
17	P8	49	$+V_{DD}$
18	P9	50	$+V_{DD}$
19	P10	51	Y5
20	P11	52	Y4
21	TRIL	53	Y3
22	TRIM	54	Y2
23	GND	55	Y1
24	GND	56	Y0
25	FT	57	TCX
26	FA	58	RND
27	CLK L	59	CLK Y
28	CLK M	60	CLK X
29	P12	61	X11
30	P13	62	X10
31	P14	63	X9
32	P15	64	X8

Pin Grid Array

PIN	FUNCTION	PIN	FUNCTION
1	P0	35	TCY
2	P1	36	Y11
3	P2	37	Y10
4	P3	38	Y9
5	P4	39	Y8
6	P5	40	Y7
7	P6	41	Y6
8	P7	42	V_{DD}
9	P8	43	V_{DD}
10	P9	44	V_{DD}
11	P10	45	Y5
12	P11	46	Y4
13	TRIL	47	Y3
14	TRIM	48	Y2
15	GND	49	Y1
16	GND	50	Y0
17	N/C	51	N/C
18	FT	52	TCX
19	FA	53	RND
20	CLK L	54	CLK Y
21	CLK M	55	CLK X
22	P12	56	X11
23	P13	57	X10
24	P14	58	X9
25	P15	59	X8
26	P16	60	X7
27	P17	61	X6
28	P18	62	X5
29	P19	63	X4
30	P20	64	X3
31	P21	65	X2
32	P22	66	X1
33	P23	67	X0
34	N/C	68	N/C

LCC

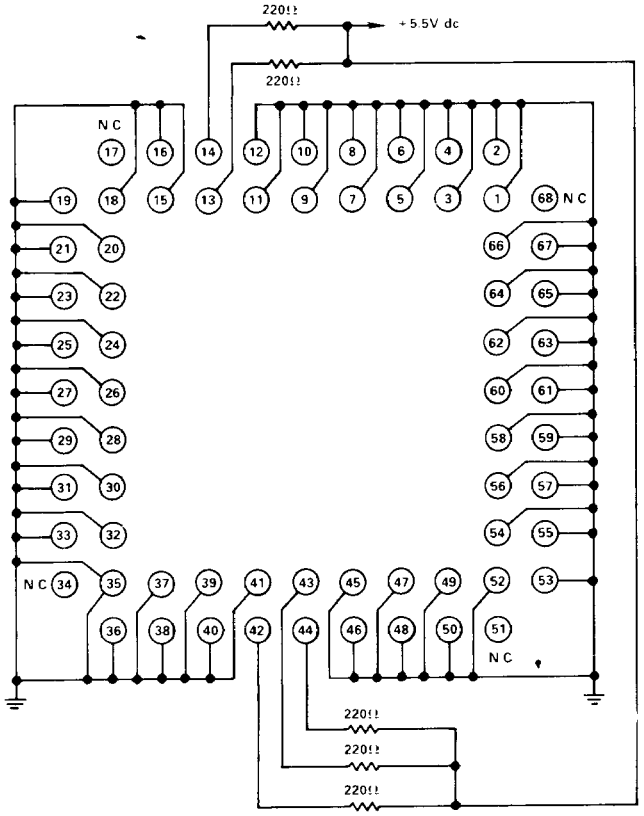
PIN	FUNCTION	PIN	FUNCTION
1	X7	35	P16
2	X6	36	P17
3	X5	37	P18
4	X4	38	P19
5	X3	39	P20
6	X2	40	P21
7	X1	41	P22
8	X0	42	P23
9	N/C	43	N/C
10	P0	44	TCY
11	P1	45	Y11
12	P2	46	Y10
13	P3	47	Y9
14	P4	48	Y8
15	P5	49	Y7
16	P6	50	Y6
17	P7	51	$+V_{DD}$
18	P8	52	$+V_{DD}$
19	P9	53	$+V_{DD}$
20	P10	54	Y5
21	P11	55	Y4
22	TRIL	56	Y3
23	TRIM	57	Y2
24	GND	58	Y1
25	GND	59	Y0
26	N/C	60	N/C
27	FT	61	TCX
28	FA	62	RND
29	CLK L	63	CLK Y
30	CLK M	64	CLK X
31	P12	65	X11
32	P13	66	X10
33	P14	67	X9
34	P15	68	X8

3.2.4 Microcircuit Technology Group.

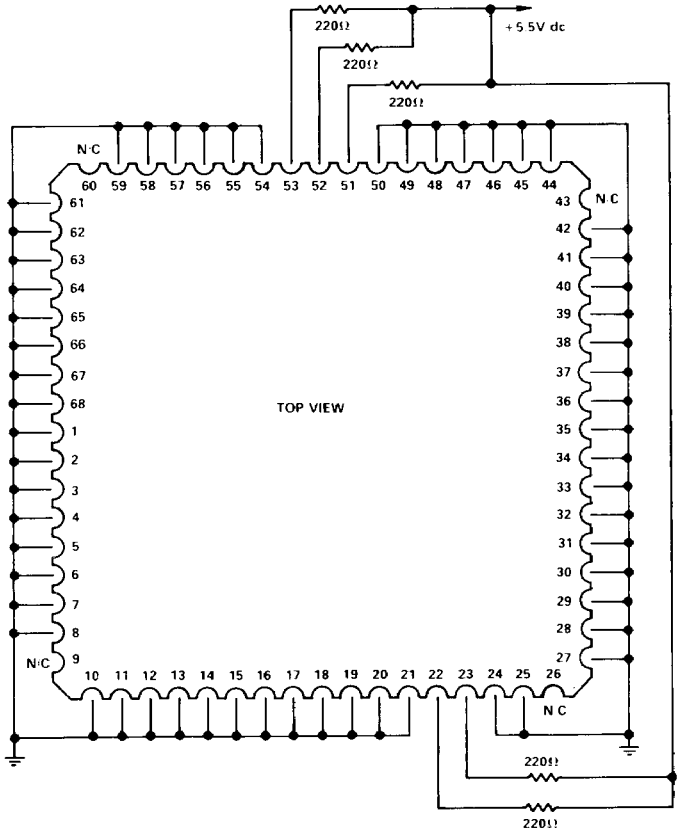
This microcircuit is covered by technology group (105).

4.2.1 Life Test/Burn-In Circuit.

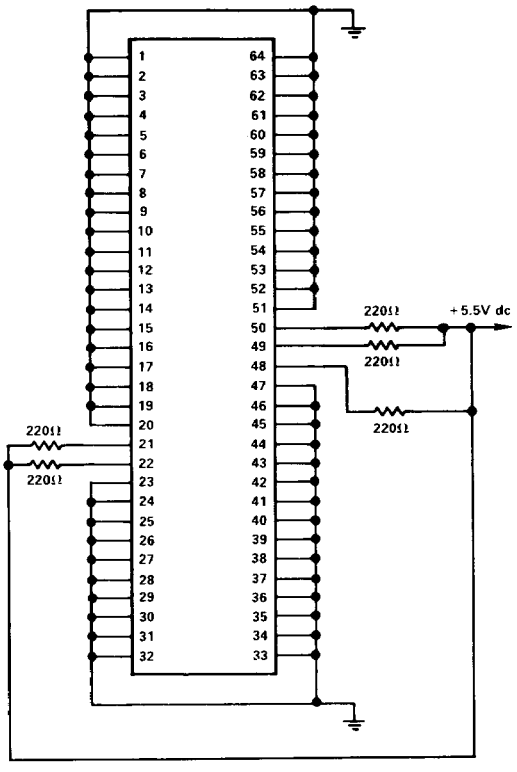
Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



ADSP-1012AG Life Test and Burn-In Circuit



ADSP-1012AE Life Test and Burn-In Circuit



ADSP-1012AD Life Test and Burn-In Circuit

REV. E

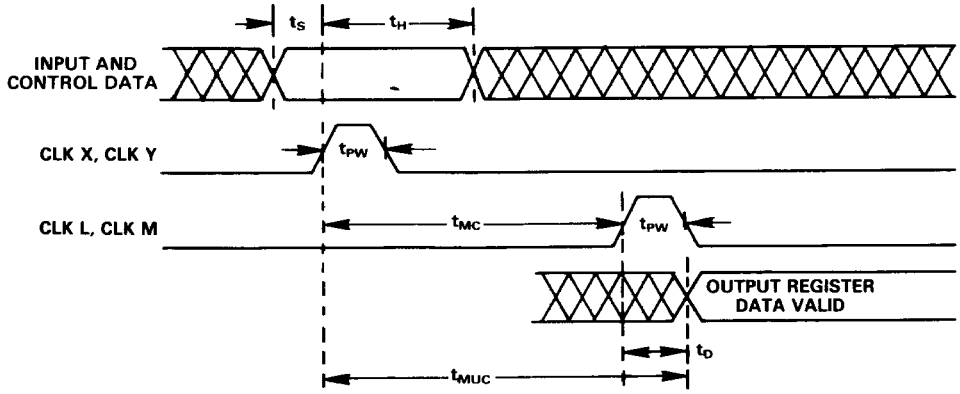


Figure 1. ADSP-1012A Timing Diagram

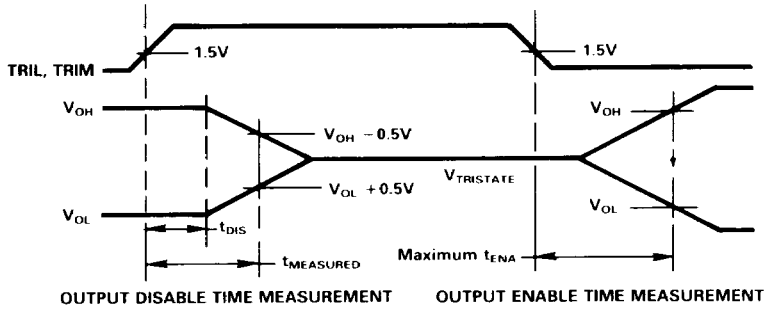


Figure 2. Three-State Disable and Enable Timing

Output disable time, t_{DIS}, is measured from the time the output enable control signal reaches 1.5 V to the time when all outputs have ceased driving. This is calculated by measuring the time, $t_{MEASURED}$, from the same starting point to when the output voltages have changed by 0.5 V toward +1.5 V. From the tester capacitive loading, C_L, and the measured current, i_L, the decay time, t_{DECAY}, can be approximated to first order by:

$$t_{DECAY} = \frac{C_L \cdot 0.5\ V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. Disable times are longest at the highest specified temperature.

The maximum output enable time, maximum t_{ENA}, is also measured from output enable control signal at 1.5 V to the time when all outputs have reached TTL input levels (V_{OH} or V_{OL}). This could also be considered as "data valid." Maximum enable times are longest at the highest specified temperature.

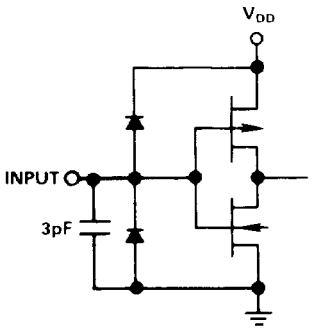


Figure 3. Equivalent Input Circuit

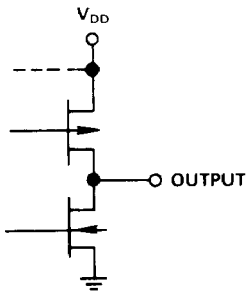


Figure 4. Equivalent Output Circuit

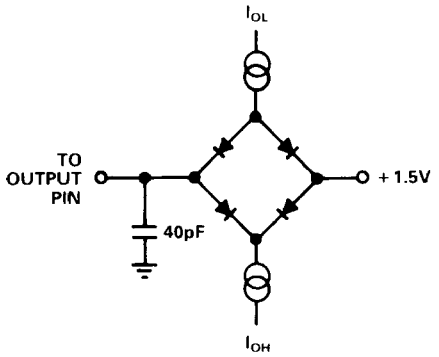


Figure 5. Normal Load Circuit for AC Measurements