

## CMP-01

### FEATURES

- Fast Response Time ..... 180ns Max
- High Input Slew Rate ..... 92V/ $\mu$ s
- Low Offset Voltage ..... 0.3mV Typical, 0.8mV Max
- Low Offset Current ..... 4nA Typical, 25nA Max
- Low Offset Drift ..... 1 $\mu$ V/ $^{\circ}$ C, 30pA/ $^{\circ}$ C
- Standard Power Supplies ..... +5V or  $\pm$ 5V to  $\pm$ 18V
- Guaranteed Operation from Single +5V Supply
- No Pull-Up Resistor Required for TTL Drive
- Wired OR Capability
- Fits 111, 106, 710 Sockets
- Easy Offset Nulling ..... Single 2k $\Omega$  Potentiometer
- Easy to Use ..... Free from Oscillations
- Available in Die Form

### GENERAL DESCRIPTION

The CMP-01 is a monolithic fast precision voltage comparator using an advanced NPN-Schottky Barrier Diode process. It features fast response time to both large and small input signals, while maintaining excellent input characteristics. The CMP-01 is capable of operating over a wide range of supply voltages including single ended 5 volt supply. The large output current sinking and high output voltage capability assure good application flexibility, while the combination of fast response, high accuracy, and freedom from oscillation assure performance in precision level detectors and 12 and 13-bit A/D converters. The CMP-01 is pin-compatible to earlier 111, 106, and 710 types. For applications requiring lower input offset and bias currents, refer to the CMP-02 data sheet.

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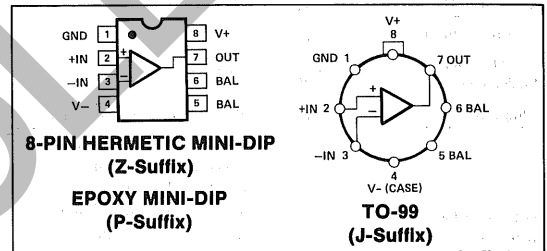
### ORDERING INFORMATION <sup>†</sup>

| T <sub>A</sub> = +25 $^{\circ}$ C<br>V <sub>OS</sub> MAX<br>(mV) | PACKAGE |                 |                  | OPERATING<br>TEMPERATURE<br>RANGE |
|--|---------|-----------------|------------------|-----------------------------------|
|  | TO-99   | CERDIP<br>8-PIN | PLASTIC<br>8-PIN |                                   |
| 0.8  | CMP01J* | CMP01Z/883      | —                | MIL                               |
| 0.8  | CMP01EJ | CMP01EZ         | CMP01EP          | COM                               |
| 2.8  | CMP01CJ | CMP01CZ         | CMP01CP          | COM                               |

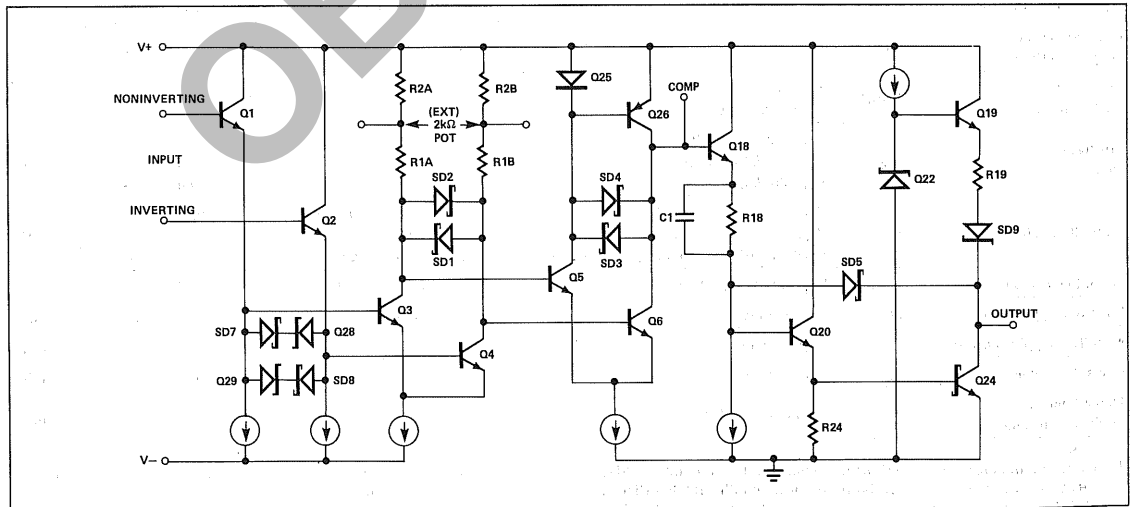
\* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

<sup>†</sup> Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

### PIN CONNECTIONS



### SIMPLIFIED SCHEMATIC



# CMP-01

## ABSOLUTE MAXIMUM RATINGS (Note 1)

|  |                 |
|--|-----------------|
| Total Supply Voltage, V+ to V-             | 36V             |
| Output to Ground                           | -5V to +32V     |
| Output to Negative Supply Voltage          | 50V             |
| Ground to Negative Supply Voltage          | 30V             |
| Positive Supply Voltage to Ground          | +30V            |
| Positive Supply Voltage to Offset Null     | 0 to 2V         |
| Differential Input Voltage                 | ±11V            |
| Input Voltage (V <sub>S</sub> = ±15V)      | ±15V            |
| Output Sink Current (Continuous Operation) | 75mA            |
| Operating Temperature Range                |                 |
| CMP-01                                     | -55°C to +125°C |
| CMP-01E, CMP-01C                           | 0°C to +70°C    |
| Junction Temperature (T <sub>J</sub> )     | -65°C to +150°C |
| Storage Temperature Range                  | -65°C to +150°C |
| P-Suffix                                   | -65°C to +125°C |

|                                      |            |
|--------------------------------------|------------|
| Lead Temperature (Soldering, 60 sec) | 300°C      |
| Output Short-Circuit Duration        |            |
| To Ground                            | Indefinite |
| To V+                                | 1 Minute   |

| PACKAGE TYPE          | θ <sub>JA</sub> (Note 2) | θ <sub>JC</sub> | UNITS |
|-----------------------|--------------------------|-----------------|-------|
| TO-99 (J)             | 150                      | 18              | °C/W  |
| 8-Pin Plastic DIP (P) | 148                      | 16              | °C/W  |
| 8-Pin SO (S)          | 103                      | 43              | °C/W  |

### NOTES:

1. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.
2. θ<sub>JA</sub> is specified for worst case mounting conditions, i.e., θ<sub>JA</sub> is specified for device in socket for TO and P-DIP packages.

## ELECTRICAL CHARACTERISTICS at V<sub>S</sub> = ±15V, T<sub>A</sub> = 25°C, unless otherwise noted.

| PARAMETER                       | SYMBOL            | CONDITIONS  | CMP-01 |      |      | CMP-01E |      |      | CMP-01C |     |      | UNITS |
|---------------------------------|-------------------|---|--------|------|------|---------|------|------|---------|-----|------|-------|
|                                 |                   |   | MIN    | TYP  | MAX  | MIN     | TYP  | MAX  | MIN     | TYP | MAX  |       |
| Input Offset Voltage            | V <sub>OS</sub>   | R <sub>S</sub> ≤ 5kΩ, (Note 1)                                  | —      | 0.3  | 0.8  | —       | 0.4  | 2.8  | —       | 0.4 | 2.8  | mV    |
| Input Offset Current            | I <sub>OS</sub>   | (Note 1)  | —      | 4    | 25   | —       | 5    | 80   | —       | 5   | 80   | nA    |
| Input Bias Current              | I <sub>B</sub>    |   | —      | 350  | 600  | —       | 400  | 900  | —       | 400 | 900  | nA    |
| Differential Input Resistance   | R <sub>IN</sub>   | (Note 2)  | 150    | 300  | —    | 100     | 200  | —    | —       | —   | —    | kΩ    |
| Voltage Gain                    | A <sub>V</sub>    | V <sub>O</sub> = 0.4V to 2.4V, (Notes 1, 2)                     | 200    | 500  | —    | 100     | 500  | —    | —       | —   | —    | V/mV  |
| Response Time<br>(Note 3)       | t <sub>r</sub>    | 100mV step, 5mV Overdrive<br>No Load (No Pull-Up)               | —      | 110  | 180  | —       | 110  | 180  | —       | —   | —    | ns    |
|                                 |                   | 5kΩ to 5v (Pull-Up)   | —      | 110  | —    | —       | 110  | —    | —       | —   | —    |       |
|                                 |                   | TTL Fan-Out = 4, No Pull-Up                                     | —      | 110  | —    | —       | 110  | —    | —       | —   | —    |       |
|                                 |                   | 5V Step 5mV Overdrive<br>No Load (No Pull-Up)                   | —      | 160  | —    | —       | 160  | —    | —       | —   | —    |       |
|                                 |                   | 5kΩ to 5v (Pull-Up)<br>TTL Fan-Out = 4, No Pull-Up              | —      | 160  | —    | —       | 160  | —    | —       | —   | —    |       |
| Input Slew Rate                 |                   |   | —      | 92   | —    | —       | 92   | —    | —       | —   | V/μs |       |
| Input Voltage Range             | CMVR              |   | ±12.5  | ±13  | —    | ±12.5   | ±13  | —    | —       | —   | V    |       |
| Common-Mode Rejection Ratio     | CMRR              |   | 94     | 110  | —    | 90      | 110  | —    | —       | —   | dB   |       |
| Power Supply Rejection Ratio    | PSRR              | 5V ≤ V <sub>S+</sub> ≤ 18V,<br>-18V ≤ V <sub>S-</sub> ≤ 0V      | 80     | 100  | —    | 74      | 98   | —    | —       | —   | dB   |       |
| Positive Output Voltage         | V <sub>OH</sub>   | V <sub>IN</sub> ≥ 3mV, I <sub>O</sub> = 320μA                   | 2.4    | 3.2  | —    | —       | —    | —    | —       | —   | —    | V     |
|                                 |                   | V <sub>IN</sub> ≥ 3mV, I <sub>O</sub> = 240μA                   | —      | —    | —    | 2.4     | 3.4  | —    | —       | —   | —    |       |
|                                 |                   | V <sub>IN</sub> ≥ 3mV, I <sub>O</sub> = 0mA                     | 2.4    | 4.8  | —    | 2.4     | 4.8  | —    | —       | —   | —    |       |
| Saturation Voltage              | V <sub>OL</sub>   | V <sub>IN</sub> ≤ -10mV, I <sub>sink</sub> = 0mA                | —      | 0.16 | 0.4  | —       | 0.16 | 0.4  | —       | —   | —    | V     |
|                                 |                   | V <sub>IN</sub> ≤ -10mV, I <sub>sink</sub> ≤ 6.4mA              | —      | 0.3  | 0.45 | —       | 0.31 | 0.45 | —       | —   | —    |       |
|                                 |                   | V <sub>IN</sub> ≤ -10mV, I <sub>sink</sub> ≤ 12mA (CMP-01 only) | —      | 0.36 | 0.5  | —       | —    | —    | —       | —   | —    |       |
| Output Leakage Current          | I <sub>LEAK</sub> | V <sub>IN</sub> ≥ 10mV, V <sub>O</sub> = +30V                   | —      | 0.03 | 2    | —       | 0.05 | 8    | —       | —   | μA   |       |
| Positive Supply Current         | I+                | V <sub>IN</sub> ≤ -10mV   | —      | 5.6  | 8    | —       | 5.6  | 8.5  | —       | —   | mA   |       |
| Negative Supply Current         | I-                | V <sub>IN</sub> ≤ -10mV   | —      | 1.3  | 2.2  | —       | 1.3  | 2.2  | —       | —   | mA   |       |
| Power Dissipation               | P <sub>d</sub>    | V <sub>IN</sub> ≤ -10mV   | —      | 103  | 153  | —       | 103  | 161  | —       | —   | mW   |       |
| Offset Voltage Adjustment Range |                   | Nulling Pot ≥ 2kΩ   | —      | ±5   | —    | —       | ±5   | —    | —       | —   | mV   |       |

### NOTES:

1. These parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1kΩ load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.
2. Guaranteed by design.
3. Sample tested.

**ELECTRICAL CHARACTERISTICS** at  $V_{S+} = 5V$ ,  $V_{S-} = 0V$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

| PARAMETER               | SYMBOL   | CONDITIONS  | CMP-01<br>CMP-01E |         |      | CMP-01C |         |      | UNITS |
|-------------------------|----------|---|-------------------|---------|------|---------|---------|------|-------|
|                         |          |   | MIN               | TYP     | MAX  | MIN     | TYP     | MAX  |       |
| Input Offset Voltage    | $V_{OS}$ | $R_S \leq 5k\Omega$ , (Note 1)  | —                 | 0.4     | 1.5  | —       | 0.5     | 3.5  | mV    |
| Input Offset Current    | $I_{OS}$ | (Note 1)  | —                 | 3       | 21   | —       | 4       | 65   | nA    |
| Input Bias Current      | $I_B$    |   | —                 | 250     | 500  | —       | 300     | 720  | nA    |
| Voltage Gain            | $A_V$    | $V_O = 0.4V$ to $2.4V$ , (Notes 1, 2)                                       | —                 | 50      | —    | —       | 50      | —    | V/mV  |
| Response Time           | $t_r$    | 100mV Step, 5mV Overdrive   | —                 | 150     | —    | —       | 150     | —    | ns    |
|                         |          | 5k $\Omega$ to 5V (Pull-Up)<br>TTL Fan-Out = 4, 5k $\Omega$ to 5V (Pull-Up) | —                 | 150     | —    | —       | 150     | —    |       |
| Input Voltage Range     | CMVR     |   | 1.8               | 1.7-3.8 | 3.5  | 1.8     | 1.7-3.8 | 3.5  | V     |
| Saturation Voltage      | $V_{OL}$ | $V_{IN} \leq -10mV$ , $I_{sink} \leq 6.4mA$                                 | —                 | 0.3     | 0.45 | —       | 0.3     | 0.45 | V     |
| Positive Supply Current | $I_+$    | $V_{IN} \leq -10mV$   | —                 | 2.3     | 3.2  | —       | 2.4     | 3.8  | mA    |
| Power Dissipation       | $P_d$    | $V_{IN} \leq -10mV$   | —                 | 11.5    | 16   | —       | 12      | 19   | mW    |

**ELECTRICAL CHARACTERISTICS** at  $V_S = \pm 15V$ ,  $-55^\circ C \leq T_A \leq 125^\circ C$ , unless otherwise noted.

| PARAMETER                          | SYMBOL      | CONDITIONS  | CMP-01   |          |      | UNITS            |
|------------------------------------|-------------|---|----------|----------|------|------------------|
|                                    |             |   | MIN      | TYP      | MAX  |                  |
| Input Offset Voltage               | $V_{OS}$    | $R_S \leq 5k\Omega$ , (Note 1)<br>$V_{S+} = 5V$ , $V_{S-} = 0V$ , (Note 1)          | —        | 0.5      | 1.6  | mV               |
|                                    |             |   | —        | 0.6      | 2.8  |                  |
| Average Input Offset Voltage Drift |             |   |          |          |      |                  |
| Without External Trim              | $TCV_{OS}$  | $R_S = 50\Omega$  | —        | 1.5      | —    | $\mu V/^\circ C$ |
| With External Trim                 | $TCV_{OSn}$ |   | —        | 1        | —    |                  |
| Input Offset Current               | $I_{OS}$    | $T_A = +125^\circ C$ , (Note 1)<br>$T_A = -55^\circ C$ , (Note 1)                   | —        | 4        | 25   | nA               |
|                                    |             |   | —        | 5        | 45   |                  |
| Average Input Offset Current Drift | $TCI_{OS}$  | $+25^\circ C \leq T_A \leq +125^\circ C$<br>$-55^\circ C \leq T_A \leq +25^\circ C$ | —        | 12       | —    | $pA/^\circ C$    |
|                                    |             |   | —        | 35       | —    |                  |
| Input Bias Current                 | $I_B$       | $T_A = +125^\circ C$<br>$T_A = -55^\circ C$   | —        | 330      | 600  | nA               |
|                                    |             |   | —        | 550      | 1400 |                  |
| Voltage Gain                       | $A_V$       | $V_O = 0.4V$ to $2.4V$ , (Notes 1, 2)   | 100      | 500      | —    | V/mV             |
| Response Time                      | $t_r$       | 100mV Step, 5mV Overdrive, (Note 2)   | —        | 220      | —    | ns               |
|                                    |             | $T_A = +125^\circ C$ , No Load<br>$T_A = -55^\circ C$ , No Load                     | —        | 100      | —    |                  |
| Input Voltage Range                | CMVR        |   | $\pm 12$ | $\pm 13$ | —    | V                |
| Common-Mode Rejection Ratio        | CMRR        |   | 88       | 106      | —    | dB               |
| Power Supply Rejection Ratio       | PSRR        | $5V \leq V_{S+} \leq 15V$ , $-15V \leq V_{S-} \leq 0V$                              | 75       | 96       | —    | dB               |
| Positive Output Voltage            | $V_{OH}$    | $V_{IN} \geq 4mV$ , $I_O = 200\mu A$  | 2.4      | 3        | —    | V                |
| Saturation Voltage                 | $V_{OL}$    | $V_{IN} \leq -10mV$ , $I_{sink} = 0mA$  | —        | 0.20     | 0.4  | V                |
|                                    |             | $V_{IN} \leq -10mV$ , $I_{sink} = 6.4mA$  | —        | 0.32     | 0.5  |                  |

**NOTES:**

1. These parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1k $\Omega$  load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.
2. Guaranteed by design.

# CMP-01

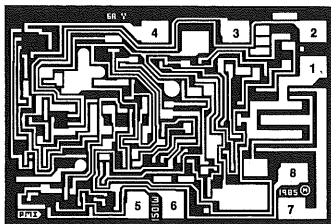
**ELECTRICAL CHARACTERISTICS** at  $V_S = \pm 15V$ ,  $0^\circ C \leq T_A \leq 70^\circ C$ , unless otherwise noted.

| PARAMETER                          | SYMBOL      | CONDITIONS   | CMP-01E    |            |     | CMP-01C    |            |      | UNITS            |
|------------------------------------|-------------|--|------------|------------|-----|------------|------------|------|------------------|
|                                    |             |  | MIN        | TYP        | MAX | MIN        | TYP        | MAX  |                  |
| Input Offset Voltage               | $V_{OS}$    | $R_S \leq 5k\Omega$ , (Note 1)                         | —          | 0.4        | 1.4 | —          | 0.5        | 3.5  | mV               |
|                                    |             | $V_{S+} = 5V$ , $V_{S-} = 0V$ , (Note 1)               | —          | 0.5        | 2.4 | —          | 0.6        | 4.3  |                  |
| Average Input Offset Voltage Drift |             |  |            |            |     |            |            |      |                  |
| Without External Trim              | $TCV_{OS}$  | $R_S = 50\Omega$                                       | —          | 1.5        | —   | —          | 1.8        | —    | $\mu V/^\circ C$ |
| With External Trim                 | $TCV_{OSn}$ |  | —          | 1.0        | —   | —          | 1.2        | —    |                  |
| Input Offset Current               | $I_{OS}$    | $T_A = +70^\circ C$ , (Note 1)                         | —          | 4          | 25  | —          | 5          | 80   | nA               |
|                                    |             | $T_A = 0^\circ C$ , (Note 1)                           | —          | 5          | 45  | —          | 6          | 120  |                  |
| Average Input Offset Current Drift | $TCI_{OS}$  | $+25^\circ C \leq T_A \leq +70^\circ C$                | —          | 12         | —   | —          | 12         | —    | $\mu A/^\circ C$ |
|                                    |             | $0^\circ C \leq T_A \leq +25^\circ C$                  | —          | 35         | —   | —          | 40         | —    |                  |
| Input Bias Current                 | $I_B$       | $T_A = +70^\circ C$                                    | —          | 330        | 600 | —          | 340        | 900  | nA               |
|                                    |             | $T_A = 0^\circ C$                                      | —          | 400        | 950 | —          | 450        | 1200 |                  |
| Voltage Gain                       | $A_V$       | $V_O = 0.4V$ to $2.4V$ , (Notes 1, 2)                  | 100        | 500        | —   | 70         | 500        | —    | V/mV             |
| Response Time                      | $t_r$       | 100mV Step, 5mV Overdrive                              | —          | 150        | —   | —          | 150        | —    | ns               |
|                                    |             | $T_A = +70^\circ C$ , No Load                          | —          | 100        | —   | —          | 100        | —    |                  |
|                                    |             | $T_A = 0^\circ C$ , No Load                            | —          | 100        | —   | —          | 100        | —    |                  |
| Input Voltage Range                | CMVR        |  | $\pm 12.0$ | $\pm 13.3$ | —   | $\pm 12.0$ | $\pm 13.3$ | —    | V                |
| Common-Mode Rejection Ratio        | CMRR        |  | 90         | 108        | —   | 86         | 108        | —    | dB               |
| Power Supply Rejection Ratio       | PSRR        | $5V \leq V_{S+} \leq 15V$ , $-15V \leq V_{S-} \leq 0V$ | 77         | 98         | —   | 70         | 88         | —    | dB               |
| Positive Output Voltage            | $V_{OH}$    | $V_{IN} \geq 4mV$ , $I_O = 200\mu A$                   | 2.4        | 3.2        | —   | 2.4        | 3.2        | —    | V                |
| Saturation Voltage                 | $V_{OL}$    | $V_{IN} \leq -10mV$ , $I_{sink} = 0$                   | —          | 0.17       | 0.4 | —          | 0.17       | 0.4  | V                |
|                                    |             | $V_{IN} \leq -10mV$ , $I_{sink} = 6.4mA$               | —          | 0.3        | 0.5 | —          | 0.31       | 0.5  |                  |

## NOTES:

- These parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1k $\Omega$  load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.
- Guaranteed by design.

DICE CHARACTERISTICS



DIE SIZE 0.065 × 0.043 inch, 2730 sq. mils  
(1.651 × 1.092 mm, 1.803 sq. mm)

1. GROUND
2. NONINVERTING INPUT
3. INVERTING INPUT
4. NEGATIVE SUPPLY (SUBSTRATE)
5. BALANCE
6. BALANCE
7. OUTPUT
8. POSITIVE SUPPLY

WAFER TEST LIMITS at  $V_S = \pm 15V$ ,  $T_A = 25^\circ C$ .

| PARAMETER                     | SYMBOL     | CONDITIONS   | CMP-01N<br>LIMIT | CMP-01GR<br>LIMIT | UNITS          |
|-------------------------------|------------|--|------------------|-------------------|----------------|
| Input Offset Voltage          | $V_{OS}$   | $R_S \leq 5k\Omega$ , (Note 1)   | 0.8              | 2.8               | mV MAX         |
| Input Offset Current          | $I_{OS}$   | (Note 1)   | 25               | 80                | nA MAX         |
| Input Bias Current            | $I_B$      |  | 600              | 900               | nA MAX         |
| Differential Input Resistance | $R_{IN}$   | (Note 2)   | 150              | 100               | k $\Omega$ MIN |
| Input Voltage Range           | CMVR       |  | $\pm 12.5$       | $\pm 12.5$        | V MIN          |
| Common-Mode Rejection Ratio   | CMRR       | $V_{CM} = \pm CMVR$  | 94               | 90                | dB MIN         |
| Power Supply Rejection Ratio  | PSRR       | $5V \leq V_S \leq 18V$<br>$-18V \leq V_S \leq 0V$                            | 80               | 74                | dB MIN         |
| Positive Output Voltage       | $V_{OH}$   | $V_{IN} \geq 3mV$ , $I_O = 320\mu A$<br>$V_{IN} \geq 3mV$ , $I_O = 240\mu A$ | 2.4<br>—         | —<br>2.4          | V MIN          |
| Saturation Voltage            | $V_{OL}$   | $I_{sink} = 6.4mA$   | 0.45             | 0.45              | V MAX          |
| Output Leakage Current        | $I_{LEAK}$ | $V_{IN} \geq 10mV$ , $V_O = 30V$   | 2                | 8                 | $\mu A$ MAX    |
| Positive Supply Current       | I+         | $V_{IN} \leq -10mV$  | 8.0              | 8.5               | mA MAX         |
| Negative Supply Current       | I-         | $V_{IN} \leq -10mV$  | 2.2              | 2.2               | mA MAX         |
| Power Consumption             | $P_d$      | $V_{IN} \leq -10mV$  | 153              | 161               | mW MAX         |

NOTES:

1. These parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1k $\Omega$  load tied to

+5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.

2. Guaranteed by design.

WAFER TEST LIMITS at  $V_S + = 5V$  and  $V_S - = 0V$ ,  $T_A = 25^\circ C$ .

| PARAMETER            | SYMBOL   | CONDITIONS                     | CMP-01N<br>LIMIT | CMP-01GR<br>LIMIT | UNITS  |
|----------------------|----------|--------------------------------|------------------|-------------------|--------|
| Input Offset Voltage | $V_{OS}$ | $R_S \leq 5k\Omega$ , (Note 1) | 1.5              | 3.5               | mV MAX |
| Input Offset Current | $I_{OS}$ |                                | 21               | 65                | nA MAX |

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

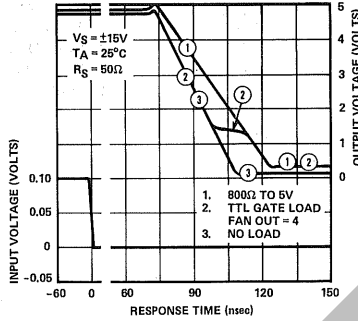
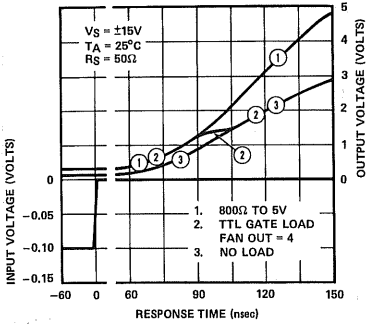
TYPICAL ELECTRICAL CHARACTERISTICS at  $V_S = \pm 15V$ , and  $25^\circ C$ .

| PARAMETER                          | SYMBOL     | CONDITIONS  | CMP-01N<br>TYPICAL | CMP-01GR<br>TYPICAL | UNITS            |
|------------------------------------|------------|---|--------------------|---------------------|------------------|
| Average Input Offset Voltage Drift | $TCV_{OS}$ | $R_S = 50\Omega$  | 1.5                | 1.8                 | $\mu V/^\circ C$ |
| Average Input Offset Current Drift | $TCI_{OS}$ |   | 35                 | 40                  | pA/°C            |
| Response Time                      | $t_r$      | 100mV Step, 5mV Overdrive<br>No Load (No Pull-Up), $T_A = 25^\circ C$ | 110                | 110                 | ns               |

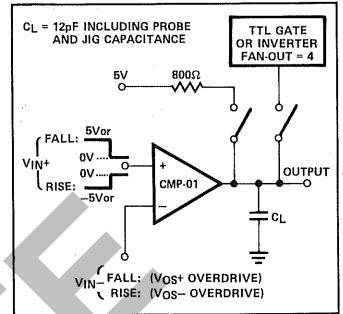
# CMP-01

## TYPICAL PERFORMANCE CHARACTERISTICS

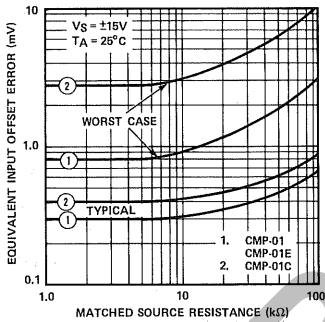
### RESPONSE TIME, 100mV STEP, 5mV OVERDRIVE, VARIOUS LOADS



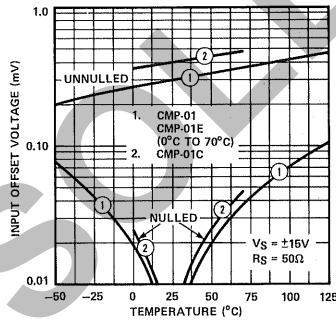
### RESPONSE TIME TEST CIRCUIT



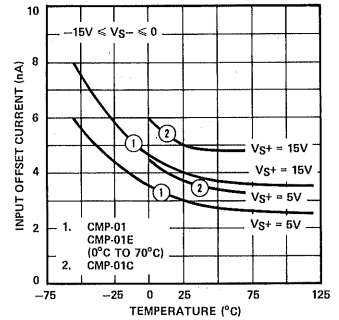
### INPUT OFFSET ERROR vs SOURCE RESISTANCE



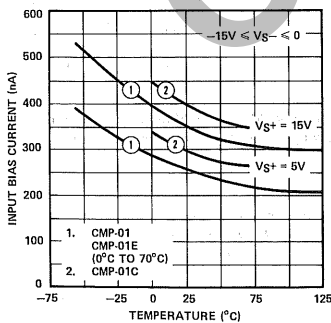
### OFFSET VOLTAGE vs TEMPERATURE



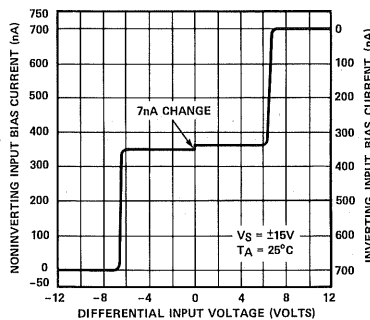
### INPUT OFFSET CURRENT vs TEMPERATURE



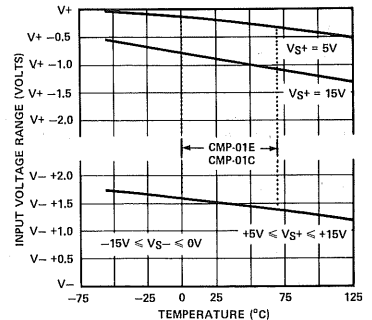
### INPUT BIAS CURRENT vs TEMPERATURE



### INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE

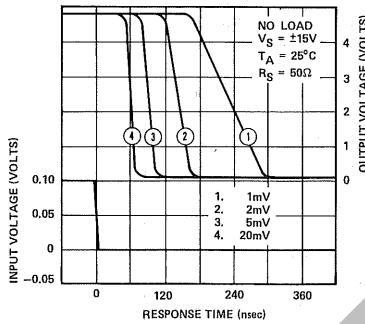
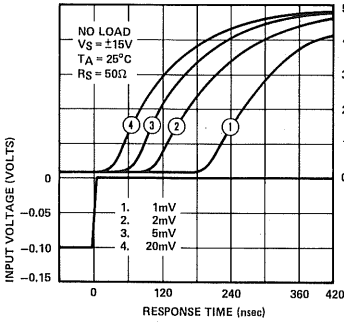


### INPUT VOLTAGE RANGE vs TEMPERATURE

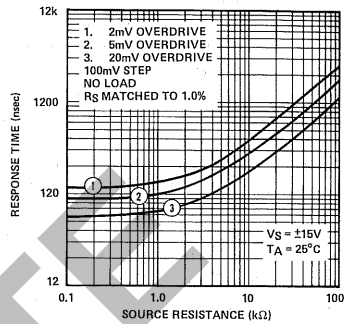


TYPICAL PERFORMANCE CHARACTERISTICS

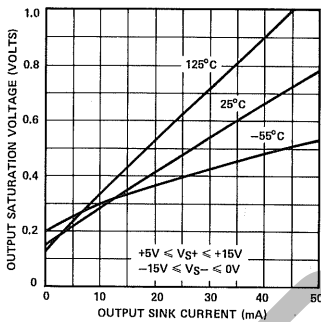
RESPONSE TIME  
FOR 100mV STEP AND VARIOUS INPUT OVERDRIVES



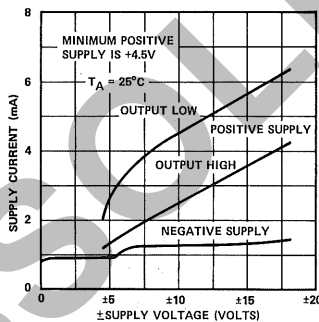
RESPONSE TIME vs  
SOURCE RESISTANCE



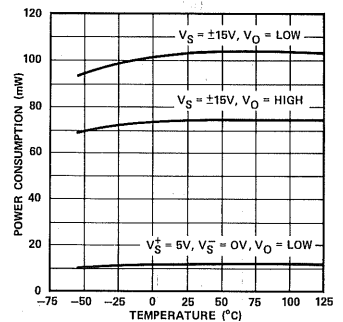
SATURATION VOLTAGE  
vs SINK CURRENT



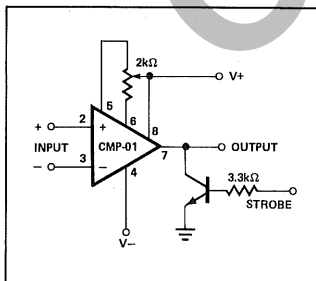
SUPPLY CURRENT vs  
SUPPLY VOLTAGE



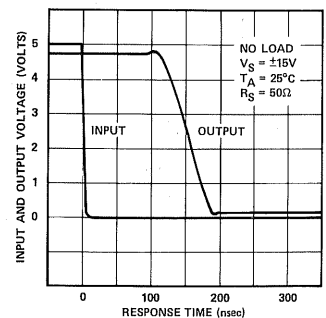
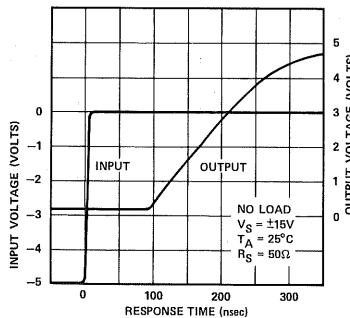
POWER CONSUMPTION  
vs TEMPERATURE



OFFSET TRIMMING AND  
STROBE CIRCUIT



RESPONSE TIME  
FOR 5V STEP AND 5mV OVERDRIVE



# CMP-01

## APPLICATIONS INFORMATION

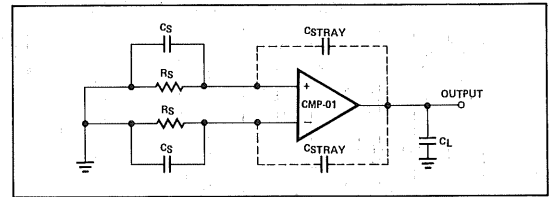
The CMP-01 provides fast response times even with small overdrives; to achieve this performance requires very high gain at high frequencies. The CMP-01 is completely free of oscillations; however, small values of stray capacitance from output to input when combined with high-source resistances can cause an unstable condition. DC characteristics are not affected, but when the input is within a few microvolts of the transition level, certain conditions can create an oscillation region. The width of this oscillatory region and the size of source resistance where oscillations begin is a strong function of the stray coupling present. The following suggestions are offered as a guide towards minimizing the conditions for oscillation: matched source resistors, minimized stray capacitances (e.g., a ground plane between output and input), or capacitive output loading ( $C_L$ ). The capacitive loading techniques will eliminate the oscillations, but result in slower response time. Matched bypass capacitors across the input resistors also can eliminate the instability,

$$\text{and if } C_S \geq 20\text{pF} \left( \frac{\text{maximum step size}}{\text{minimum overdrive}} \right)$$

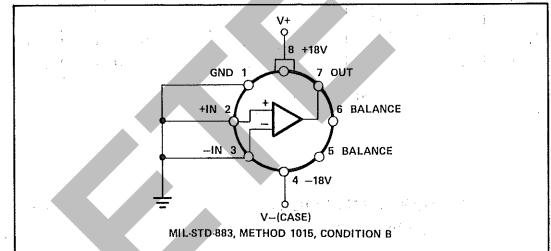
the response time will approximate the response time for low values of  $R_S$ . It should be noted that the offset nulling terminals do not require bypassing for stability. As with all

wideband circuits, it is recommended that the supplies be bypassed near the socket of the device.

## MINIMIZING OSCILLATION



## BURN-IN CIRCUIT



## 8-BIT TRACKING A/D CONVERTER

