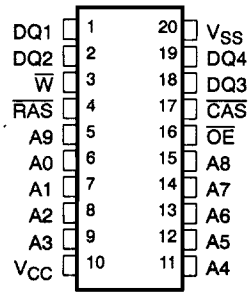
- **Processed to MIL-STD-883, Class B**
- **Military Temperature Range . . . −55 to 125°C**
- **Organization . . . 1 048 576 × 4**
- **Single 5-V Power Supply (±10% Tolerance)**
- **Performance Ranges:**

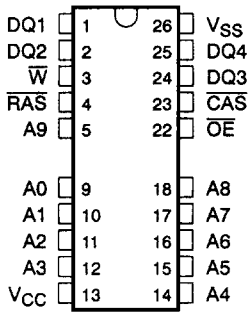
	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{CAC}) (MAX)	ACCESS TIME (t_{AA}) (MAX)	READ OR WRITE CYCLE (MIN)
SMJ44400-80	80 ns	20 ns	40 ns	150 ns
SMJ44400-10	100 ns	25 ns	50 ns	180 ns
SMJ44400-12	120 ns	30 ns	55 ns	210 ns

- **Enhanced Page Mode Operation for Faster Memory Access**
  - **Higher Data Bandwidth Than Conventional Page-Mode Parts**
  - **Random Single-Bit Access Within a Row With a Column Address**
- **$\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . . 1024-Cycle Refresh in 16 ms (Max)**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **Texas Instruments EPIC™ CMOS Process**
- **All Inputs/Outputs and Clocks are TTL Compatible**
- **Packaging Options:**
  - **400-mil 20/26-Leadless Ceramic SOLCC (HM Suffix)**
  - **20-Pin, 400-Mil Ceramic DIP (JD Suffix)**
  - **20-Pin Ceramic Flatpack (HR Suffix)**
  - **20-Pin Ceramic CSOJ**
  - **Additional Package Options Planned**

JD AND HR PACKAGES†
(TOP VIEW)



HM AND CSOJ PACKAGES†
(TOP VIEW)



† Packages are shown for pinout reference only.

PIN NOMENCLATURE	
A0–A9	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1–DQ4	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

description

The SMJ44400 series are high-speed 4 194 304-bit dynamic random-access memories, organized as 1 048 576 words of four bits each. They employ state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low-power operation.

The SMJ44400 features maximum row access time of 80 ns, 100 ns, and 120 ns. Maximum power dissipation is as low as 360 mW operating and 22 mW standby.

EPIC is a trademark of Texas Instruments Incorporated.

All inputs and outputs, including clocks, are compatible with Series 54 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The SMJ44400 is offered in a 400-mil 20/26-leadless ceramic surface mount SOLCC package (HM suffix), a 20-pin ceramic dual-in-line package (JD suffix), a 20-pin ceramic flatpack (HR suffix), and a 20-pin leaded ceramic chip carrier (CSOJ). All packages are characterized for operation from −55°C to 125°C.

operation

enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used. With minimum $\overline{CAS}$ page cycle time, all 1024 columns specified by column addresses A0 through A9 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the SMJ44400 to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as *enhanced page mode*. Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low), if t_{AA} max (access time from column address) has been satisfied. In the event that column addresses for the next cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of t_{CAC} or t_{CPA} (access time from rising edge of $\overline{CAS}$).

address (A0–A9)

Twenty address bits are required to decode 1 of 1 048 576 storage cell locations. Ten row-address bits are set up on inputs A0 through A9 and latched onto the chip by the row-address strobe ($\overline{RAS}$). The ten column-address bits are set up on pins A0 through A9 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the output buffer, as well as latching the address bits into the column-address buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle permitting a write operation independent of the state of $\overline{OE}$. This permits early write operation to be completed with $\overline{OE}$ grounded.

data in/out (DQ1–DQ4)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 54 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ and $\overline{OE}$ are brought low. In a read cycle the output becomes valid after all access times are satisfied. The output remains valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high-impedance state. This is accomplished by bringing $\overline{OE}$ high prior to applying data, thus satisfying t_{OED}.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers, putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state. Once in the low-impedance state, they will remain in the low-impedance state until either $\overline{OE}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every sixteen milliseconds to retain data. This can be achieved by strobing each of the1024 rows (A0–A9). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle. The external address is ignored during the hidden refresh cycles.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

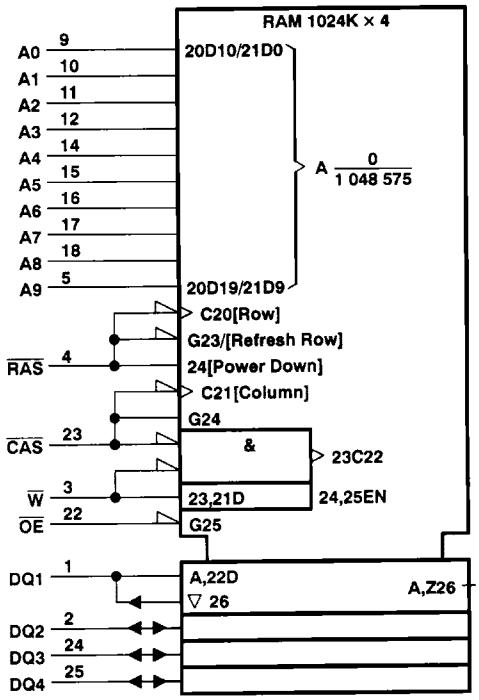
power up

To achieve proper device operation, an initial pause of 200 µs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. These eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$) cycle.

test mode

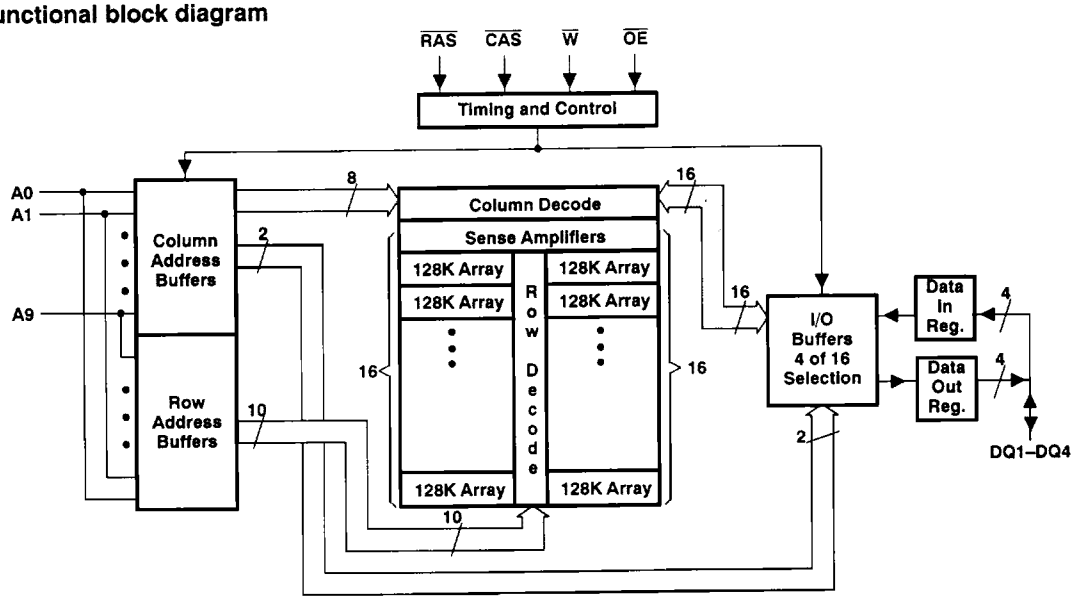
An industry standard Design For Test (DFT) mode is incorporated in the SMJ44400. A $\overline{CAS}$-before-$\overline{RAS}$ with $\overline{W}$ low (WCBR) cycle is used to enter test mode. In the test mode, data is written into and read from eight sections of the array in parallel. All data is written into the array through DQ1. Data is compared upon reading and if all bits are equal, all DQ pins will go high. If any one bit is different, all the DQ pins will go low. Any combination read, write, read-write, or page-mode can be used in the test mode. The test mode function reduces test times by enabling the 1M × 4 DRAM to be tested as if it were a 512K DRAM where column address 0 is not used. A $\overline{RAS}$-only or CBR refresh cycle is used to exit the DFT mode.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. The pinouts illustrated are for the HM package.

functional block diagram



absolute maximum ratings over operating temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) ..... – 1 V to 7 V
Voltage range on V_{CC} ..... – 1 V to 7 V
Short circuit output current ..... 50 mA
Power dissipation ..... 1 W
Operating temperature ..... – 55°C to 125°C
Storage temperature range ..... – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Min operating temperature	– 55			°C
T_C	Max operating case temperature			125	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'44400-80		'44400-10		'44400-12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		85		80		70	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V		4		4		4	mA
I_{CC3}	Average refresh current ($\overline{RAS}$-only, or $\overline{CBR}$)	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low, after $\overline{CAS}$ low (CBR)		85		75		65	mA
I_{CC4}	Average page current (see Note 4)	t_{PC} = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		50		40		35	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

capacitance over recommended ranges of supply voltage and operating temperature, f = 1 MHz (see Note 5)

	PARAMETER	MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			7	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			10	pF
$C_{i(W)}$	Input capacitance, write-enable input			10	pF
C_O	Output capacitance			10	pF

NOTE 5: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V. Capacitance is sampled only at initial design and after any major change.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

		'44400-80		'44400-10		'44400-12		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		40		45		55	ns
t_{CAC}	Access time from $\overline{CAS}$ low		20		25		30	ns
t_{CPA}	Access time from column precharge		45		50		55	ns
t_{RAC}	Access time from $\overline{RAS}$ low		80		100		120	ns
t_{OEA}	Access time from $\overline{OE}$ low		20		25		30	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)		20		25		30	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 6)		20		25		30	ns

NOTE 6: t_{OFF} and t_{OEZ} are specified when the output is no longer driven. The outputs are disabled by bringing either $\overline{OE}$ or $\overline{CAS}$ high.

timing requirements over recommended ranges of supply voltage and operating temperature

		'44400-80		'44400-10		'44400-12		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	150		180		210		ns
t_{RWC}	Read-write cycle time	205		245		285		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	50		60		65		ns
t_{PRWC}	Page-mode read-write cycle time	100		120		135		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	80	100 000	100	100 000	120	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	80	10 000	100	10 000	120	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 10)	20	10 000	25	10 000	30	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		15		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	60		70		80		ns
t_{WP}	Write pulse duration	15		20		25		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Data setup time (see Note 11)	0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	$\overline{W}$ low setup time before $\overline{CAS}$ high	20		25		30		ns
t_{RWL}	$\overline{W}$ low setup time before $\overline{RAS}$ high	20		25		30		ns
t_{WCS}	$\overline{W}$ low setup time before $\overline{CAS}$ low (Early write operation only)	0		0		0		ns
t_{WSR}	$\overline{W}$ high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	15		20		20		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low	60		75		90		ns
t_{DH}	Data hold time (see Note 11)	15		20		25		ns
t_{AR}	Column-address hold time after $\overline{RAS}$ low (see Note 10)	60		75		90		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		15		15		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 12)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 12)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (Early write operation only)	15		20		25		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 10)	60		75		90		ns
t_{WHR}	$\overline{W}$ high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{AWD}	Delay time, column-address to $\overline{W}$ low (Read-write operation only)	70		80		90		ns

Continued next page.

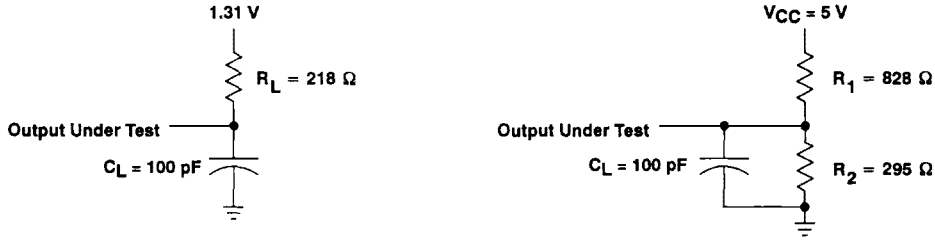
NOTES: 7. All cycle times assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
9. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
10. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
11. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating temperature

		'44400-80		'44400-10		'44400-12		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	20		20		25		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	80		100		120		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Read-write operation only)	50		60		70		ns
t_{OEH}	$\overline{OE}$ command hold time	20		25		30		ns
t_{OED}	$\overline{OE}$ to data delay	20		25		30		ns
t_{ROH}	$\overline{RAS}$ hold time referenced to $\overline{OE}$	20		25		30		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 13)	15	40	20	50	20	65	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	40		50		55		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	40		50		55		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 13)	20	60	25	75	25	90	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	20		25		30		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Read-write operation only)	110		135		160		ns
t_{REF}	Refresh time interval		16		16		16	ms
t_T	Transition time (see Note 15)							

NOTES: 13. Maximum value specified only to assure access time.
14. Valid data is presented at the outputs after all access times are satisfied but may go from three-state to an invalid data state prior to the specified access times as the outputs are driven when $\overline{CAS}$ goes low.
15. Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$ are to be a minimum of 3 ns and a maximum of 50 ns.

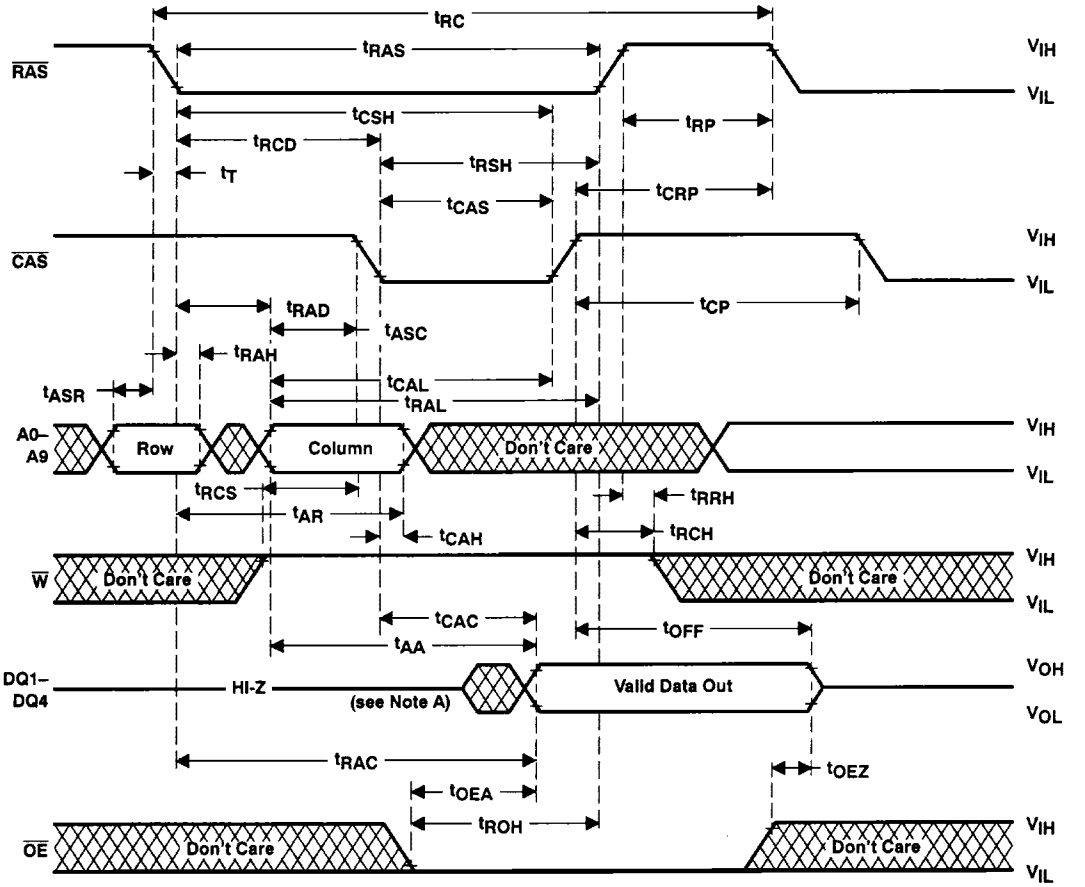
PARAMETER MEASUREMENT INFORMATION



(a) Load Circuit (b) Alternate Load Circuit

Figure 1. Load Circuits for Timing Parameters

PARAMETER MEASUREMENT INFORMATION



NOTE A: Valid data is presented at the outputs after all access times are satisfied but may go from three-state to an invalid data state prior to the specified access times as the outputs are driven when $\overline{CAS}$ goes low.

Figure 2. Read Cycle Timing

PARAMETER MEASUREMENT INFORMATION

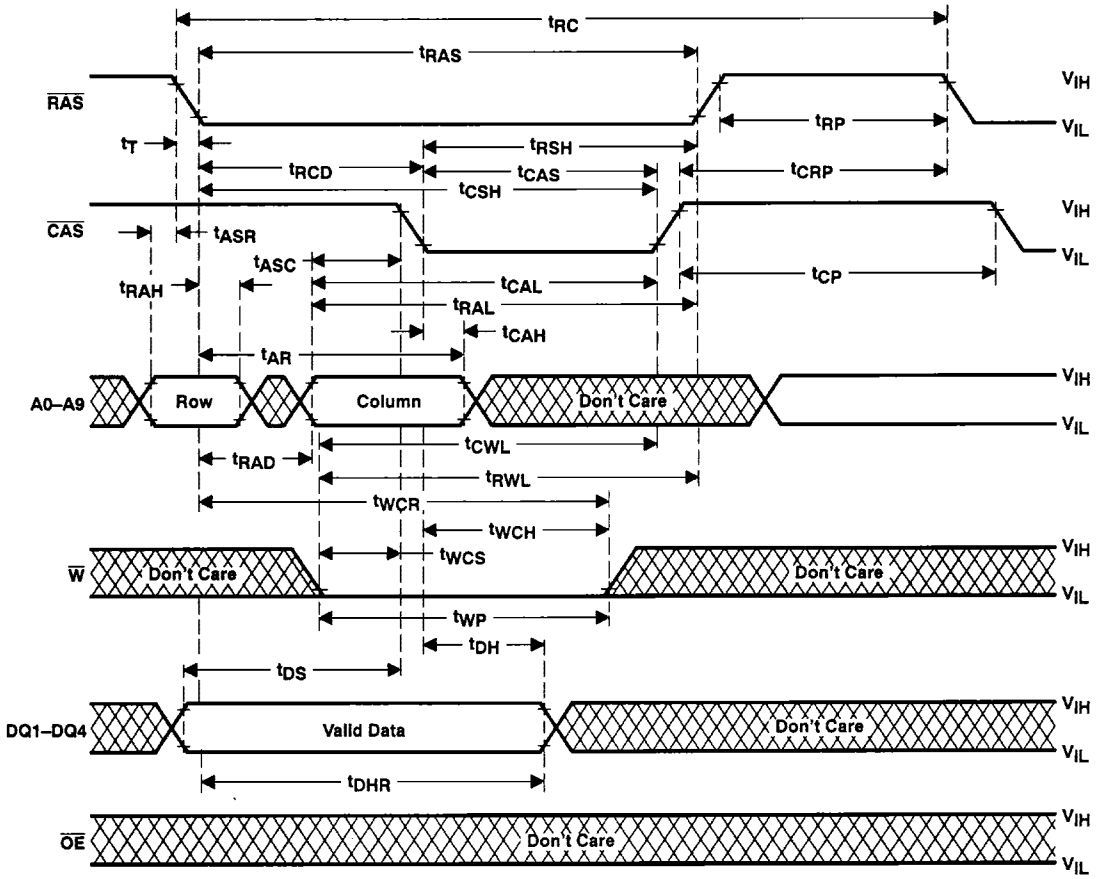


Figure 3. Early Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

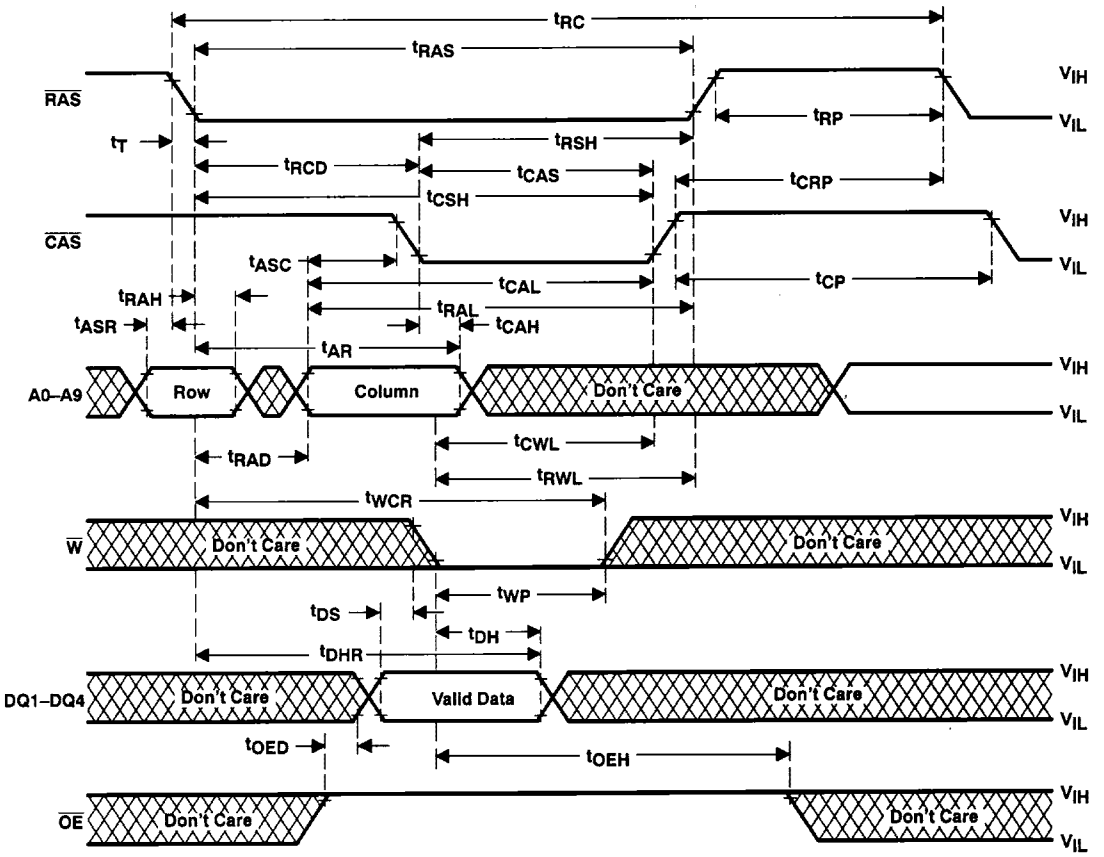
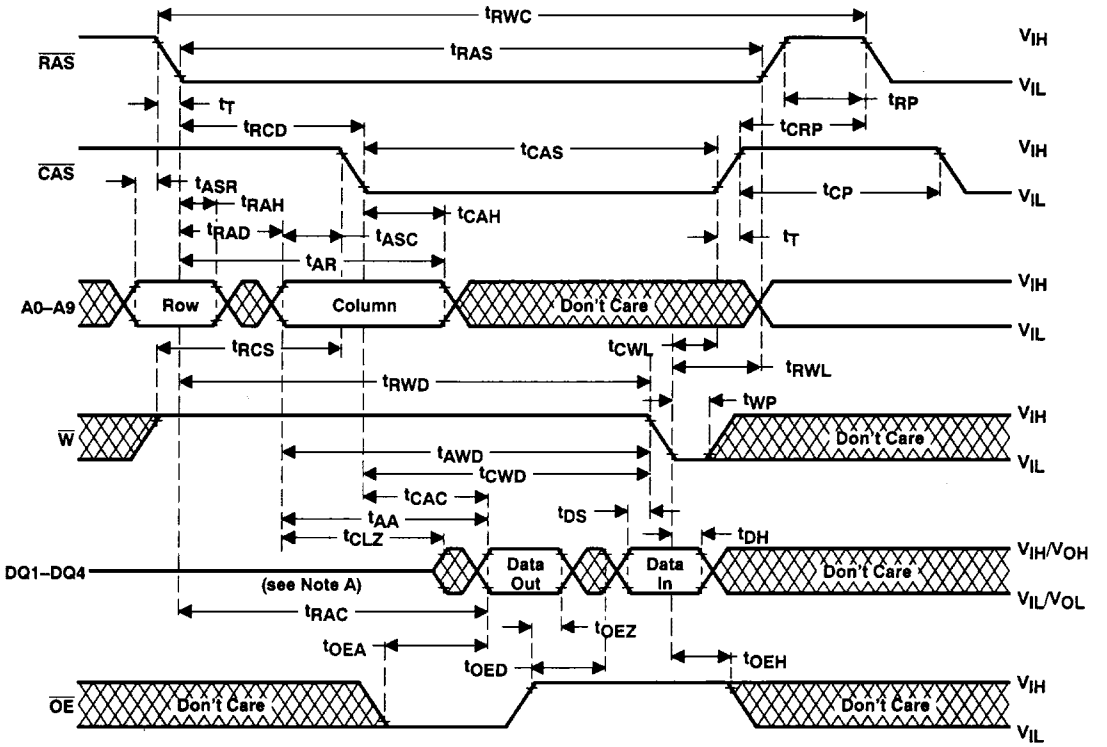


Figure 4. Write Cycle Timing

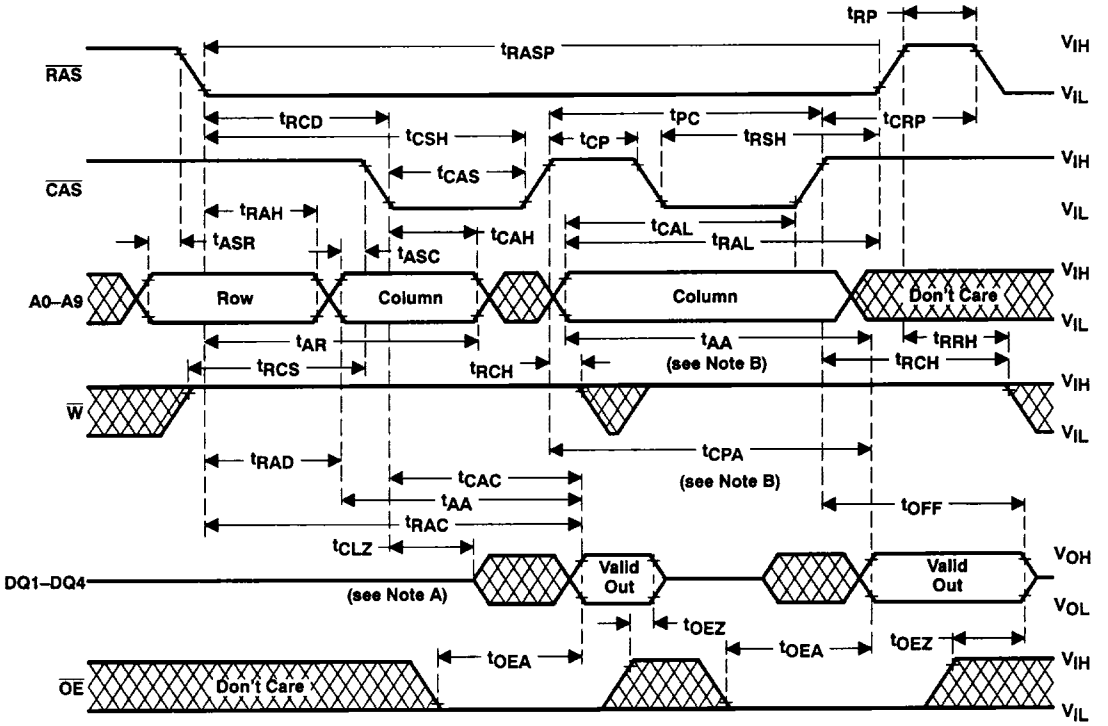
PARAMETER MEASUREMENT INFORMATION



NOTE A: Valid data is presented at the outputs after all access times are satisfied but may go from three-state to an invalid data state prior to the specified access times as the outputs are driven when $\overline{CAS}$ goes low.

Figure 5. Read-Write Cycle Timing

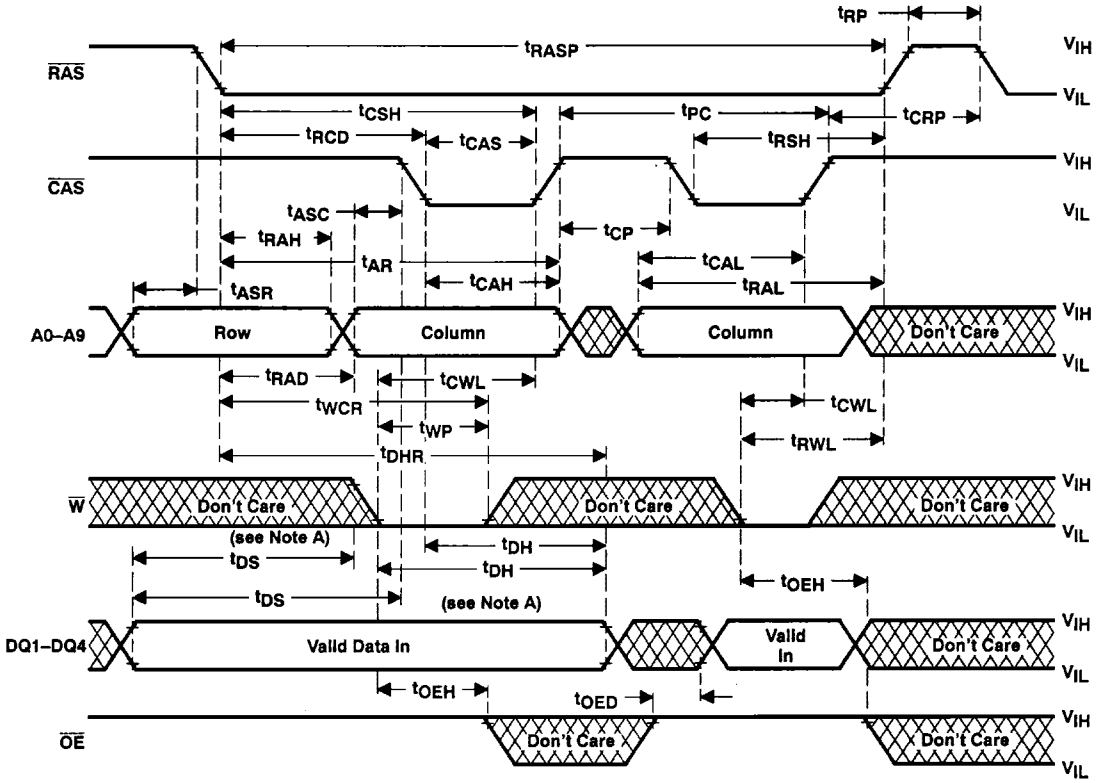
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Valid data is presented at the outputs after all access times are satisfied but may go from three-state to an invalid data state prior to the specified access times as the outputs are driven when $\overline{CAS}$ goes low.
B. Access time is t_{CPA} or t_{AA} dependent.

Figure 6. Enhanced Page-Mode Read Cycle Timing

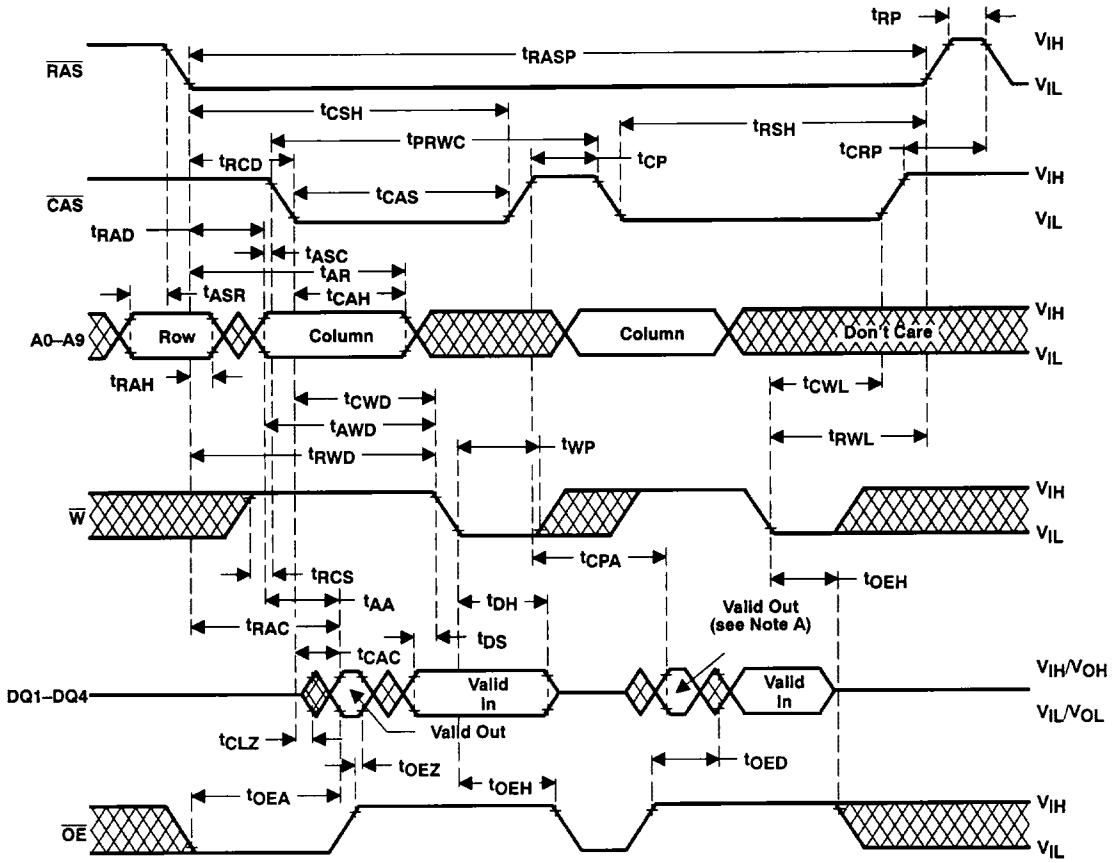
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.
B. A read cycle or a read-write cycle can be intermixed with write cycles as long as read and read-write timing specifications are not violated.

Figure 7. Enhanced Page-Mode Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION

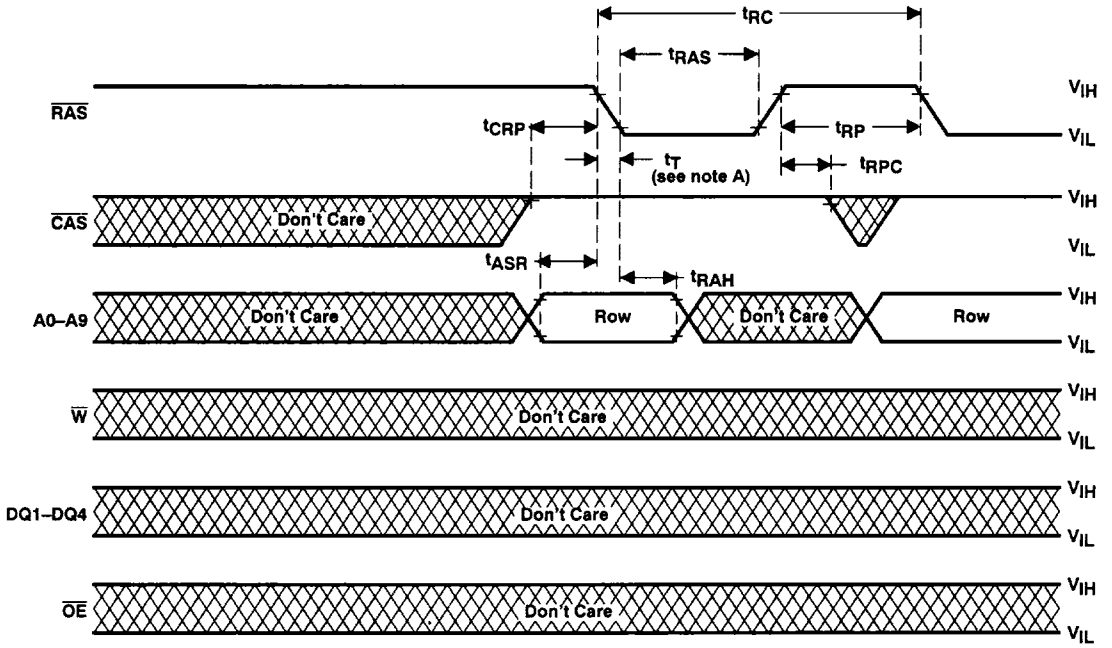


NOTES: A. Valid data is presented at the outputs after all access times are satisfied but may go from three-state to an invalid data state prior to the specified access times as the outputs are driven when $\overline{CAS}$ goes low.

B. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

Figure 8. Enhanced Page-Mode Read-Write Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTE A: Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$ are to be a minimum of 3 ns and a maximum of 50 ns.

Figure 9. $\overline{RAS}$-Only Refresh Timing

PARAMETER MEASUREMENT INFORMATION

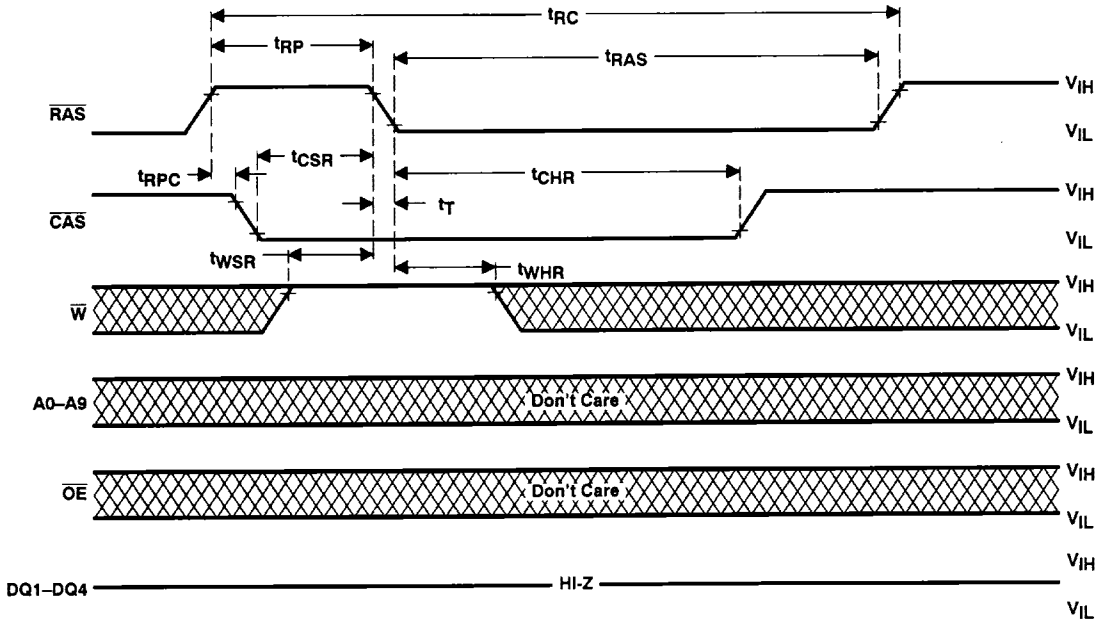
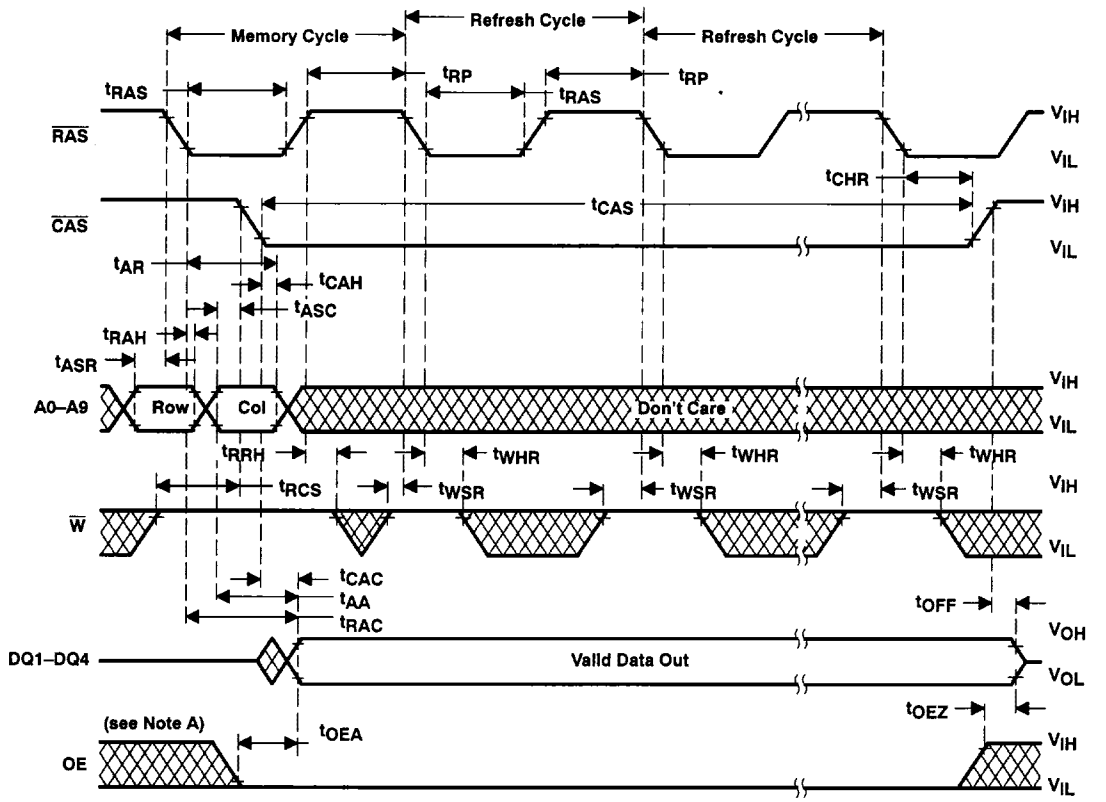


Figure 10. Automatic ($\overline{CAS}$-Before-$\overline{RAS}$) Refresh Cycle Timing

PARAMETER MEASUREMENT INFORMATION



NOTE A: Valid data is presented at the outputs after all access times are satisfied but may go from three-state to an invalid data state prior to the specified access times as the outputs are driven when $\overline{CAS}$ goes low.

Figure 11. Hidden Refresh Cycle (Read)

PARAMETER MEASUREMENT INFORMATION

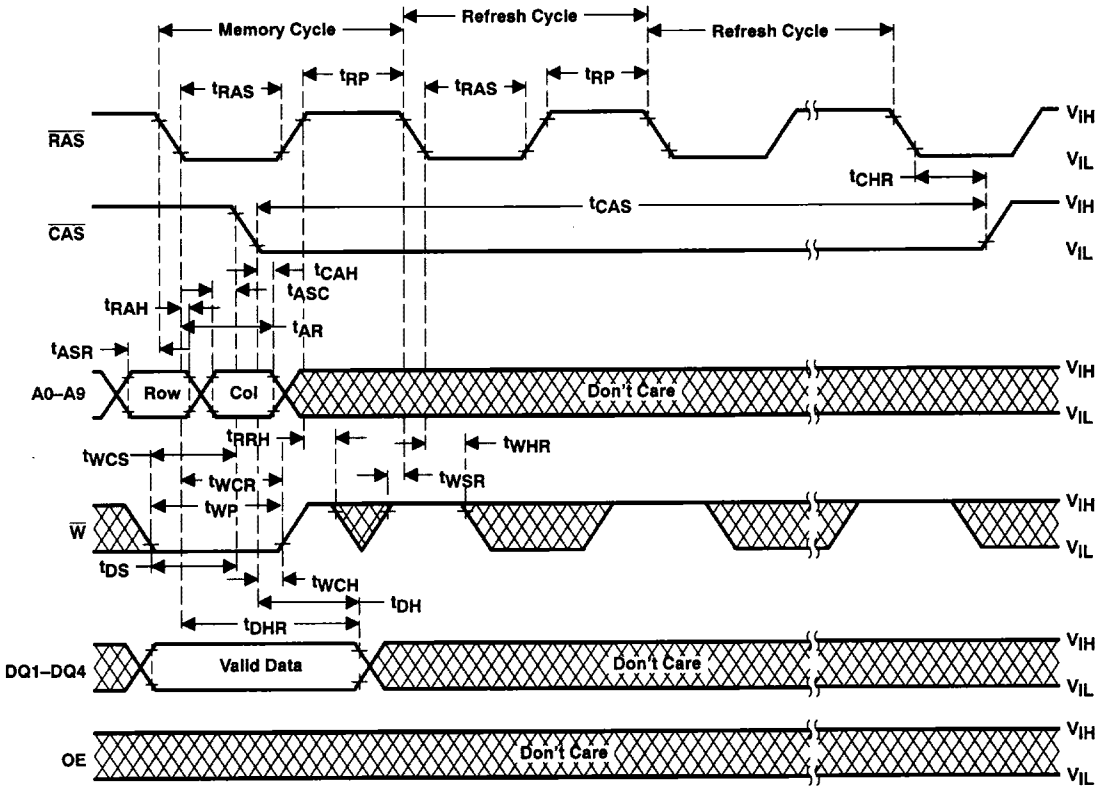


Figure 12. Hidden Refresh Cycle (Write)