FEATURES

- **JFET Switches Rather Than CMOS**
- **Low "ON" Resistance** .... **220Ω Typ**
- **Highly Resistant to Static Discharge Damage**
- **No SCR Latch-Up Problems**
- **Digital Inputs Compatible With TTL and CMOS**
- **125° C Temperature Tested Dice Available**
- **MUX-08 Pin Compatible With DG508, HI-508A, IH5108, IH6108, LF11508/12508/13508, AD7506**
- **MUX-24 Pin Compatible With DG509, HI-509A, IH5208, IH6208, LF11509/12509/13509, AD7507**
- **Available In Surface Mount Packages**
- **Available In Die Form**

ORDERING INFORMATION †

25°C ON RESISTANCE	CERDIP 16-PIN	PLASTIC 16-PIN	LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
		PACKAGE		
220Ω	MUX08AQ*	–	–	MIL
	MUX08EQ	–	–	IND
	–	MUX08EP	–	COM
300Ω	MUX08BQ*	–	MUX08BRC/883	MIL
	MUX08FQ	–	–	IND
	–	MUX08FP	–	XIND
	–	MUX08FS††	–	XIND
220Ω	MUX24AQ*	–	–	MIL
	MUX24EQ	–	–	IND
	–	MUX24EP	–	COM
300Ω	MUX24BQ*	–	–	MIL
	MUX24FQ	–	–	IND
	–	MUX24FP	–	XIND
	–	MUX24FS††	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages. For ordering information, see PMI's Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

The MUX-08 is a monolithic eight-channel analog multiplexer which connects a single output to one of the eight analog inputs depending upon the state of a 3-bit binary address.

The MUX-24 is a monolithic four-channel differential analog multiplexer configured in a double pole, four-position (plus OFF) electronic switch array. A two-bit binary input address connects a pair of independent analog inputs from each four-channel input section to the corresponding pair of independent analog outputs.
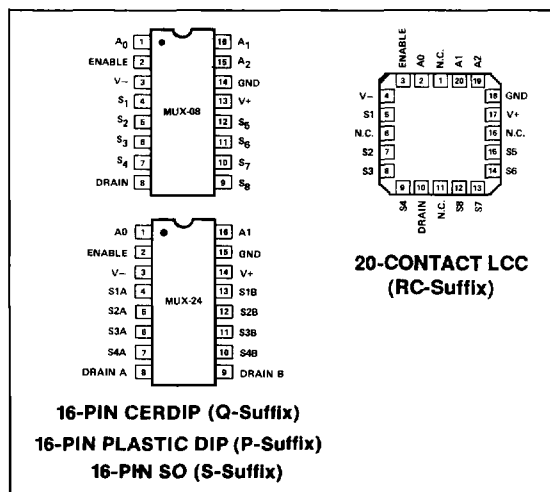
All switches in the MUX-08/MUX-24 are turned OFF by applying logic "0" to the ENABLE pin, thereby providing a package select function.

Fabricated with Precision Monolithics' high performance Bipolar-JFET technology, these devices offer low, constant "ON" resistance, low leakag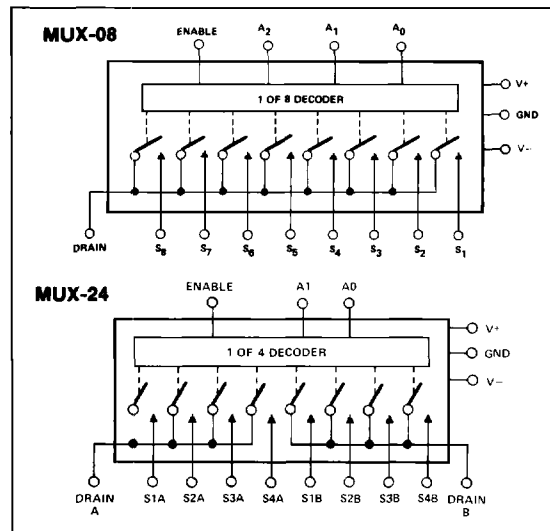e currents and fast settling time with low crosstalk to satisfy a wide variety of applications. These multiplexers do not suffer from latch-up or static charge blow-out problems associated with similar CMOS parts. The digital inputs are designed to operate from both TTL and CMOS levels while always providing a definite break-before-make action without the need for external pull-up resistors over the full operating temperature range.

For single sixteen-channel and dual eight-channel models, refer to the MUX-16/MUX-28 data sheet.

PIN CONNECTIONS

20-CONTACT LCC (RC-Suffix)

16-PIN CERDIP (Q-Suffix)

16-PIN PLASTIC DIP (P-Suffix)

16-PIN SO (S-Suffix)

FUNCTIONAL DIAGRAMS

MUX-08

MUX-24

ABSOLUTE MAXIMUM RATINGS (Note 1)

Operating Temperature Range

MUX-08/24-AQ, BQ, BRC	–55°C to +125°C
MUX-02/24-EQ, FQ	–25°C to +85°C
MUX-08/24-EP	0°C to +70°C
MUX-08/24-FP, FS	–40°C to +85°C
Junction Temperature (T_J)	–65°C to +150°C
Storage Temperature Range	–65°C to +150°C
P-Suffix	–65°C to +125°C
Lead Temperature (Soldering, 60 sec)	300°C
Maximum Junction Temperature	150°C
V+ Supply to V– Supply	36V
Logic Input Voltage	(–4V or V–) to V+ Supply

Analog Input Voltage .... V– Supply –20V to V+ Supply +20V
Maximum Current Through Any Pin 25mA

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
16-Pin Hermetic DIP (Q)	100	16	°C/W
16-Pin Plastic DIP (P)	82	39	°C/W
20-Contact LCC (RC)	98	38	°C/W
16-Pin SO (S)	111	35	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V+ = +15V, V– = –15V and T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		MUX-08A/E MUX-24A/E MIN	TYP	MAX	MUX-08B/F MUX-24B/F MIN	TYP	MAX	UNITS
"ON" Resistance	R_{ON}	$V_S \leq 10V$, $I_S \leq 200\mu A$		—	220	300	—	300	400	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \leq V_S \leq 10V$, $I_S = 200\mu A$		—	1	5	—	3	7	%
R_{ON} Match Between Switches	R_{ON} Match	$V_S = 0V$, $I_S = 200\mu A$		—	7	15	—	9	20	%
Analog Voltage Range	V_A	(Note 6)		+10 / –10	+10.4 / –15	— / —	+10 / –10	+10.4 / –15	— / —	V
Source Current (Switch "OFF")	$I_{S (OFF)}$	$V_S = 10V$, $V_D = -10V$ (Note 1)		—	0.01	1.0	—	0.01	2.0	nA
Drain Current (Switch "OFF")	$I_{D (OFF)}$	$V_S = 10V$, $V_D = -10V$ (Note 1)	MUX-08	—	0.1	1.0	—	0.1	2.0	nA
			MUX-24	—	0.05	1.0	—	0.05	2.0	
Leakage Current (Switch "ON")	$I_{D (ON)}$ $+I_{S (ON)}$	$V_D = 10V$ (Note 1)	MUX-08	—	0.1	1.0	—	0.1	2.0	nA
			MUX-24	—	0.05	1.0	—	0.05	2.0	
Digital Input Current	I_{IN}	$V_{IN} = 0.4V$ to 15V		—	1	10	—	1	10	μA
Digital "0" Enable Current	$I_{INL (EN)}$	$V_{EN} = 0.4V$		—	4	10	—	4	10	μA
Digital Input Capacitance	C_{DIG}			—	3	—	—	3	—	pF
Switching Time (t_{TRAN})	t_{PHL} t_{PLH}	(Notes 2, 5) Figure 1 (Test Circuit)		— / —	1.5 / 1.0	2.1 / 1.3	— / —	1.5 / 1.0	2.1 / 1.3	μs
Output Settling Time	t_S	10V Step to 0.10% / 10V Step to 0.05% / 10V Step to 0.02%		— / — / —	2.2 / 2.7 / 3.4	— / — / —	— / — / —	2.2 / 2.7 / 3.4	— / — / —	μs
Break-Before-Make Delay	t_{OPEN}	Figure 3 (Test Circuit)		—	0.8	—	—	1.0	—	μs
Enable Delay "ON"	$t_{ON (EN)}$	(Note 5) Figure 2 (Test Circuit)		—	1	2	—	1	2	μs
Enable Delay "OFF"	$t_{OFF (EN)}$	(Note 5) Figure 2 (Test Circuit)	MUX-08	—	0.1	0.4	—	0.2	0.4	μs
			MUX-24	—	0.2	0.5	—	0.3	0.6	
"OFF" Isolation	ISO_{OFF}	(Note 4) Figure 5 (Test Circuit)	MUX-08	—	60	—	—	60	—	dB
			MUX-24	—	66	—	—	66	—	
Crosstalk	CT	(Note 3) Figure 4 (Test Circuit)	MUX-08	—	70	—	—	70	—	dB
			MUX-24	—	76	—	—	76	—	
Source Capacitance	$C_{S (OFF)}$	Switch "OFF", $V_S = 0V$, $V_D = 0V$	MUX-08	—	2.5	—	—	2.5	—	pF
			MUX-24	—	2	—	—	2	—	
Drain Capacitance	$C_{D (OFF)}$	Switch "OFF", $V_S = 0V$, $V_D = 0V$	MUX-08	—	7	—	—	7	—	pF
			MUX-24	—	4	—	—	4	—	
Input to Output Capacitance	$C_{DS (OFF)}$	(Note 4)	MUX-08	—	0.3	—	—	0.3	—	pF
			MUX-24	—	0.15	—	—	0.15	—	
Positive Supply Current All Digital Inputs Logic "0" or "1"	I+	V+ = 15V / V+ = 5V		— / —	10 / 8	12 / —	— / —	6 / 5	12 / —	mA
Negative Supply Current All Digital Inputs Logic "0" or "1"	I–	V+ = –15V / V+ = –5V		— / —	3.0 / 2.5	3.8 / —	— / —	2.0 / 1.8	3.8 / —	mA

ANALOG SWITCHES/MULTIPLEXERS

13

ELECTRICAL CHARACTERISTICS at V+ = 15V, V− = −15V and −55°C ≤ T$_A$ ≤ 125°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		MUX-08A/ MUX-24A			MUX-08B/ MUX-24B		UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
"ON" Resistance	R$_{ON}$	V$_S$ ≤ 10V, I$_S$ ≤ 200µA	—	—	400	—	—	500	Ω
ΔR$_{ON}$ With Applied Voltage	ΔR$_{ON}$	−10V ≤ V$_S$ ≤ 10V, I$_S$ = 200µA	—	1.5	—	—	4.5	—	%
R$_{ON}$ Match Between Switches	R$_{ON}$ Match	V$_S$ = 0V, I$_S$ = 200µA	—	10	—	—	15	—	%
Analog Voltage Range	V$_A$	(Note 6)	+10 −10	+10.4 −15	— —	+10 −10	+10.4 −15	— —	V
Source Current (Switch "OFF")	I$_{S (OFF)}$	V$_S$ = 10V, V$_D$ = −10V (Notes 1, 7)	—	—	25	—	—	50	nA
Drain Current (Switch "OFF")	I$_{D (OFF)}$	V$_S$ = 10V, V$_D$ = −10V (Notes 1, 7) MUX-08 MUX-24	— —	— —	100 50	— —	— —	500 500	nA
Leakage Current (Switch "ON")	I$_{D (ON)}$ +I$_{S (ON)}$	V$_D$ = 10V (Notes 1, 7) MUX-08 MUX-24	— —	— —	100 50	— —	— —	500 500	nA
Digital "1" Input Voltage	V$_{INH}$	(Note 6)	2	—	—	2	—	—	V
Digital "0" Input Voltage	V$_{INL}$	(Note 6)	—	—	0.7	—	—	0.7	V
Digital Input Current	I$_{IN}$	V$_{IN}$ = 0.4V to 15V	—	—	20	—	—	20	µA
Digital "0" Enable Current	I$_{INL (EN)}$	V$_{EN}$ = 0.4V	—	—	20	—	—	20	µA
Positive Supply Current	I+	All Digital Inputs Logic "0" or "1"	—	—	15	—	—	15	mA
Negative Supply Current	I−	All Digital Inputs Logic "0" or "1"	—	—	5	—	—	5	mA
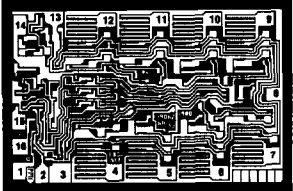
ELECTRICAL CHARACTERISTICS at V+ = 15V, V− = −15V and −25°C ≤ T$_A$ +85°C for MUX-08EQ/FQ and MUX-24EQ/FC 0°C ≤ T$_A$ ≤ +70°C for MUX-08EP and MUX-24EP; −40°C ≤ T$_A$ ≤ +85°C for MUX-08FP/FS and MUX-24FP/FS, unless otherwise noted

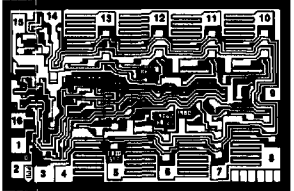| PARAMETER	SYMBOL	CONDITIONS		MUX-08E/ MUX-24E			MUX-08F/ MUX-24F		UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
"ON" Resistance	R$_{ON}$	V$_S$ ≤ 10V, I$_S$ ≤ 200µA	—	—	400	—	—	500	Ω
ΔR$_{ON}$ With Applied Voltage	ΔR$_{ON}$	−10V ≤ V$_S$ ≤ 10V, I$_S$ = 200µA	—	1.5	—	—	4.5	—	%
R$_{ON}$ Match Between Switches	R$_{ON}$ Match	V$_S$ = 0V, I$_S$ = 200µA	—	10	—	—	15	—	%
Analog Voltage Range	V$_A$	(Note 6)	+10 −10	+10.4 −15	— —	+10 −10	+10.4 −15	— —	V
Source Current (Switch "OFF")	I$_{S (OFF)}$	V$_S$ = 10V, V$_D$ = −10V (Notes 1, 7)	—	—	10	—	—	10	nA
Drain Current (Switch "OFF")	I$_{D (OFF)}$	V$_S$ = 10V, V$_D$ = −10V (Notes 1, 7) MUX-08 MUX-24	— —	— —	100 50	— —	— —	100 50	nA
Leakage Current (Switch "ON")	I$_{D (ON)}$ +I$_{S (ON)}$	V$_D$ = 10V (Notes 1, 7) MUX-08 MUX-24	— —	— —	100 50	— —	— —	100 50	nA
Digital "1" Input Voltage	V$_{INH}$	(Note 6)	2	—	—	2	—	—	V
Digital "0" Input Voltage	V$_{INL}$	(Note 6)	—	—	0.8	—	—	0.8	V
Digital Input Current	I$_{IN}$	V$_{IN}$ = 0.4V to 15V	—	—	20	—	—	20	µA
Digital "0" Enable Current	I$_{INL (EN)}$	V$_{EN}$ = 0.4V	—	—	20	—	—	20	µA
Positive Supply Current	I+	All Digital Inputs Logic "0" or "1"	—	—	15	—	—	15	mA
Negative Supply Current	I−	All Digital Inputs Logic "0" or "1"	—	—	5	—	—	5	mA

NOTES:
1. Conditions applied to leakage tests insure worst case leakages. Exceeding 11V on the analog input may cause an "OFF" channel to turn "ON"
2. R$_L$ = 10MΩ, C$_L$ = 10pF.
3. Crosstalk is measured by driving channel 8 with channel 4 "ON". R$_L$ = 1MΩ, C$_L$ = 10pF, V$_S$ = 5V RMS, f = 500kHz
4. "OFF" isolation is measured by driving channel 8 with ALL channels "OFF" R$_L$ = 1kΩ, C$_L$ = 10pF, V$_S$ = 5V RMS, f = 500kHz. C$_{DS}$ is computed from t OFF isolation measurement.
5. Sample tested.
6. Guaranteed by leakage current and R$_{ON}$ tests.
7. Leakage tests are performed only on military temperature grades at 125°

8/89, Rev.

DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)

MUX-08   **MUX-24**

DIE SIZE 0.093 × 0.059 inch, 5487 sq. mils
(2.362 × 1.500 mm, 3543 sq. mm)

1. A0	9. S8	1. A0	9. DRAIN B
2. ENABLE	10. S7	2. ENABLE	10. S4 B
3. V− (SUBSTRATE)	11. S6	3. V− (SUBSTRATE)	11. S3 B
4. S1	12. S5	4. S1 A	12. S2 B
5. S2	13. V+	5. S2 A	13. S1 B
6. S3	14. GND	6. S3 A	14. V+
7. S4	15. A2	7. S4 A	15. GND
8. DRAIN	16. A1	8. DRAIN A	16. A1

For additional DICE ordering information,
refer to 1990/91 Data Book, Section 2.

WAFER TEST LIMITS at V+ = 15V, V− = −15V, T_A = 25° C, unless otherwise noted. (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MUX-08/ MUX-24NT LIMIT	MUX-08/ MUX-24N LIMIT	MUX-08/ MUX-24G LIMIT	UNITS
"ON" Resistance	R_{ON}	V_S = 0V, I_S = 200µA	T_A = 125° C	300 400	300 —	400 —	Ω MAX
Digital "1" Input Voltage	V_{INH}	(Note 2)		2	2	2	V MIN
Digital "0" Input Voltage	V_{INL}	(Note 2)		0.8	0.8	0.8	V MAX
Digital "0" Input Current	I_{INL}	V_{IN} = 0.4V	T_A = 125° C	10 20	10 —	10 —	µA MAX
Digital "0" Enable Current	$I_{INL(EN)}$	V_{IN} = 0.4V	T_A = 125° C	10 20	10 —	10 —	µA MAX
Positive Supply Current (All Digital Inputs Logic "0")	I+		T_A = 125° C	12 15	12 —	12 —	mA MAX
Negative Supply Current (All Digital Inputs Logic "0")	I−		T_A = 125° C	3.8 5	3.8 —	3.8 —	mA MAX
Analog Input Range	V_A	(Note 2)		±10	±10	±10	V MIN

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly mehtods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at V+ = 15V, V− = −15V and T_A = 25° C for MUX-08/24N & G, T_A = 125° C for MUX-08/24NT, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MUX-08/ MUX-24NT TYPICAL	MUX-08/ MUX-24N TYPICAL	MUX-08/ MUX-24G TYPICAL	UNITS
Switching Time (t_{TRAN})	t_{PHL} t_{PLH}	(Note 1)	1.7 1.1	1.3 0.9	2.1 1.3	µs
Output Settling Time	t_S	10V Step to 0.1% (Note 1)	2.1	1.5	1.9	µs
Break-Before-Make Delay	t_{OPEN}	(Note 1)	0.8	0.8	1.0	µs
Crosstalk	CT	Note 1	70	70	70	dB
R_{ON} With Applied Voltage	ΔR_{ON}	−10V ≤ V_S ≤ 10V, I_S = 200µA	2	2	6	%
Leakage Current (Switch "ON")	$I_{D(ON)}$	V_D = 10V (Note 1)	20	0.5	0.5	nA
Analog Input Range	V_A		+ 10.4/−15	+ 10.4/−15	+ 10.4/−15	V

NOTES:
The data shown is extrapolated from measurements made on the packaged devices.

2. Guaranteed by leakage current and R_{ON} tests.
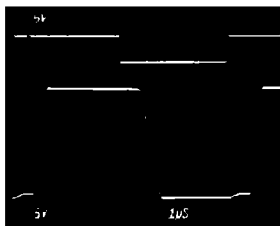
MUX-08 LOGIC STATE

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

MUX-24 LOGIC STATE

A_1	A_0	EN	"ON" CHANNEL
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

TYPICAL PERFORMANCE CHARACTERISTICS (Applies to all grades, unless otherwise noted.)

MUX-08 BREAK-BEFORE-MAKE SWITCHING
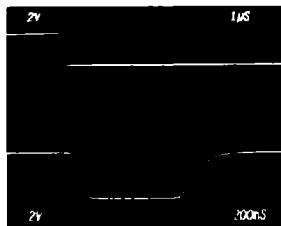
R_L = 1kΩ, C_L = 10pF, $V_{1, 8}$ = 10V
VOLTAGE = 2V/DIV
TIME = 200ns/DIV

MUX-08 LARGE-SIGNAL SWITCHING

R_L= 1MΩ, C_L = 10pF, V_1 = −10V, V_8 = +10V
VOLTAGE = 5V/DIV
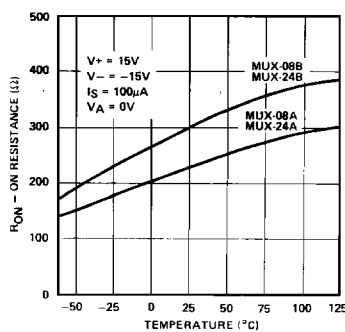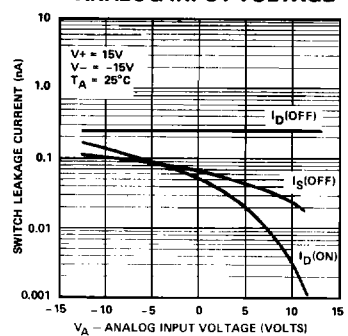TIME = 1μs/DIV

MUX-08 SMALL-SIGNAL SWITCHING
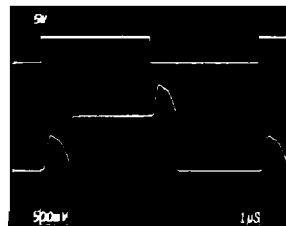
R_L = 1MΩ, C_L = 10pF, V_1 = −500mV, V_8 = +500mV
VOLTAGE = 500mV/DIV
TIME = 1μs/DIV

MUX-08 SMALL-SIGNAL SWITCHING WITH FILTERING
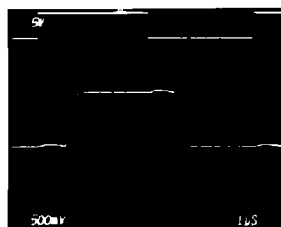
R_L = 1MΩ, C_L = 500pF, V_1 = 500mV, V_8 = +500mV
VOLTAGE = 500mV/DIV
TIME = 1μs/DIV

MUX-08 SMALL-SIGNAL SWITCHING WITH 2μs SAMPLE TIME
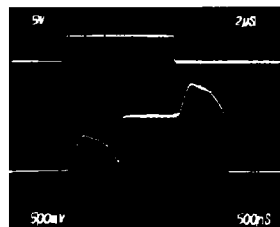
R_L = 1MΩ, C_L = 10pF, V_1 = −500mV, V_8 = +500mV
VOLTAGE = 500mV/DIV
TIME = 500ns/DIV

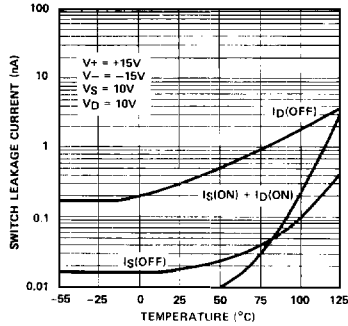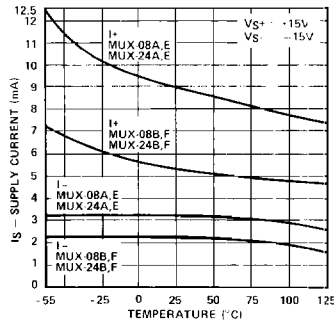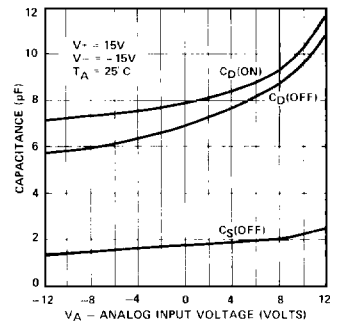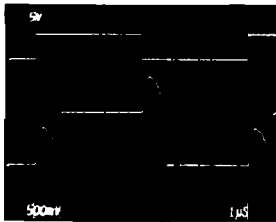### MUX-08 SMALL-SIGNAL SWITCHING WITH FILTERING AND 2.5μs SAMPLE TIME

R_L = 1MΩ, C_L = 500pF, V_1 = −500mV, V_8 = +500m
VOLTAGE = 500mV/DIV
TIME = 500ns/DIV

NOTE:
Top waveforms: Digital Input 5V/DIV
Bottom waveforms: Multiplexer Output

8/89, Rev. A

TYPICAL PERFORMANCE CHARACTERISTICS (Applies to all grades, unless otherwise noted.)

MUX-08 CROSSTALK AND OFF ISOLATION PERFORMANCE OF CHANNEL 8

EPOXY (P) PACKAGE

$V(+) = +15V$
$V(-) = -15V$
$T_A = 25°C$
CROSSTALK:
$R_L = 1MΩ$, $C_L = 10pF$, $V_S = +5V$ RMS
OFF ISOLATION:
$R_L = 1kΩ$, $C_L = 10pF$, $V_S = +5V$ RMS

CROSSTALK
OFF ISOLATION

$V_S \div V_D$ – OFF ISOLATION OR CROSSTALK (dB)
FREQUENCY (Hz)

MUX-08 CROSSTALK AND OFF ISOLATION PERFORMANCE OF CHANNEL 8

CERAMIC (Q) PACKAGE

$V(+) = +15V$
$V(-) = -15V$
$T_A = 25°C$
CROSSTALK:
$R_L = 1MΩ$, $C_L = 10pF$, $V_S = +5V$ RMS
OFF-ISOLATION:
$R_L = 1kΩ$, $C_L = 10pF$, $V_S = +5V$ RMS
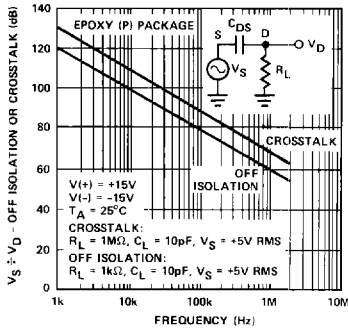
CROSSTALK
OFF ISOLATION

$V_S \div V_D$ – OFF-ISOLATION OR CROSSTALK (dB)
FREQUENCY (Hz)
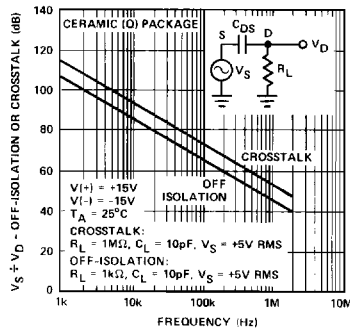
TRANSITION TIMES vs TEMPERATURE

$V+ = 15V$
$V- = -15V$
$R_L = 10MΩ$
$C_L = 10pF$

MUX-08B,F MUX-24B,F
MUX-08A,E MUX-24A,E

TIME (μsec)
TEMPERATURE (°C)
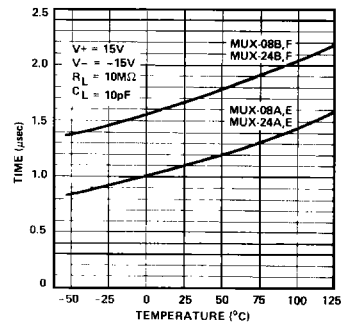
ENABLE DELAY TIMES vs TEMPERATURE

$V+ = +15V$
$V- = -15V$
$V_{S2} - V_{S8} = 0V$
$R_L = 1kΩ$
MUX-08A, E
$V_{S1} = 10V$
MUX-08B, F
$V_{S1} = 2V$

MUX-08B,F MUX-24B,F t_{ON}
MUX-08A,E MUX-24A,E t_{ON}
MUX-08B,F MUX-24B,F t_{OFF}
MUX-08A,E; MUX-24A,E t_{OFF}

TIME (μsec)
TEMPERATURE (°C)
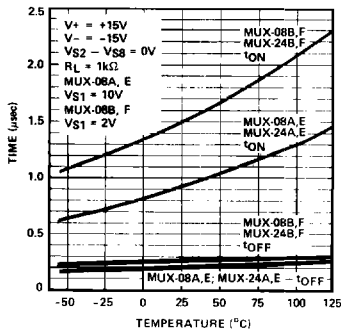
"ON" RESISTANCE (R_{ON}) vs ANALOG VOLTAGE (V_A)

$I_S = 200\mu A$ MUX-08B,F MUX-24B,F
$I_S = 200\mu A$ MUX-08A,E MUX-24A,E

$V+ = +15V$
$V- = -15V$
$T_A = 25°C$

R_{ON} – ON RESISTANCE (Ω)
V_A – ANALOG INPUT VOLTAGE (VOLTS)
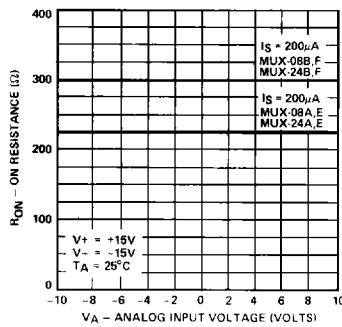
R_{ON} vs SWITCH VOLTAGE (V_{SD})

$V+ = +15V$
$V- = -15V$
$T_A = 25°C$

MUX-08B,F MUX-24B,F
MUX-08A,E MUX-24A,E

R_{ON} – ON RESISTANCE (Ω)
V_S – SWITCH VOLTAGE (mV)

R_{ON} vs SWITCH CURRENT (I_S)

$V+ = 15V$
$V- = -15V$
$T_A = 25°C$

MUX-08B,F MUX-24B,F
MUX-08A,E MUX-24A,E

I_S – SWITCH CURRENT (μA)

R_{ON} vs TEMPERATURE

$V+ = 15V$
$V- = -15V$
$I_S = 100\mu A$
$V_A = 0V$

MUX-08B MUX-24B
MUX-08A MUX-24A

R_{ON} – ON RESISTANCE (Ω)
TEMPERATURE (°C)
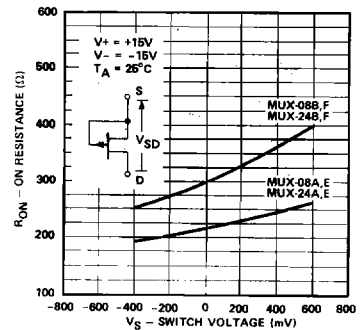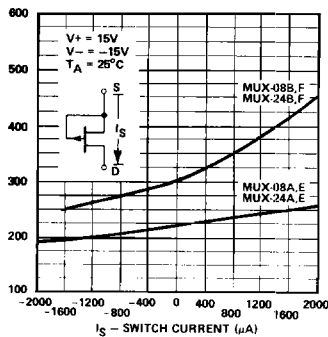
SWITCH LEAKAGE CURRENTS vs ANALOG INPUT VOLTAGE

$V+ = 15V$
$V- = -15V$
$T_A = 25°C$

$I_{D(OFF)}$
$I_{S(OFF)}$
$I_{D(ON)}$

SWITCH LEAKAGE CURRENT (nA)
V_A – ANALOG INPUT VOLTAGE (VOLTS)

ANALOG SWITCHES/MULTIPLEXERS

13

TYPICAL PERFORMANCE CHARACTERISTICS (Applies to all grades, unless otherwise noted.)

SWITCH LEAKAGE CURRENTS vs TEMPERATURE

SUPPLY CURRENTS vs TEMPERATURE

MUX-08 SWITCH CAPACITANCES vs ANALOG INPUT VOLTAGE
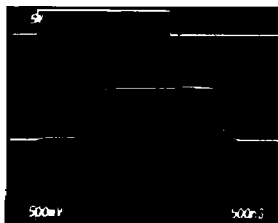

MUX-24 SMALL-SIGNAL SWITCHING

$R_L = 1M\Omega$, $C_L = 10pF$, $V_1 = -500mV$,
$V_4 = +500mV$
VOLTAGE = 500mV/DIV, TIME = 1µs/DIV

### MUX-24 SMALL-SIGNAL SWITCHING WITH FILTERING

$R_L = 1M\Omega$, $C_L = 500pF$, $V_1 = -500mV$,
$V_4 = +500mV$
VOLTAGE = 500mV/DIV, TIME = 1µs/DIV

MUX-24 SMALL-SIGNAL SWITCHING WITH 2µs SAMPLE TIME
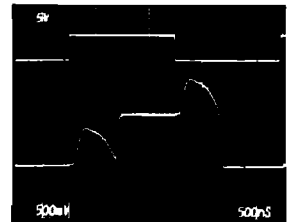
$R_L = 1M\Omega$, $C_L = 10pF$, $V_1 = -500mV$,
$V_4 = +500mV$
VOLTAGE = 500mV/DIV, TIME = 500ns/DIV

MUX-24 SMALL-SIGNAL SWITCHING WITH FILTERING AND 2.5µs SAMPLE TIME

$R_L = 1M\Omega$, $C_L = 500pF$, $V_1 = -500mV$,
$V_4 = +500mV$
VOLTAGE = 500mV/DIV, TIME = 500ns/DIV

MUX-24 BREAK-BEFORE-MAKE SWITCHING
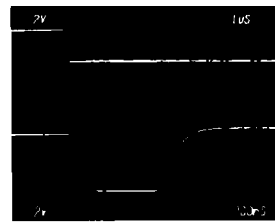
$R_L = 1k\Omega$, $C_L = 10pF$, $V_{1,4} = 10V$
VOLTAGE = 2V/DIV, TIME = 200ns/DIV

MUX-24 LARGE-SIGNAL SWITCHING
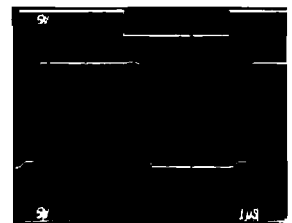
$R_L = 1M\Omega$, $C_L = 10pF$, $V_1 = -10V$, $V_4 = +10V$
VOLTAGE = 5V/DIV, TIME = 1µs/DIV

NOTE:
Top waveforms: Digital Input 5V/DIV
Bottom waveforms: Multiplexer Output

TYPICAL PERFORMANCE CHARACTERISTICS (Applies to all grades, unless otherwise noted.)

DIGITAL INPUT CURRENTS vs TEMPERATURE

MUX-24 SWITCH CAPACITANCES vs ANALOG INPUT VOLTAGE

MUX-24 CROSSTALK AND OFF ISOLATION PERFORMANCE OF CHANNEL 3A
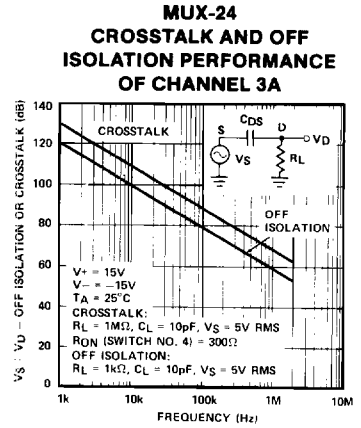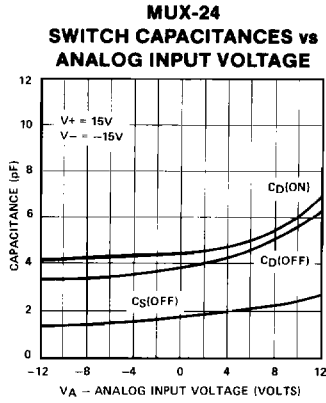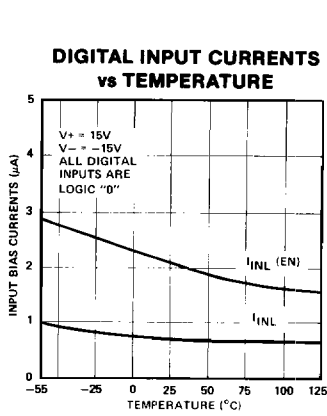
A.C. TEST CIRCUITS

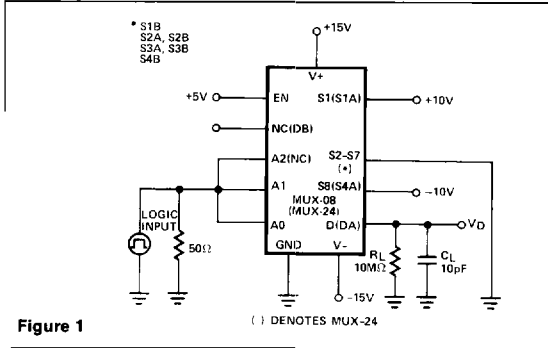### TRANSITION TIME TEST CIRCUIT

Figure 1
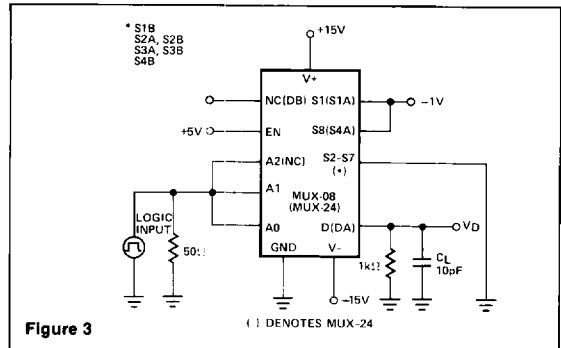
BREAK-BEFORE-MAKE TEST CIRCUIT
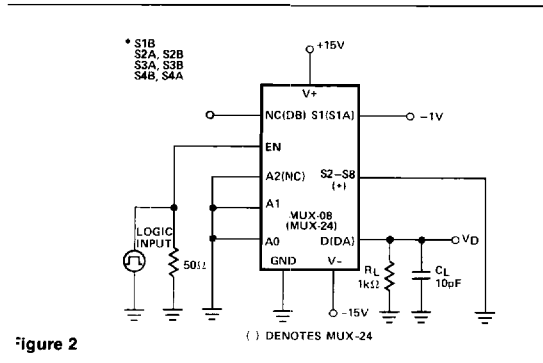

Figure 3

ENABLE DELAY TIME TEST CIRCUIT

Figure 2

CROSSTALK MEASUREMENT CIRCUIT
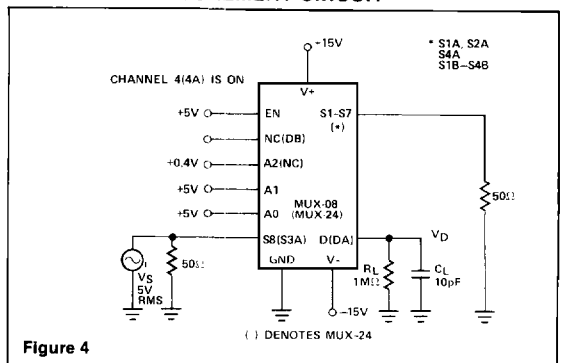
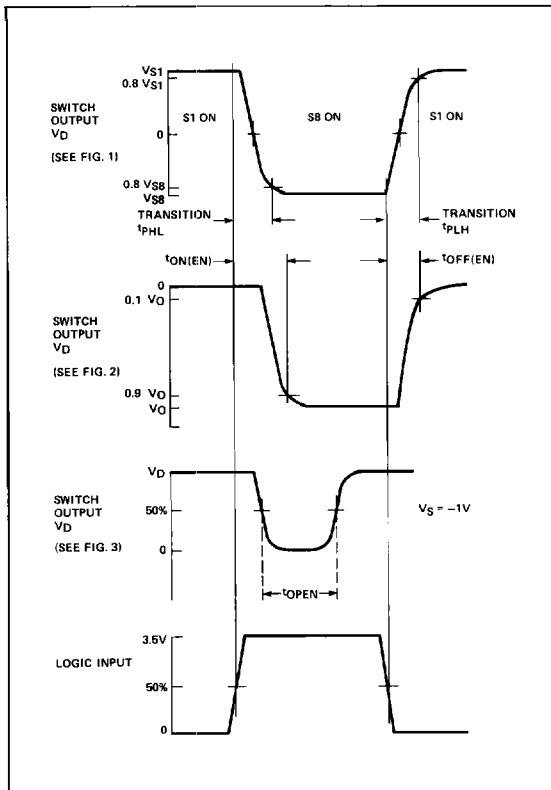**Figure 4**

A.C. TEST CIRCUITS

OFF-ISOLATION MEASUREMENT CIRCUIT

Figure 5
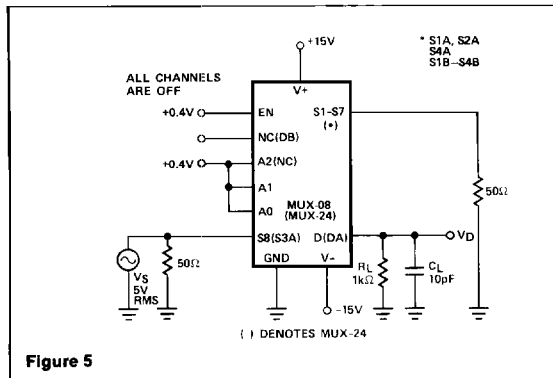
SWITCHING TIME WAVEFORMS

APPLICATIONS INFORMATION

These analog multiplexers employ ion-implanted JFETs in a switch configuration designed to assure break-before-make action. The turn-off time is much faster than the turn-on time to guarantee this feature over the full operating temperature and input voltage range. Fabricated with Bipolar-JFET processing, **special handling as required with CMOS devices, is not necessary to prevent damage to this multiplexer.** Because the digital inputs only require a 2.0V logic "1" input level, power-consuming pull-up resistors are not required for TTL compatibility to insure break-make switching as is most often the case with CMOS multiplexers. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode (about 10nA) as the input voltage is raised above $\approx 1.4V$.

The "ON" resistance, R_{ON}, of the analog switches is constant over the wide input voltage range of $-15V$ to $+11V$ with $V_{SUPPLY} = \pm 15V$. Higher input voltage is tolerable provided that some form of current limiting is employed (such as that of an op-amp output stage) to avoid exceeding junction temperature and power dissipation requirements. For normal operation, however, positive input voltages should be restricted to 11V (or 4V less than the positive supply). This assures that the V_{GS} of an "OFF" switch remains greater than its V_p and prevents that channel from being falsely turned "ON". When operating with negative input voltages, the gate-to-channel diode will be turned on if the voltage drop across an "ON" switch exceeds $-0.6V$. While this condition will cause an error in the output, it will not damage the switch. In lab tests, the multiplexer output has been loaded with 0.01μF capacitor in the circuit of Figure 1. With $V_1 = -10V$ and $V_8 = +10V$, the logic input was driven at a 1kHz rate. The positive-going slew rate was 0.3V/μs which is equivalent to normal I_{DSS} of 3mA. The negative-going slew rate was 0.7V/μs which is equivalent to a "reverse" I_{DSS} of 7mA. Note that when switch 1 is first turned "ON" it has a drop of -20 across its terminals. In spite of that fact, the current is limited to approximately twice its normal I_{DSS}.
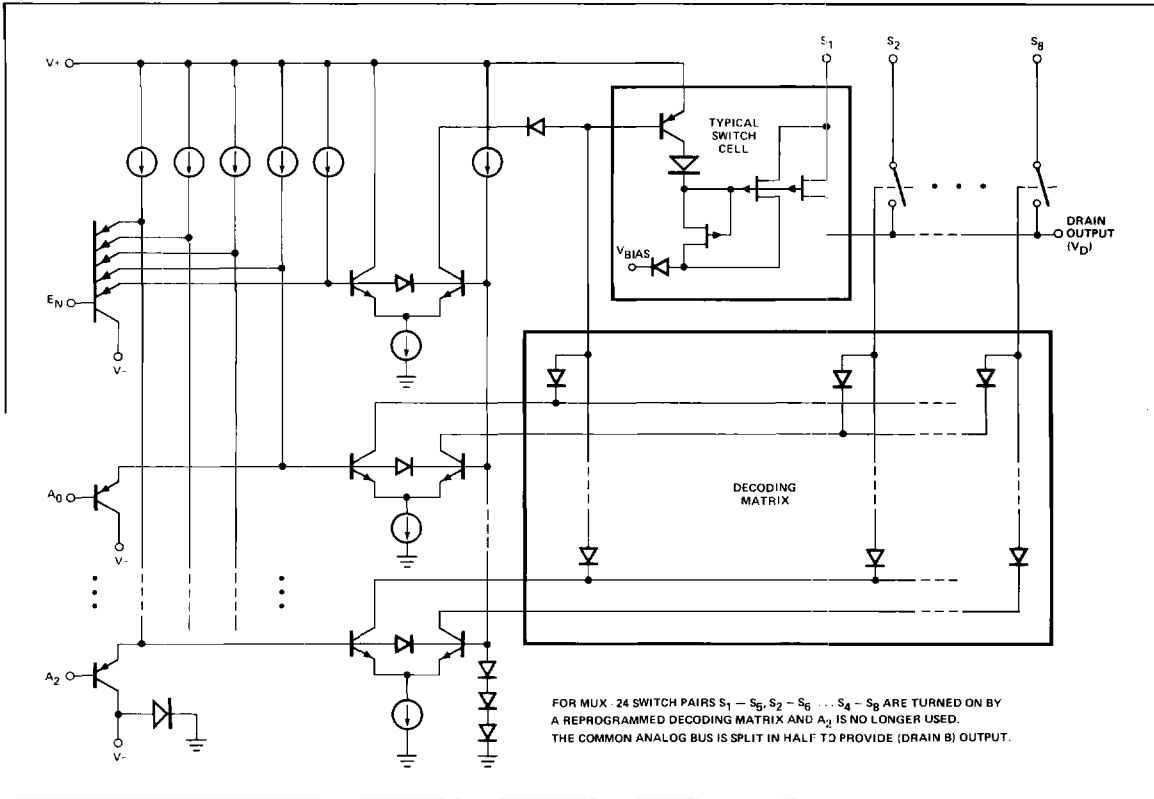
CROSSTALK AND OFF-ISOLATION

Crosstalk and off-isolation performance is influenced by the type of package selected. Epoxy (P) packaged device typically exhibit a 12dB improvement in off-isolation (f = 500kHz) performance when compared to ceramic (Q packaged devices. Epoxy packaged devices typically exhibit a 15dB improvement in crosstalk (f = 500kHz) performance when compared to ceramic (Q) packaged devices.

SINGLE SUPPLY OPERATION OF JFET MULTIPLEXERS

PMI's JFET multiplexers will operate from a single positive supply voltage with the negative supply pin at ground potential. The analog signal range will include ground.

For complete single supply operation information, refer application note, AN-32.
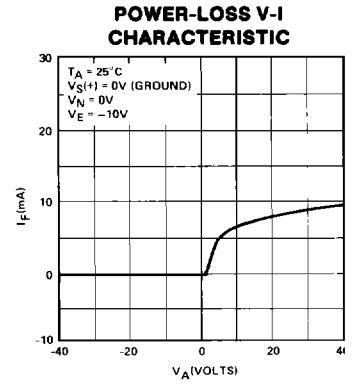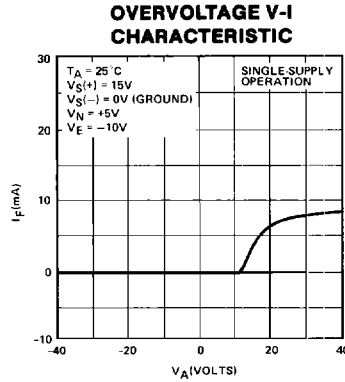
SIMPLIFIED MUX-08 SCHEMATIC

FOR MUX-24 SWITCH PAIRS $S_1 - S_5, S_2 - S_6 \ldots S_4 - S_8$ ARE TURNED ON BY A REPROGRAMMED DECODING MATRIX AND A_2 IS NO LONGER USED. THE COMMON ANALOG BUS IS SPLIT IN HALF TO PROVIDE (DRAIN B) OUTPUT.
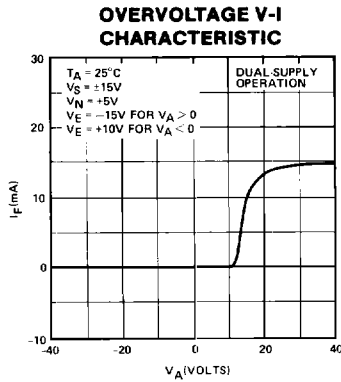
he simplified MUX-08/MUX-24 schematic shows that logic ip points are determined by two forward diode drops. An ternal clamping diode between V− and ground prevents :cessive current flow between V+ and ground in the event at V− becomes open circuit. The decoding matrix is :complished by a programmed diode array. The switch cell insists of P channel JFET's with appropriate blocking odes which ruggedizes the circuit's overvoltage and supply ss characteristics.

FFERENTIAL MULTIPLEXERS

ie characteristic unique to differential multiplexers UX-24) is the ability to reject common-mode signals from coming differential error signals. Common-mode rejection i parameter which defines the amount of rejection in terms dB. The MUX-24 exhibits a 106dB at 60Hz and 101dB at)Hz of CMRR using the test circuit of Figure 6.

CMRR TEST CIRCUIT

Figure 6

$$CMRR = 20 \log \left(\frac{V_O}{1000 \times V_i} \right)$$

ANALOG SWITCHES/MULTIPLEXERS

13
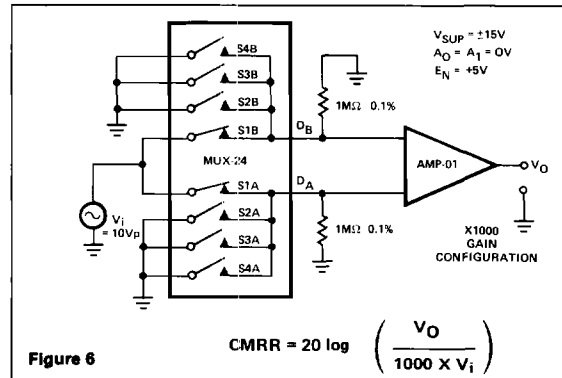
TYPICAL PERFORMANCE CHARACTERISTICS

OVERVOLTAGE V-I CHARACTERISTIC

OVERVOLTAGE V-I CHARACTERISTIC

POWER-LOSS V-I CHARACTERISTIC

OVERVOLTAGE/POWER-LOSS MEASUREMENT TEST CIRCUIT