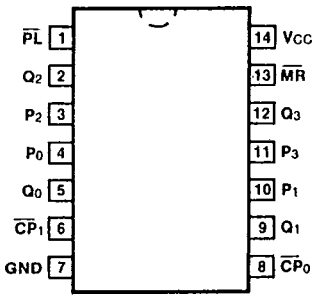
54/74196
54LS/74LS196
PRESETTABLE DECADE COUNTERS

DESCRIPTION — The '196 decade ripple counter is partitioned into divide-by-two and divide-by-five sections which can be combined to count either in BCD (8421) sequence or in a bi-quinary mode producing a 50% duty cycle output. Both circuit types have a Master Reset ($\overline{MR}$) input which overrides all other inputs and asynchronously forces all outputs LOW. A Parallel Load input ($\overline{PL}$) overrides clocked operations and asynchronously loads the data on the Parallel Data inputs (P_n) into the flip-flops. This preset feature makes the circuits usable as programmable counters. The circuits can also be used as 4-bit latches, loading data from the Parallel Data inputs when $\overline{PL}$ is LOW and storing the data when $\overline{PL}$ is HIGH. In the counting modes, state changes are initiated by the falling edge of the clock.

- **HIGH COUNTING RATES — TYPICALLY 60 MHz**
- **CHOICE OF COUNTING MODES — BCD, BI-QUINARY, BINARY**
- **ASYNCHRONOUS PRESET AND MASTER RESET**

CONNECTION DIAGRAM
PINOUT A



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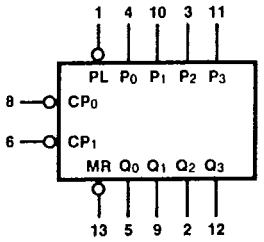
LOGIC SYMBOL



VCC = Pin 14
GND = Pin 7

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE: VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE: VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74196PC, 74LS196PC		9A
Ceramic DIP (D)	A	74196DC, 74LS196DC	54196DM, 54LS196DM	6A
Flatpak (F)	A	74196FC, 74LS196FC	54196FM, 54LS196FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$\overline{CP_0}$	÷2 Section Clock Input (Active Falling Edge)	2.0/3.0	1.0/1.5
$\overline{CP_1}$	÷5 Section Clock Input (Active Falling Edge)	3.0/4.0	2.0/1.75
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	2.0/2.0	1.0/0.5
$P_0 - P_3$	Parallel Data Inputs	1.0/1.0	0.5/0.25
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	1.0/1.0	0.5/0.25
$Q_0 - Q_3$*	Flip-flop Outputs*	20/10	10/5.0 (2.5)

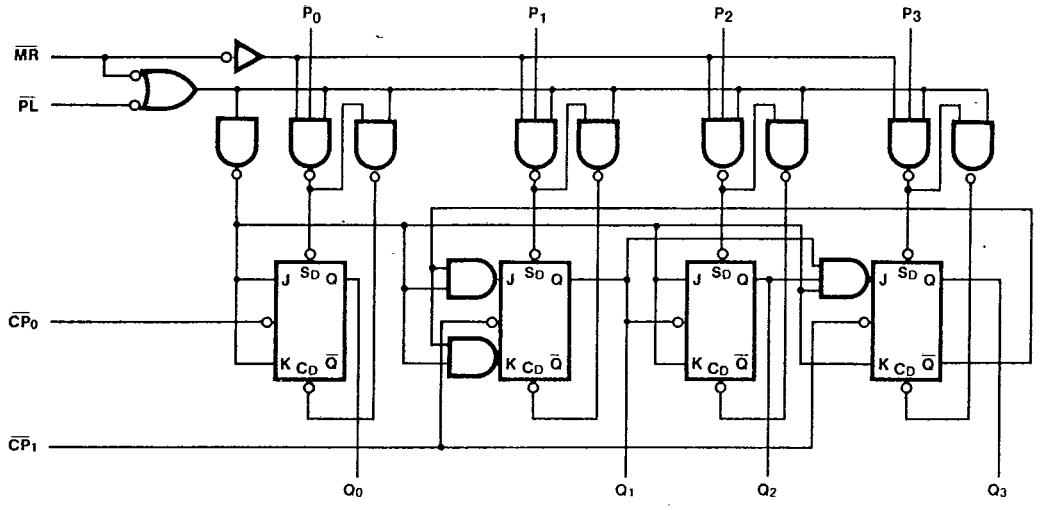
*Q_0 is guaranteed to drive the full rated fan-out plus the $\overline{CP_1}$ input.

FUNCTIONAL DESCRIPTION — The '196 and '197 are asynchronous presettable decade and binary ripple counters. The '196 decade counter is partitioned into divide-by-two and divide-by-five sections while the '197 is partitioned into divide-by-two and divide-by-eight sections, with all sections having a separate Clock input. In the counting modes, state changes are initiated by the HIGH-to-LOW transition of the clock signals. State changes of the Q outputs, however, do not occur simultaneously because of the internal ripple delays. When using external logic to decode the Q outputs, designers should bear in mind that the unequal delays can lead to decoding spikes and thus a decoded signal should not be used as a clock or strobe. The $\overline{CP_0}$ input serves the Q_0 flip-flop in both circuit types while the $\overline{CP_1}$ input serves the divide-by-five or divide-by-eight section. The Q_0 output is designed and specified to drive the rated fan-out plus the $\overline{CP_1}$ input. With the input frequency connected to $\overline{CP_0}$ and with Q_0 driving $\overline{CP_1}$, the '197 forms a straight forward modulo-16 counter, with Q_0 the least significant output and Q_3 the most significant output.

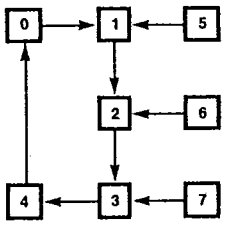
The '196 decade counter can be connected up to operate in two different count sequences. With the input frequency connected to $\overline{CP_0}$ and with Q_0 driving $\overline{CP_1}$, the circuit counts in the BCD (8421) sequence. With the input frequency connected to $\overline{CP_1}$ and Q_3 driving $\overline{CP_0}$, Q_0 becomes the low frequency output and has a 50% duty cycle waveform. Note that the maximum counting rate is reduced in the latter (bi-quinary) configuration because of the interstage gating delay within the divide-by-five section.

The '196 and '197 have an asynchronous active LOW Master Reset input ($\overline{MR}$) which overrides all other inputs and forces all outputs LOW. The counters are also asynchronously presettable. A LOW on the Parallel Load input ($\overline{PL}$) overrides the clock inputs and loads the data from Parallel Data (P_0 — P_3) inputs into the flip-flops. While $\overline{PL}$ is LOW, the counters act as transparent latches and any change in the P_n inputs will be reflected in the outputs. In order for the intended parallel data to be entered and stored, the recommended setup and hold times with respect to the rising edge of $\overline{PL}$ should be observed.

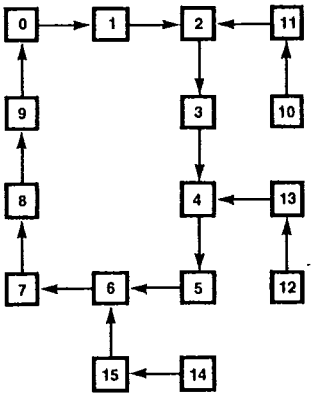
LOGIC DIAGRAM



÷5 STATE DIAGRAM



BCD STATE DIAGRAM



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MODE SELECT TABLE

INPUTS			RESPONSE
$\overline{MR}$	$\overline{PL}$	$\overline{CP}$	
L	X	X	Q_n forced LOW
H	L	X	$P_n \rightarrow Q_n$
H	H	⊓	Count Up

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARMETER		54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{IH}	Input HIGH Current	$\overline{CP_0}$		1.0		0.2	mA	V_{CC} = Max, V_{IN} = 5.5 V
		'196 $\overline{CP_1}$		1.0		0.4		
		'197 $\overline{CP_1}$		1.0		0.2		
I_{CC}	Power Supply Current			59		20	mA	V_{CC} = Max All Inputs = Gnd

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER		54/74 C_L = 15 pF, R_L = 400 Ω Min	54/74 C_L = 15 pF, R_L = 400 Ω Max	54/74LS C_L = 15 pF Min	54/74LS C_L = 15 pF Max	UNITS	CONDITIONS
f_{max}	Maximum Count Frequency at $\overline{CP_0}$	'196 '197	50 50		45 50		MHz	Figs. 3-1, 3-9
f_{max}	Maximum Count Frequency at $\overline{CP_1}$	'196 '197	25 25		22.5 25		MHz	Fig. 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP_0}$ to Q_0			12 15		12 12	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP_1}$ to Q_1			18 21		14 14	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP_1}$ to Q_2	'196		36 42		34 32	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP_1}$ to Q_2	'197		36 42		36 34	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP_1}$ to Q_3	'196		21 18		18 18	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP_1}$ to Q_3	'197		54 63		50 55	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n			24 38		15 35	ns	Figs. 3-2, 3-5
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n			33 36		24 35	ns	Figs. 3-1, 3-17
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n			37		37	ns	Figs. 3-1, 3-17

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER		54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
t_s (H) t_s (L)	Setup Time HIGH or LOW P_n to $\overline{PL}$		10 15		8.0 12		ns	Fig. 3-13
t_h (H) t_h (L)	Hold Time HIGH or LOW P_n to $\overline{PL}$		0 0		0 6.0		ns	Fig. 3-13
t_w (H)	$\overline{CP_0}$ Pulse Width HIGH	'196 '197	20 20		12 10		ns	Fig. 3-9
t_w (H)	$\overline{CP_1}$ Pulse Width HIGH	'196 '197	30 30		24 20		ns	Fig. 3-9
t_w (L)	$\overline{PL}$ Pulse Width LOW		20		18		ns	Fig. 3-17
t_w (L)	$\overline{MR}$ Pulse Width LOW		15		12		ns	Fig. 3-17
t_{rec}	Recovery Time $\overline{PL}$ to $\overline{CP_n}$		20		16		ns	Fig. 3-17
t_{rec}	Recovery Time $\overline{MR}$ to $\overline{CP_n}$		20		18		ns	Fig. 3-17