- **Output Swing Includes Both Supply Rails**
- **Extended Common-Mode Input Voltage Range . . . 0 V to 4.5 V (Min) With 5-V Single Supply**
- **No Phase Inversion**
- **Low Noise . . . 18 nV/$\sqrt{\text{Hz}}$ Typ at f = 1 kHz**
- **Low Input Offset Voltage**
  950 μV Max at T_A = 25°C (TLV2422A)
- **Low Input Bias Current . . . 1 pA Typ**
- **Micropower Operation . . . 50 μA Per Channel**
- **600-Ω Output Drive**
- **Available in Q-Temp Automotive**
  HighRel Automotive Applications
  Configuration Control / Print Support
  Qualification to Automotive Standards

description

The TLV2422 and TLV2422A are dual low-voltage operational amplifiers from Texas Instruments. The common-mode input voltage range for this device has been extended over the typical CMOS amplifiers making them suitable for a wide range of applications. In addition, the devices do not phase invert when the common-mode input is driven to the supply rails. This satisfies most design requirements without paying a premium for rail-to-rail input performance. They also exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. This family is fully characterized at 3-V and 5-V supplies and is optimized for low-voltage operation. The TLV2422 only requires 50 μA of supply current per channel, making it ideal for battery-powered applications. The TLV2422 also has increased output drive over previous rail-to-rail operational amplifiers and can drive 600-Ω loads for telecom applications.

Other members in the TLV2422 family are the high-power, TLV2442, and low-power, TLV2432, versions.

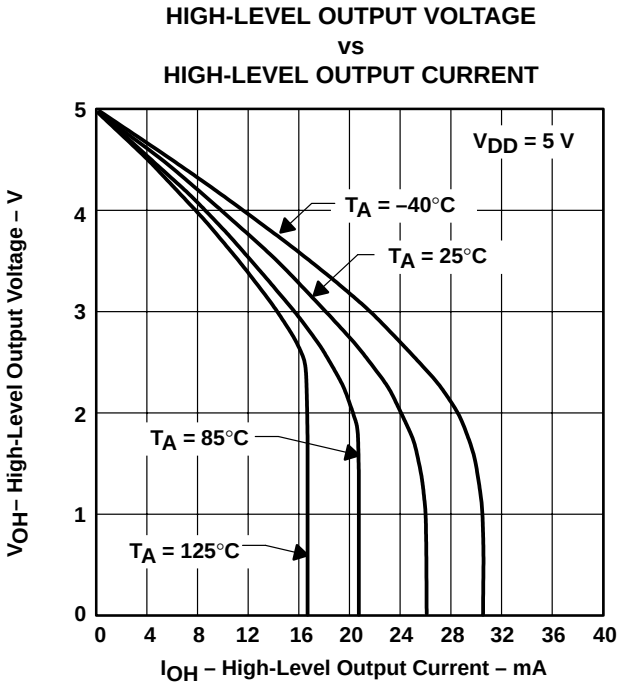

Figure 1

The TLV2422, exhibiting high input impedance and low noise, is excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels and low-voltage operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single- or split-supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLV2422A is available with a maximum input offset voltage of 950 μV.

If the design requires single operational amplifiers, see the TI TLV2211/21/31. This is a family of rail-to-rail output operational amplifiers in the SOT-23 package. Their small size and low power consumption, make them ideal for high density, battery-powered equipment.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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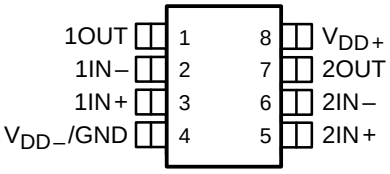
AVAILABLE OPTIONS

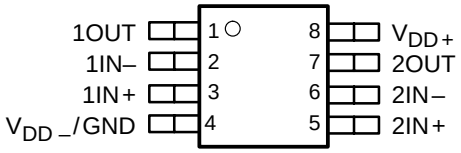
T_A	V_{IO}max AT 25°C	PACKAGED DEVICES					CHIP FORM (Y)
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	TSSOP (PW)	CERAMIC FLAT PACK (U)	
0°C to 70°C	2.5 mV	TLV2422CD	—	—	TLV2422CPWLE	—	TLV2422Y
–40°C to 85°C	950 µV	TLV2422AID	—	—	TLV2422AIPWLE	—	
	2.5 mV	TLV2422ID	—	—	—	—	
–40°C to 125°C	950 µV	TLV2422AQD	—	—	—	—	
	2.5 mV	TLV2422QD	—	—	—	—	
–55°C to 125°C	950 µV	—	TLV2422AMFK	TLV2422AMJG	—	TLV2422AMU	
	2 mV	—	TLV2422MFK	TLV2422MJG	—	TLV2422MU	

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLV2422CDR). The PW package is available only left-end taped and reeled. Chips are tested at 25°C.

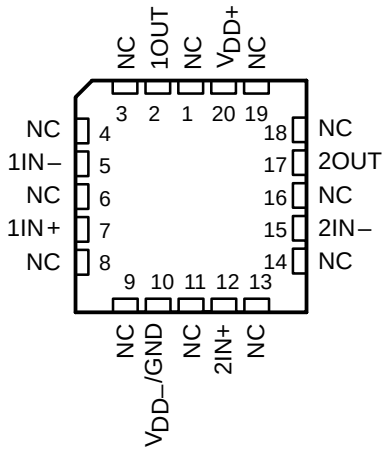
D OR JG PACKAGE
(TOP VIEW)



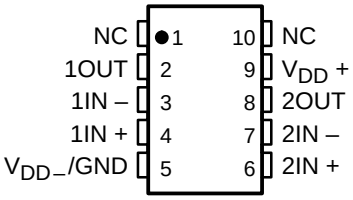
PW PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)

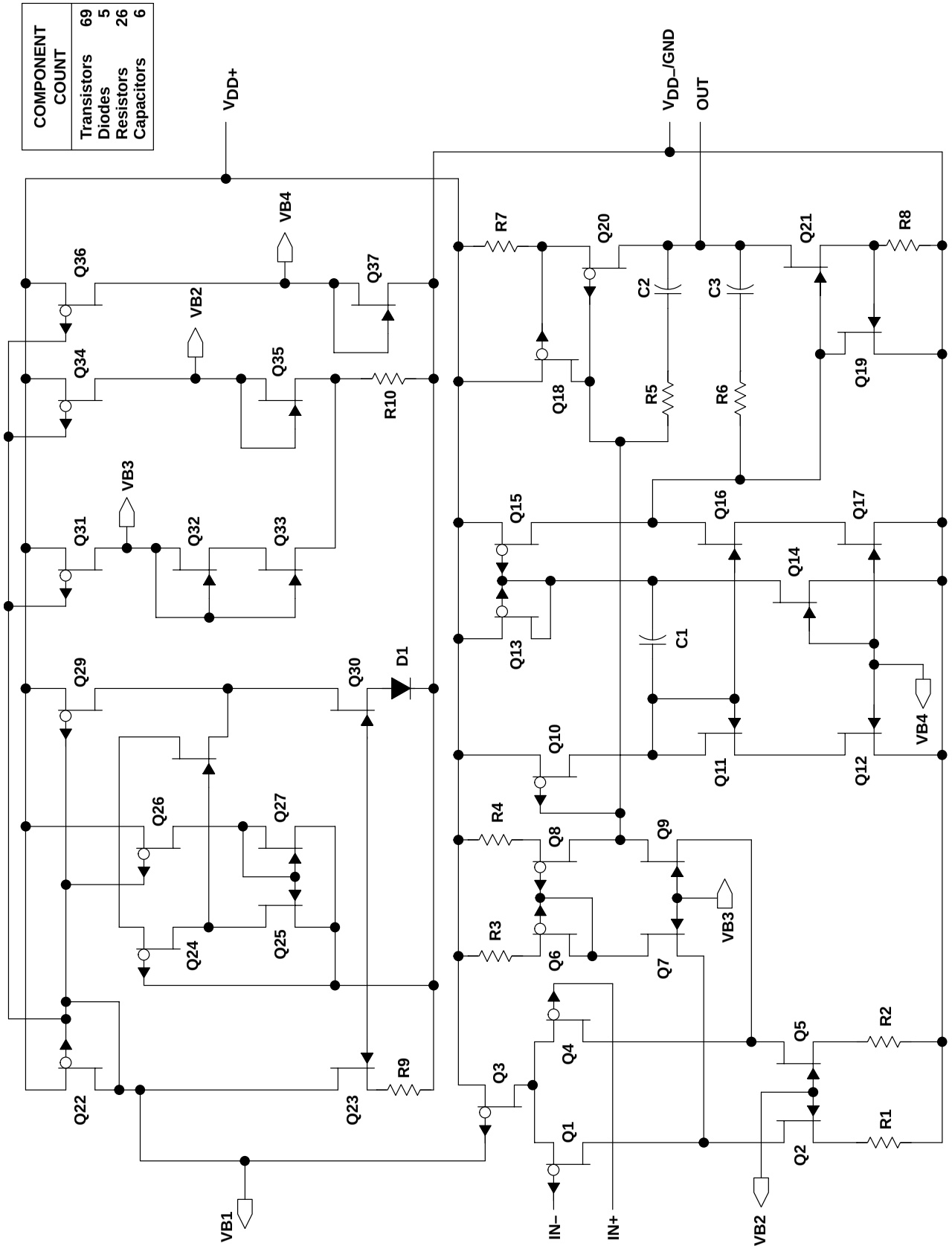


U PACKAGE
(TOP VIEW)



NC – No internal connection

equivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 12 V
Differential input voltage, V_{ID} (see Note 2) . . . . . $\pm V_{DD}$
Input voltage, V_I (any input, see Note 1): C and I suffix . . . . . –0.3 V to V_{DD}
Input current, I_I (each input) . . . . . ±5 mA
Output current, I_O . . . . . ±50 mA
Total current into V_{DD+} . . . . . ±50 mA
Total current out of V_{DD-} . . . . . ±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . . unlimited
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix . . . . . 0°C to 70°C
I suffix . . . . . –40°C to 85°C
Q suffix . . . . . –40°C to 125°C
M suffix . . . . . –55°C to 125°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
2. Differential voltages are at IN+ with respect to IN–. Excessive current flows if input is brought below V_{DD-} – 0.3 V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
PW	525 mW	4.2 mW/°C	336 mW	273 mW	105 mW
U	675 mW	5.4 mW/°C	432 mW	350 mW	135 mW

recommended operating conditions

	C SUFFIX		I SUFFIX		Q SUFFIX		M SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{DD\pm}$	2.7	10	2.7	10	2.7	10	2.7	10	V
Input voltage range, V_I	V_{DD-}	$V_{DD+}-0.8$	V_{DD-}	$V_{DD+}-0.8$	V_{DD-}	$V_{DD+}-0.8$	V_{DD-}	$V_{DD+}-0.8$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+}-0.8$	V_{DD-}	$V_{DD+}-0.8$	V_{DD-}	$V_{DD+}-0.8$	V_{DD-}	$V_{DD+}-0.8$	V
Operating free-air temperature, T_A	0	70	–40	85	–40	125	–55	125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2422C			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0,	$V_{DD}\pm$ = ±2.5 V, R_S = 50 Ω	25°C		300	2000	µV
				Full range			2500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 70°C		2		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5	60	pA
				Full range			150	
I_{IB}	Input bias current			25°C		1	60	pA
				Full range			150	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le$ 5 mV,	R_S = 50 Ω	25°C	0 to 2.5	–0.25 to 2.75		V
				Full range	0 to 2.2			
V_{OH}	High-level output voltage	I_{OH} = –100 µA		25°C		2.97		V
		I_{OH} = –500 µA		25°C		2.75		
				Full range	2.5			
V_{OL}	Low-level output voltage	V_{IC} = 0,	I_{OL} = 100 µA	25°C		0.05		V
		V_{IC} = 0,	I_{OL} = 250 µA	25°C		0.2		
				Full range			0.5	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 2 V	R_L = 10 kΩ‡	25°C	6	10		V/mV
				Full range	3			
			R_L = 1 MΩ‡	25°C		700		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz		25°C		8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.5 V, V_O = 1.5 V, R_S = 50 Ω		25°C	70	83		dB
				Full range	70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		dB
				Full range	80			
I_{DD}	Supply current	V_O = 1.5 V,	No load	25°C		100	150	µA
				Full range			175	

† Full range is 0°C to 70°C.
‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2422I			TLV2422AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0,	$V_{DD}\pm$ = ±2.5 V, R_S = 50 Ω	25°C		300	2000		300	950	μV
				Full range			2500			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 70°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				Full range			150			150	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				Full range			150			150	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le$ 5 mV,	R_S = 50 Ω	25°C	0 to 2.5	–0.25 to 2.75		0 to 2.5	–0.25 to 2.75		V
				Full range	0 to 2.2			0 to 2.2			
V_{OH}	High-level output voltage	I_{OH} = –100 μA		25°C		2.97			2.97		V
		I_{OH} = –500 μA		25°C		2.75			2.75		
				Full range	2.5			2.5			
V_{OL}	Low-level output voltage	V_{IC} = 0,	I_{OL} = 100 μA	25°C		0.05			0.05		V
		V_{IC} = 0,	I_{OL} = 250 μA	25°C		0.2			0.2		
				Full range			0.5			0.5	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 2 V	R_L = 10 kΩ‡	25°C	6	10		6	10		V/mV
				Full range	3			3			
			R_L = 1 MΩ‡	25°C		700			700		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz		25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		130			130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.5 V, R_S = 50 Ω	V_O = 1.5 V,	25°C	70	83		70	83		dB
				Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 1.5 V,	No load	25°C		100	150		100	150	μA
				Full range			175			175	

† Full range is – 40°C to 85°C.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2422C, TLV2422I TLV2422AI			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.5 V to 3.5 V, C_L = 100 pF‡	R_L = 10 kΩ‡,	25°C	0.01	0.02		V/μs
				Full range	0.008			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		100		nV/√Hz
		f = 1 kHz		25°C		23		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		2.7		μV
		f = 0.1 Hz to 10 Hz		25°C		4		
I_n	Equivalent input noise current			25°C		0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 1 kHz, R_L = 10 kΩ‡	A_V = 1	25°C		0.25%		
			A_V = 10			1.8%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF‡	R_L = 10 kΩ‡,	25°C		46		kHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, R_L = 10 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		8.3		kHz
t_s	Settling time	A_V = –1, Step = 0.5 V to 2.5 V, R_L = 10 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		8.6		μs
			To 0.01%			16		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ‡,	C_L = 100 pF‡	25°C		62°		
	Gain margin			25°C		11		dB

† Full range for the C version is 0°C to 70°C. Full range for the I version is –40°C to 85°C.
‡ Referenced to 2.5 V

electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2422Q, TLV2422M			TLV2422AQ, TLV2422AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0,	$V_{DD}\pm$ = ±1.5 V, R_S = 50 Ω	25°C		300	2000		300	950	µV
				Full range			2500			1800	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				Full range			150			150	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				Full range			300			300	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le$ 5 mV,	R_S = 50 Ω	25°C	0 to 2.5	–0.25 to 2.75		0 to 2.5	–0.25 to 2.75		V
				Full range	0 to 2.2			0 to 2.2			
V_{OH}	High-level output voltage	I_{OH} = –100 µA		25°C		2.97			2.97		V
		I_{OH} = –500 µA		25°C		2.75			2.75		
				Full range	2.5			2.5			
V_{OL}	Low-level output voltage	V_{IC} = 0,	I_{OL} = 100 µA	25°C		0.05			0.05		V
		V_{IC} = 0,	I_{OL} = 250 µA	25°C		0.2			0.2		
				Full range			0.5			0.5	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1.5 V, V_O = 1 V to 2 V	R_L = 10 kΩ‡	25°C	6	10		6	10		V/mV
				Full range	2			2			
			R_L = 1 MΩ‡	25°C		700			700		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz		25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		130			130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω	V_O = 1.5 V,	25°C	70	83		70	83		dB
				Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 1.5 V,	No load	25°C		100	150		100	150	µA
				Full range			175			175	

† Full range is –40°C to 125°C for Q level part, –55°C to 125°C for M level part.
‡ Referenced to 1.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2422Q, TLV2422M, TLV2422AQ, TLV2422AM			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.1 V to 1.9 V, C_L = 100 pF‡	R_L = 10 kΩ‡,	25°C	0.01	0.02		V/μs
				Full range	0.008			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		100		nV/√Hz
		f = 1 kHz		25°C		23		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		2.7		μV
		f = 0.1 Hz to 10 Hz		25°C		4		
I_n	Equivalent input noise current			25°C		0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 1 kHz, R_L = 10 kΩ‡	A_V = 1	25°C		0.25%		
			A_V = 10			1.8%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF‡	R_L = 10 kΩ‡,	25°C		46		kHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, R_L = 10 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		8.3		kHz
t_s	Settling time	A_V = –1, Step = 0.5 V to 2.5 V, R_L = 10 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		8.6		μs
			To 0.01%			16		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ‡,	C_L = 100 pF‡	25°C		62°		
	Gain margin			25°C		11		dB

† Full range is –40°C to 125°C for Q level part, –55°C to 125°C for M level part.
‡ Referenced to 1.5 V

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2422C			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0,	$V_{DD}\pm$ = ±2.5 V, R_S = 50 Ω	25°C		300	2000	μV
				Full range			2500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 70°C		2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5	60	pA
				Full range			150	
I_{IB}	Input bias current			25°C		1	60	pA
				Full range			150	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le$ 5 mV,	R_S = 50 Ω	25°C	0 to 4.5	–0.25 to 4.75		V
				Full range	0 to 4.2			
V_{OH}	High-level output voltage	I_{OH} = –100 μA		25°C		4.97		V
		I_{OH} = –1 mA		25°C	4.5	4.75		
				Full range	4.25			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 100 μA	25°C		0.04		V
		V_{IC} = 2.5 V,	I_{OL} = 500 μA	25°C		0.15		
				Full range			0.5	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 10 kΩ‡	25°C	8	12		V/mV
				Full range	5			
			R_L = 1 MΩ‡	25°C		1000		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz		25°C		8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 4.5 V, V_O = 2.5 V, R_S = 50 Ω		25°C	70	90		dB
				Full range	70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		dB
				Full range	80			
I_{DD}	Supply current	V_O = 2.5 V,	No load	25°C		100	150	μA
				Full range			175	

† Full range is 0°C to 70°C.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2422I			TLV2422AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0,	$V_{DD}\pm$ = ±2.5 V, R_S = 50 Ω	25°C		300	2000		300	950	μV
				Full range			2500			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 70°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				Full range			150			150	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				Full range			150			150	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le$ 5 mV,	R_S = 50 Ω	25°C	0 to 4.5	–0.25 to 4.75		0 to 4.5	–0.25 to 4.75		V
				Full range	0 to 4.2			0 to 4.2			
V_{OH}	High-level output voltage	I_{OH} = –100 μA		25°C		4.97			4.97		V
		I_{OH} = –1 mA		25°C	4.5	4.75		4.5	4.75		
				Full range	4.25			4.25			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 100 μA	25°C		0.04			0.04		V
		V_{IC} = 2.5 V,	I_{OL} = 500 μA	25°C		0.15			0.15		
				Full range			0.5			0.5	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 10 kΩ‡	25°C	8	12		8	12		V/mV
				Full range	5			5			
			R_L = 1 MΩ‡	25°C		1000			1000		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz		25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		130			130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 4.5 V, V_O = 2.5 V, R_S = 50 Ω		25°C	70	90		70	90		dB
				Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V,	No load	25°C		100	150		100	150	μA
				Full range			175			175	

† Full range is – 40°C to 85°C.
‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2422C, TLV2422I TLV2422AI			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.5 V to 3.5 V, C_L = 100 pF‡	R_L = 10 kΩ‡,	25°C	0.01	0.02		V/μs
				Full range	0.008			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		100		nV/√Hz
		f = 1 kHz		25°C		18		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1.9		μV
		f = 0.1 Hz to 10 Hz		25°C		2.8		
I_n	Equivalent input noise current			25°C		0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	V_O = 1.5 V to 3.5 V, f = 1 kHz, R_L = 10 kΩ‡	A_V = 1	25°C		0.24%		
			A_V = 10			1.7%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF‡	R_L =10 kΩ‡,	25°C		52		kHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 10 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		5.3		kHz
t_s	Settling time	A_V = −1, Step = 1.5 V to 3.5 V, R_L = 10 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		8.5		μs
			To 0.01%			15.5		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ‡,	C_L = 100 pF‡	25°C		66°		
	Gain margin			25°C		11		dB

† Full range for the C version is 0°C to 70°C. Full range for the I version is –40°C to 85°C.
‡ Referenced to 2.5 V

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2422Q, TLV2422M			TLV2422AQ, TLV2422AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, V_O = 0,	$V_{DD}\pm$ = ±2.5 V, R_S = 50 Ω	25°C		300	2000		300	950	μV
				Full range			2500			1800	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				Full range			150			150	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				Full range			300			300	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\| \le$ 5 mV,	R_S = 50 Ω	25°C	0 to 4.5	–0.25 to 4.75		0 to 4.5	–0.25 to 4.75		V
				Full range	0 to 4.2			0 to 4.2			
V_{OH}	High-level output voltage	I_{OH} = –100 μA		25°C		4.97			4.97		V
		I_{OH} = –1 mA		25°C		4.75			4.75		
				Full range	4.5			4.5			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 100 μA	25°C		0.04			0.04		V
		V_{IC} = 2.5 V,	I_{OL} = 500 μA	25°C		0.15			0.15		
				Full range			0.5			0.5	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 10 kΩ‡	25°C	8	12		8	12		V/mV
				Full range	3			3			
			R_L = 1 MΩ‡	25°C		1000			1000		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz		25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		130			130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 2.5 V, R_S = 50 Ω		25°C	70	90		70	90		dB
				Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V,	No load	25°C		100	150		100	150	μA
				Full range			175			175	

† Full range is –40°C to 125°C for Q level part, –55°C to 125°C for M level part.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2422Q, TLV2422M, TLV2422AQ, TLV2422AM			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.5 V to 3.5 V, C_L = 100 pF‡	R_L = 10 kΩ‡,	25°C	0.01	0.02		V/μs
				Full range	0.008			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		100		nV/√Hz
		f = 1 kHz		25°C		18		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1.9		μV
		f = 0.1 Hz to 10 Hz		25°C		2.8		
I_n	Equivalent input noise current			25°C		0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	V_O = 1.5 V to 3.5 V, f = 1 kHz, R_L = 10 kΩ‡	A_V = 1	25°C		0.24%		
			A_V = 10			1.7%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF‡	R_L =10 kΩ‡,	25°C		52		kHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 10 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		5.3		kHz
t_s	Settling time	A_V = –1, Step = 1.5 V to 3.5 V, R_L = 10 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		8.5		μs
			To 0.01%			15.5		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ‡,	C_L = 100 pF‡	25°C		66°		
	Gain margin			25°C		11		dB

† Full range is –40°C to 125°C for Q level part, –55°C to 125°C for M level part.
‡ Referenced to 2.5 V

TYPICAL CHARACTERISTICS

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THD + N	Total harmonic distortion plus noise	vs Frequency	44,45
	Gain-bandwidth product	vs Supply voltage vs Free-air temperature	46 47
ϕ_m	Phase margin	vs Frequency vs Load capacitance	19,20 48
	Gain margin	vs Load capacitance	49
B_1	Unity-gain bandwidth	vs Load capacitance	50

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLV2422 INPUT OFFSET VOLTAGE

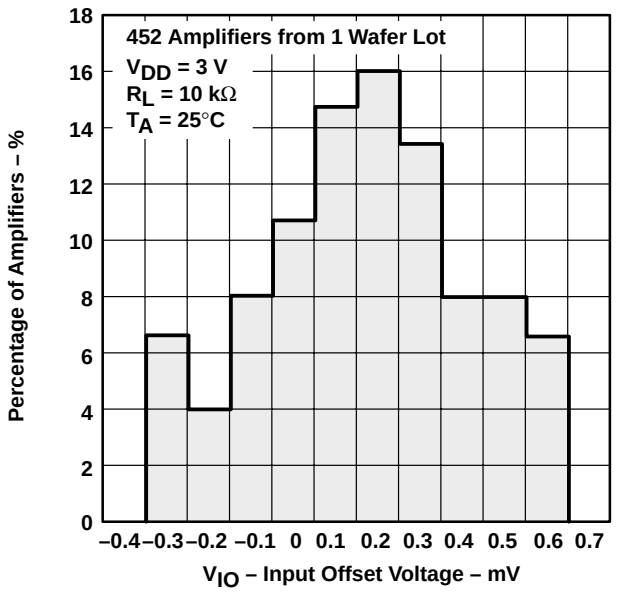


Figure 2

DISTRIBUTION OF TLV2422 INPUT OFFSET VOLTAGE

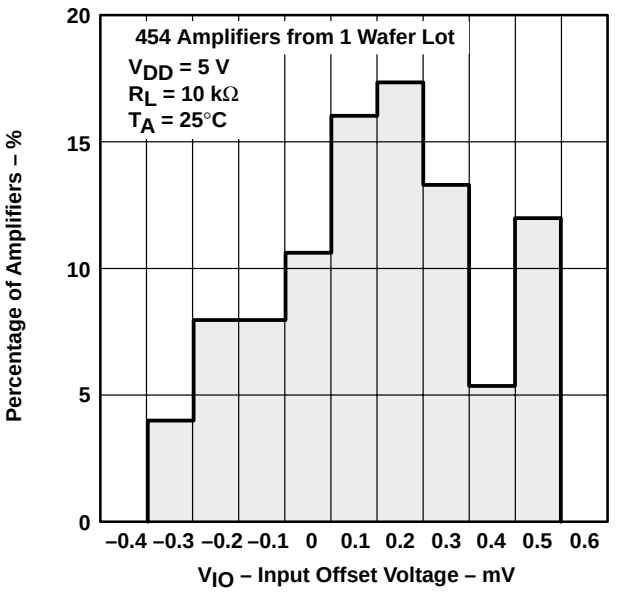


Figure 3

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

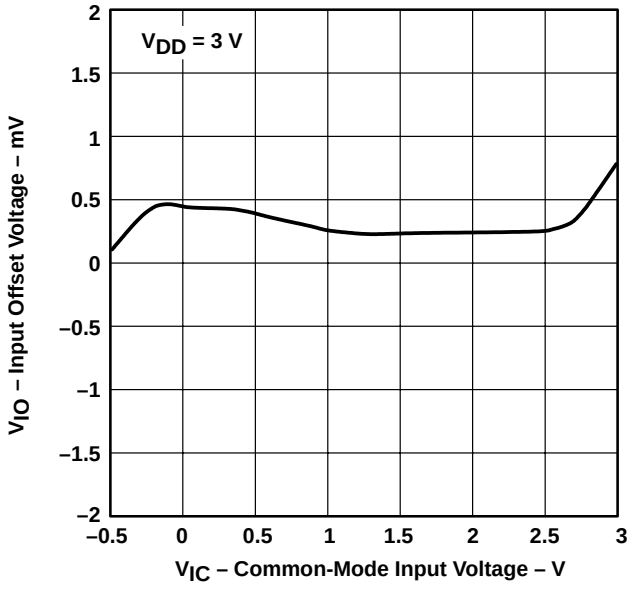


Figure 4

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

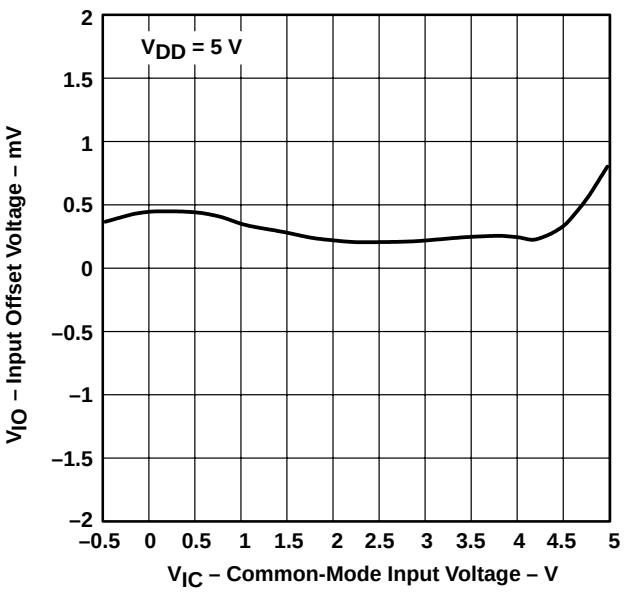


Figure 5

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLV2422 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

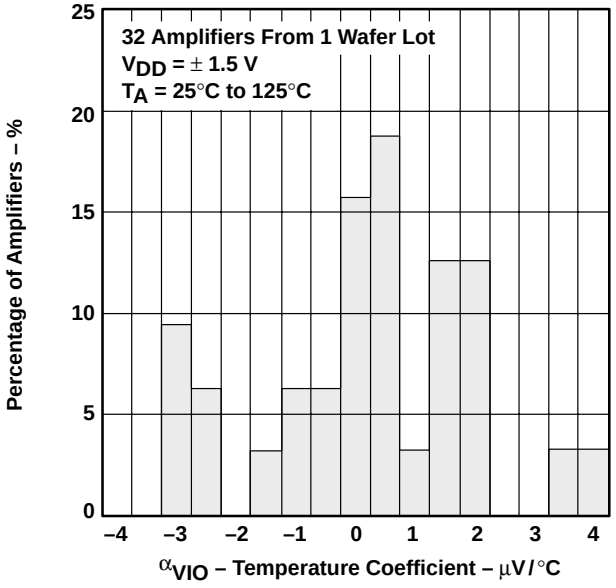


Figure 6

DISTRIBUTION OF TLV2422 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

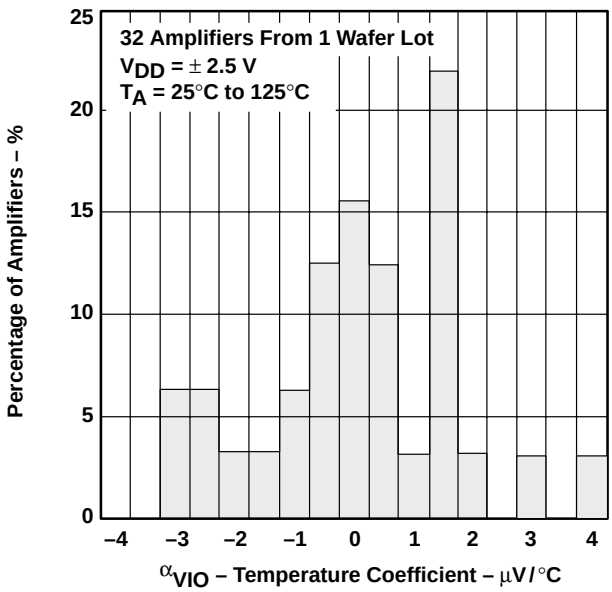


Figure 7

INPUT BIAS AND INPUT OFFSET CURRENTS vs FREE-AIR TEMPERATURE

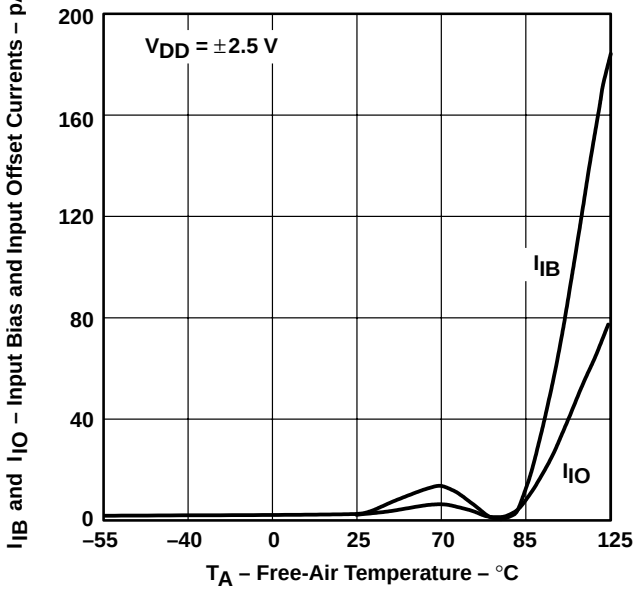


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

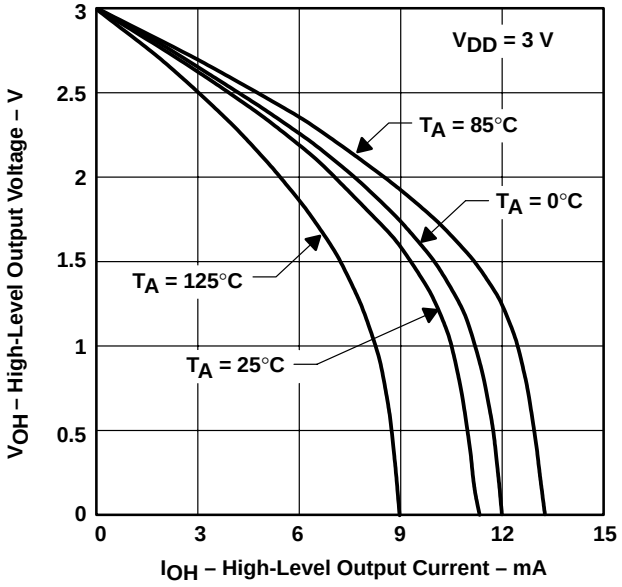


Figure 9

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

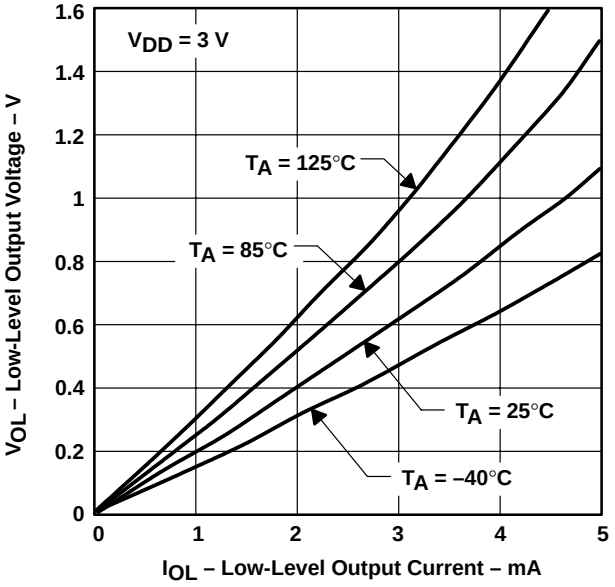


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

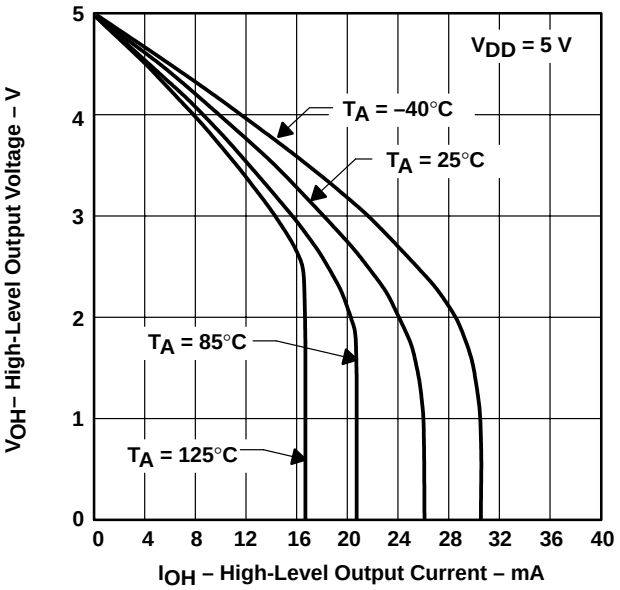


Figure 11

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

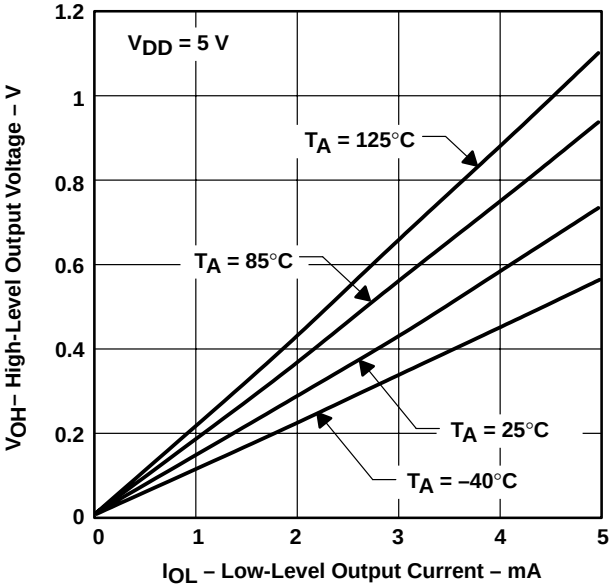


Figure 12

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

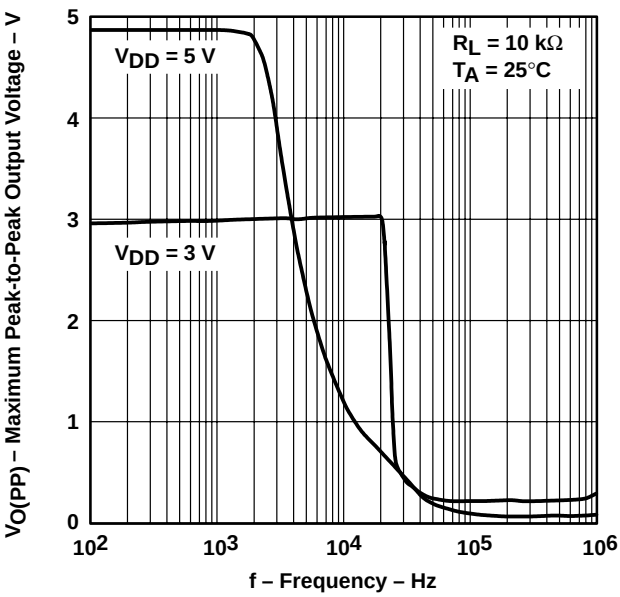


Figure 13

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT vs SUPPLY VOLTAGE

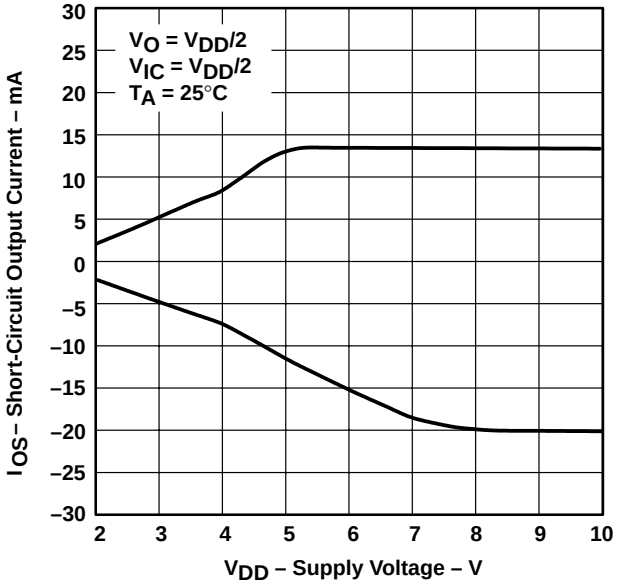


Figure 14

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

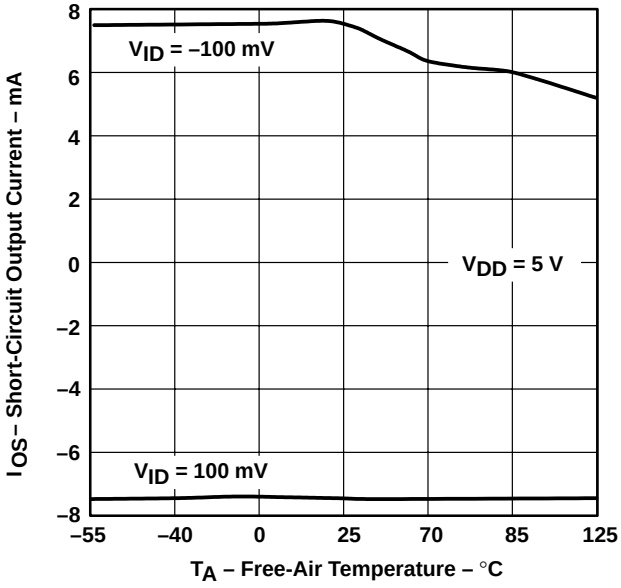


Figure 15

DIFFERENTIAL INPUT VOLTAGE vs OUTPUT VOLTAGE

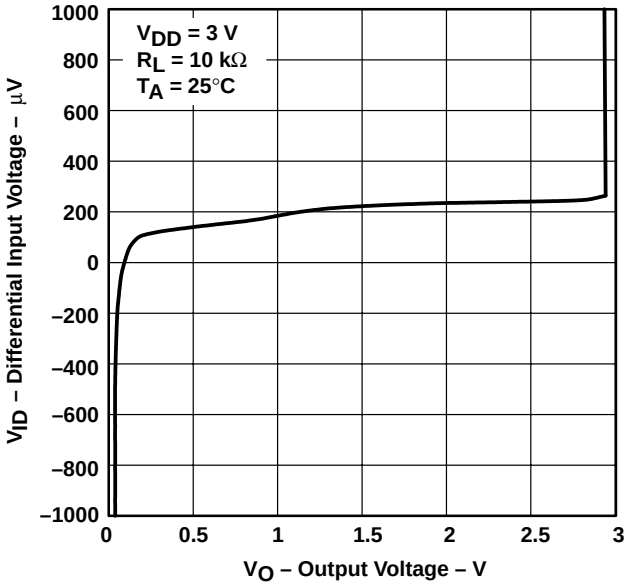


Figure 16

DIFFERENTIAL INPUT VOLTAGE vs OUTPUT VOLTAGE

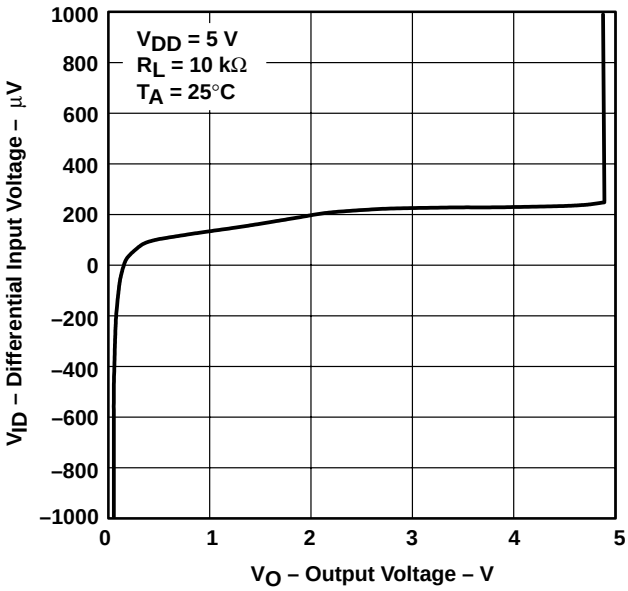


Figure 17

TYPICAL CHARACTERISTICS

DIFFERENTIAL GAIN vs LOAD RESISTANCE

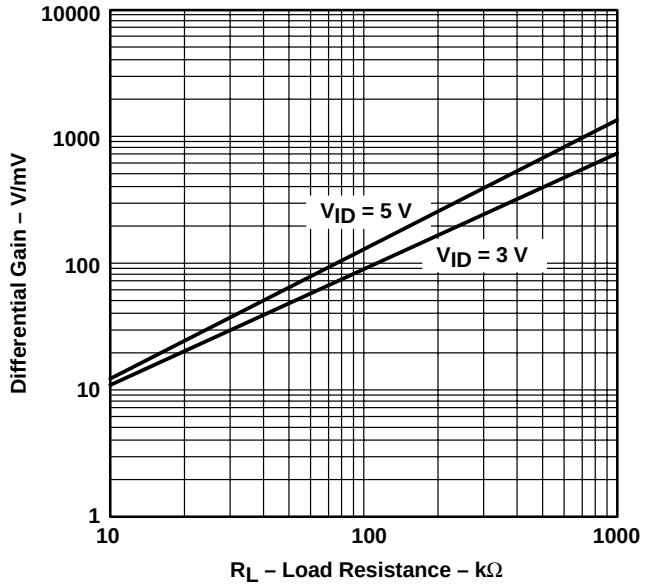


Figure 18

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

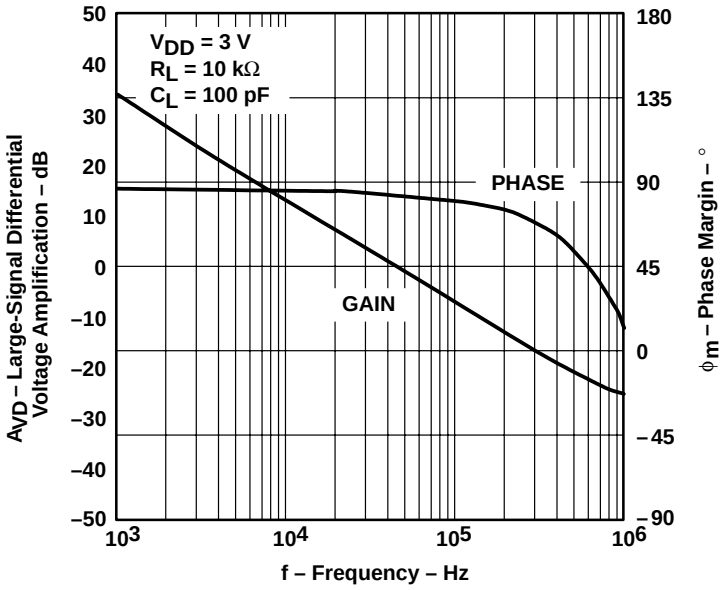


Figure 19

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN vs FREQUENCY

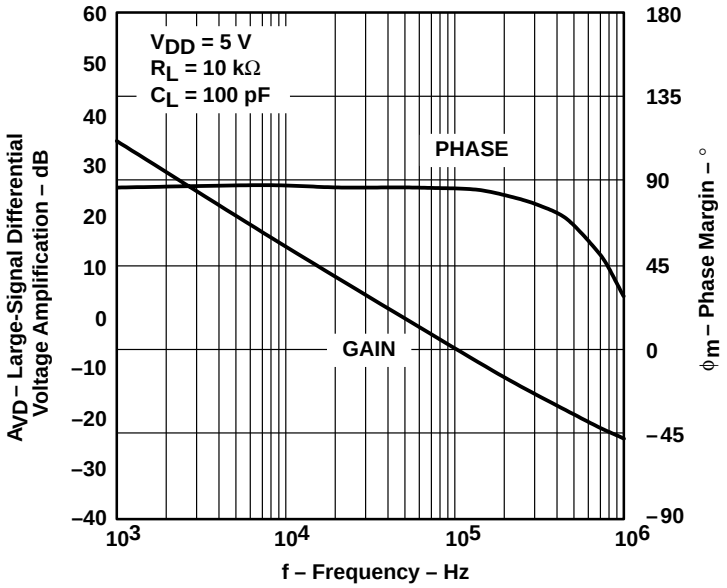


Figure 20

DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

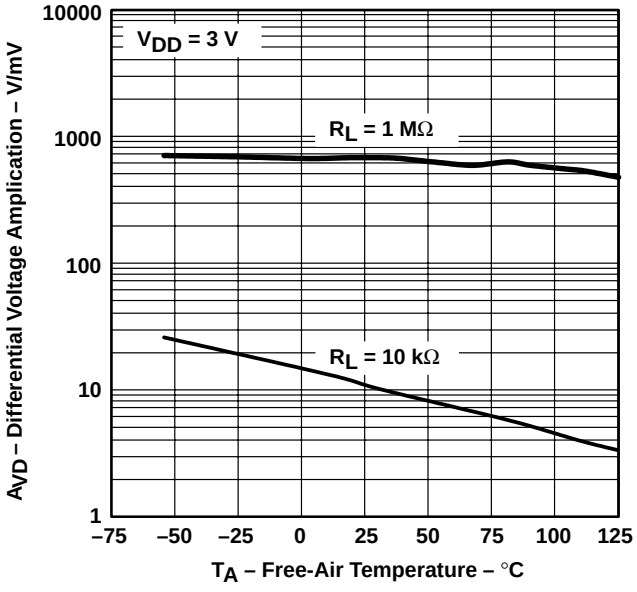


Figure 21

DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

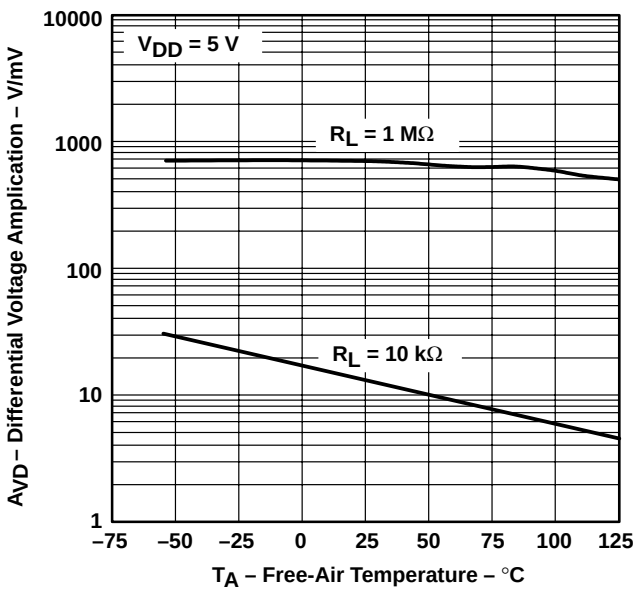


Figure 22

TYPICAL CHARACTERISTICS

OUTPUT IMPEDANCE vs FREQUENCY

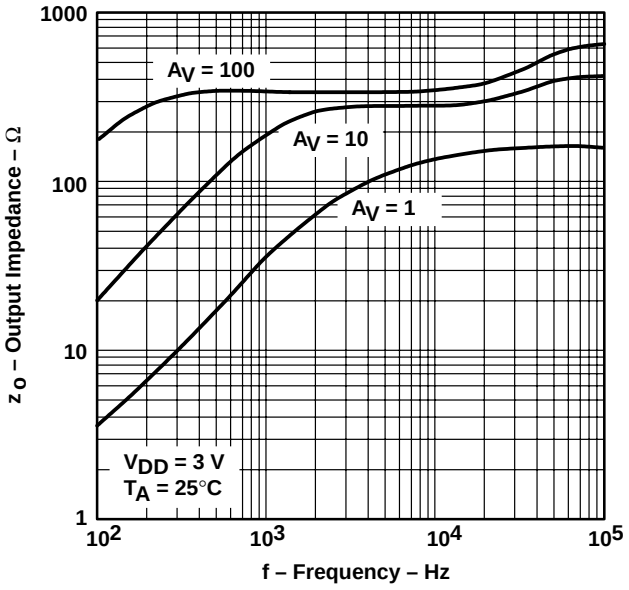


Figure 23

OUTPUT IMPEDANCE vs FREQUENCY

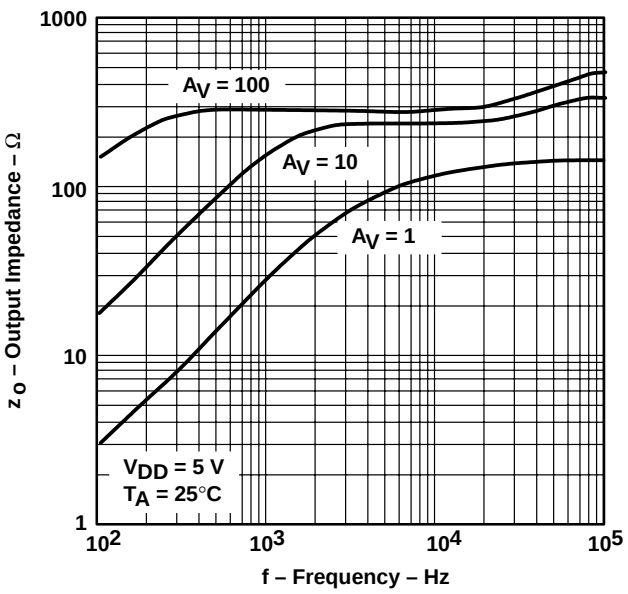


Figure 24

COMMON-MODE REJECTION RATIO vs FREQUENCY

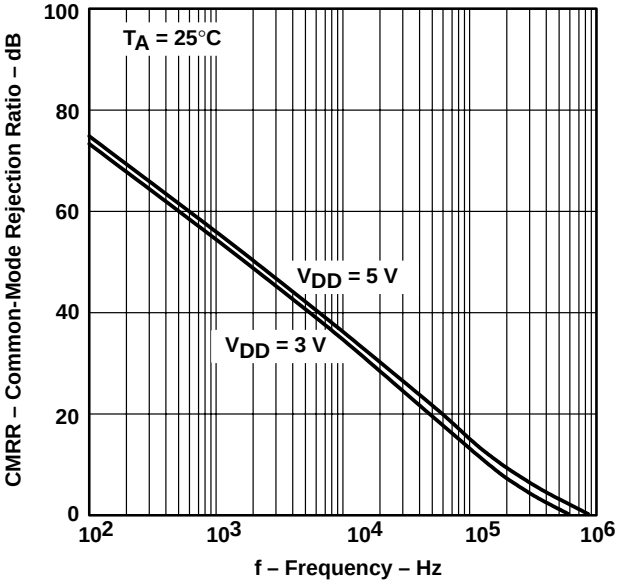


Figure 25

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

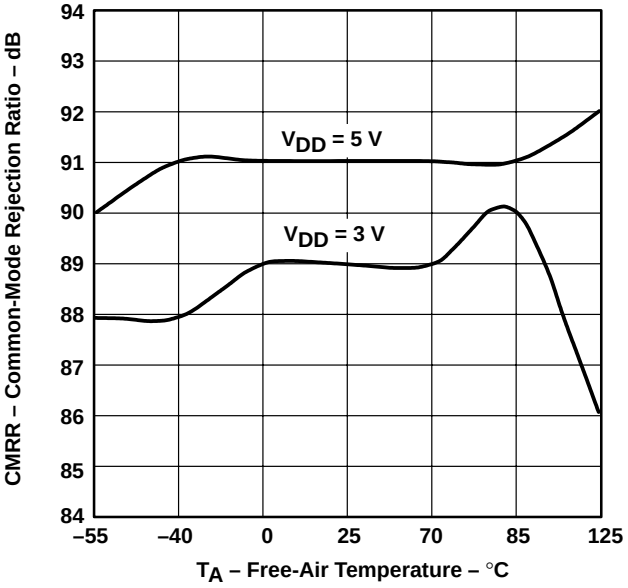


Figure 26

TYPICAL CHARACTERISTICS

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

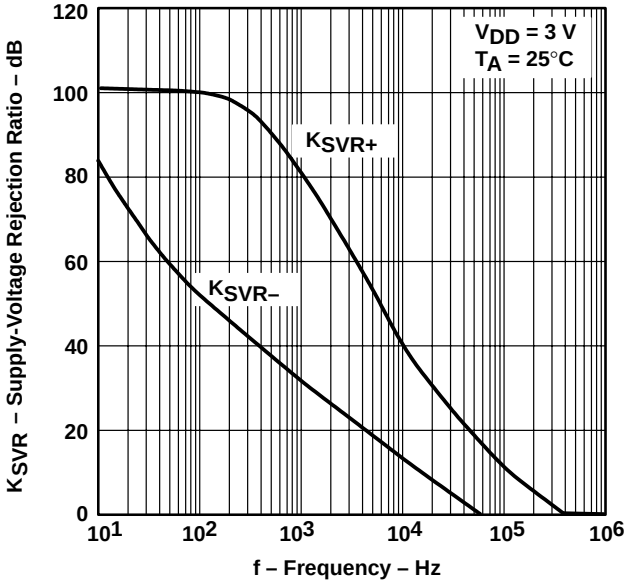


Figure 27

SUPPLY-VOLTAGE REJECTION RATIO vs FREQUENCY

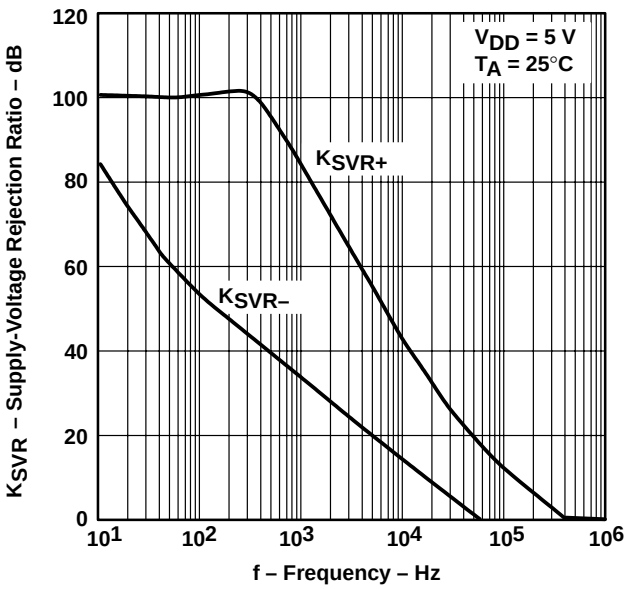


Figure 28

SUPPLY-VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

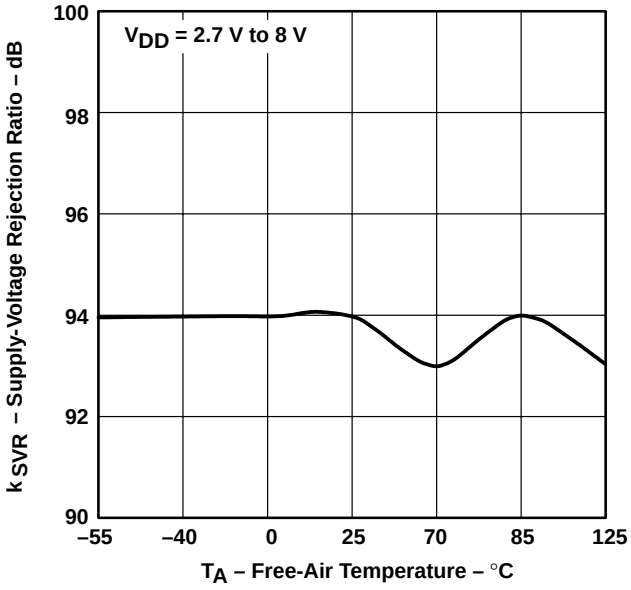


Figure 29

SUPPLY CURRENT vs SUPPLY VOLTAGE

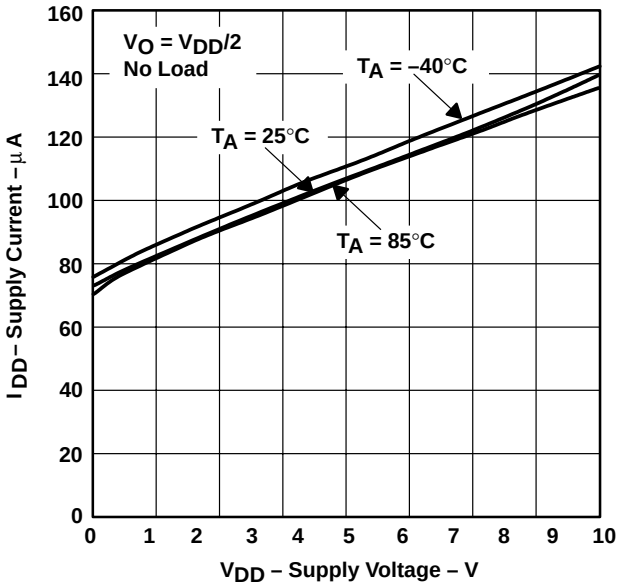


Figure 30

TYPICAL CHARACTERISTICS

SLEW RATE vs LOAD CAPACITANCE

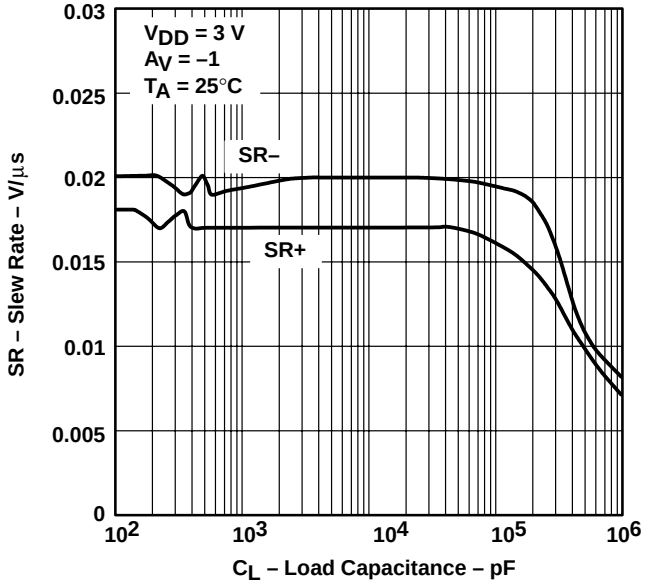


Figure 31

SLEW RATE vs FREE-AIR TEMPERATURE

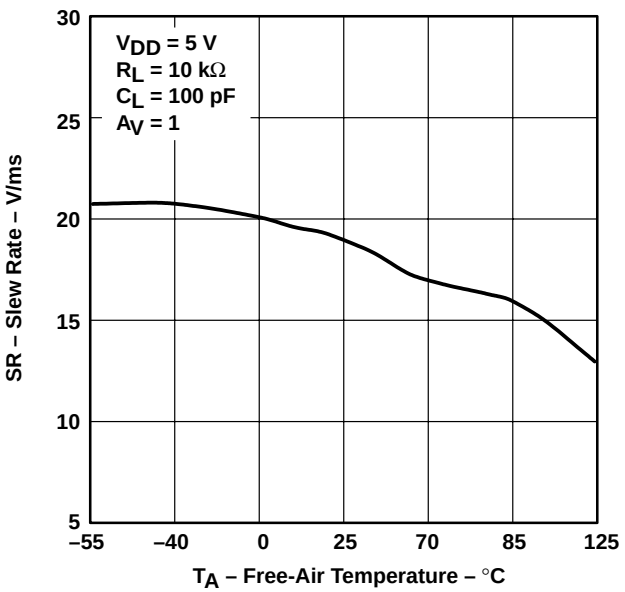


Figure 32

INVERTING LARGE-SIGNAL PULSE RESPONSE

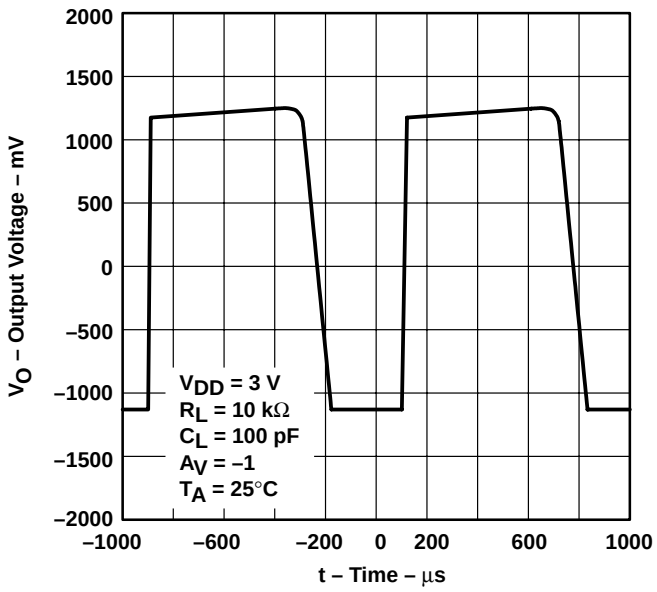


Figure 33

INVERTING LARGE-SIGNAL PULSE RESPONSE

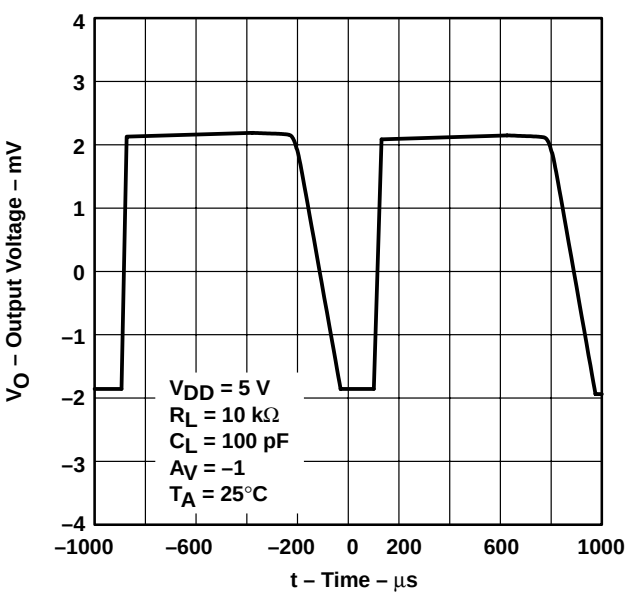


Figure 34

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER LARGE-SIGNAL
PULSE RESPONSE

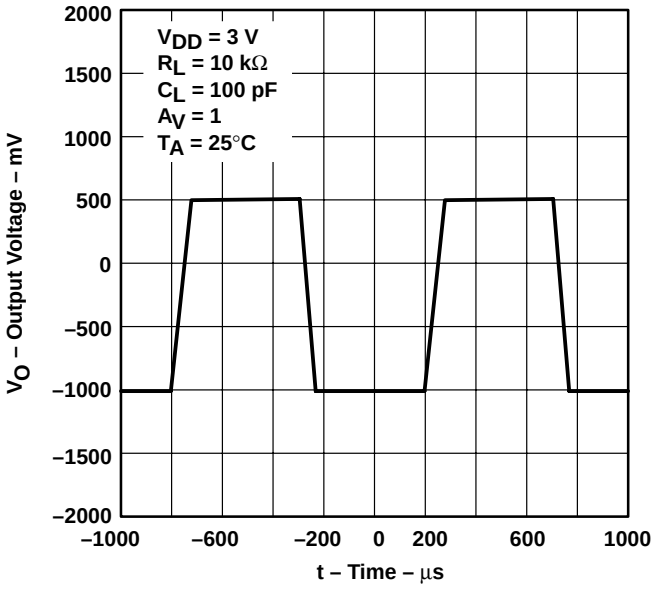


Figure 35

VOLTAGE-FOLLOWER LARGE-SIGNAL
PULSE RESPONSE

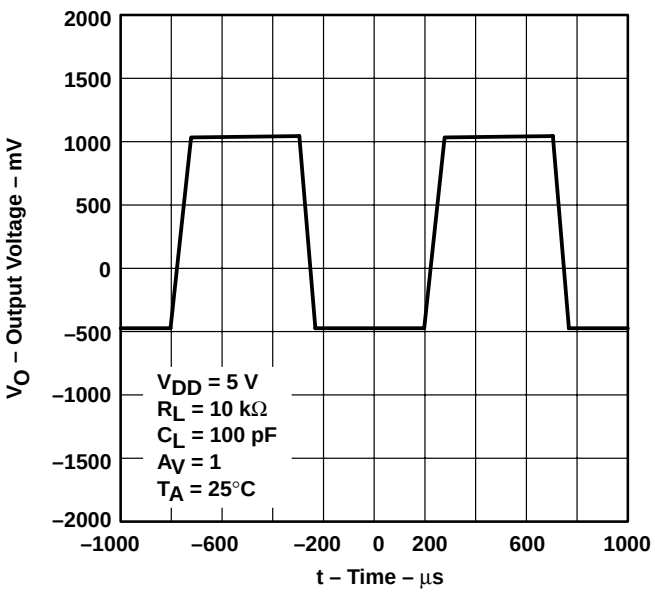


Figure 36

INVERTING SMALL-SIGNAL
PULSE RESPONSE

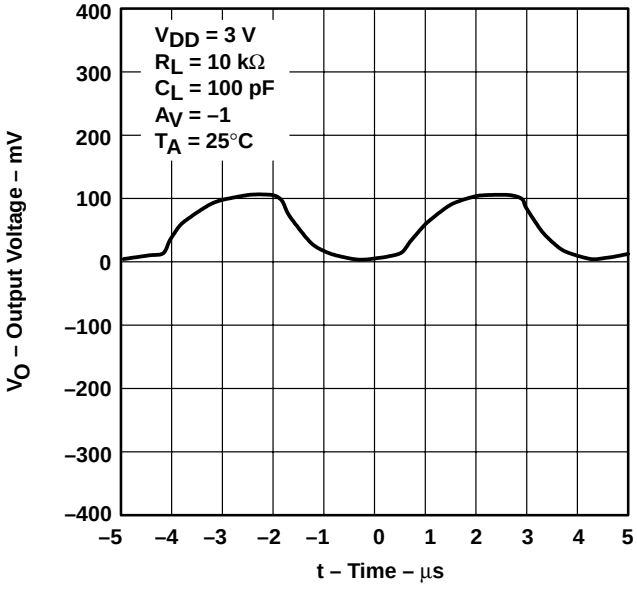


Figure 37

INVERTING SMALL-SIGNAL
PULSE RESPONSE

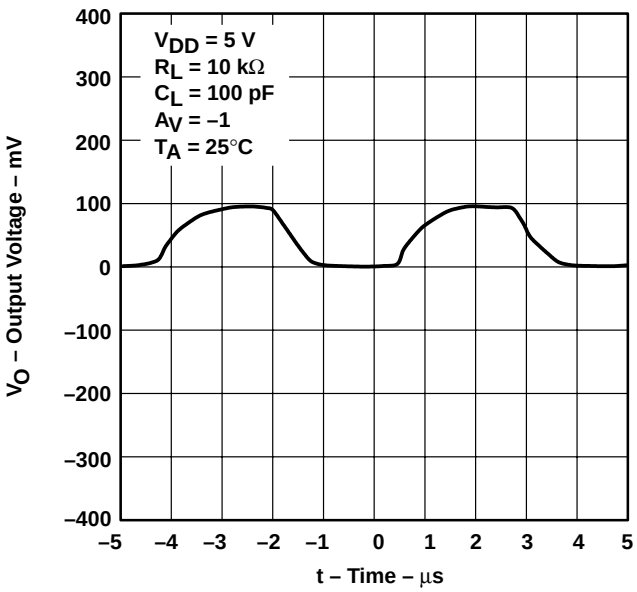


Figure 38

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

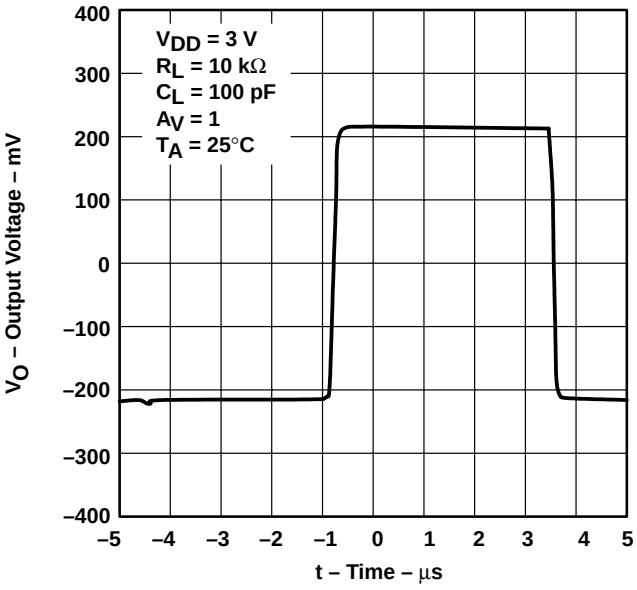


Figure 39

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

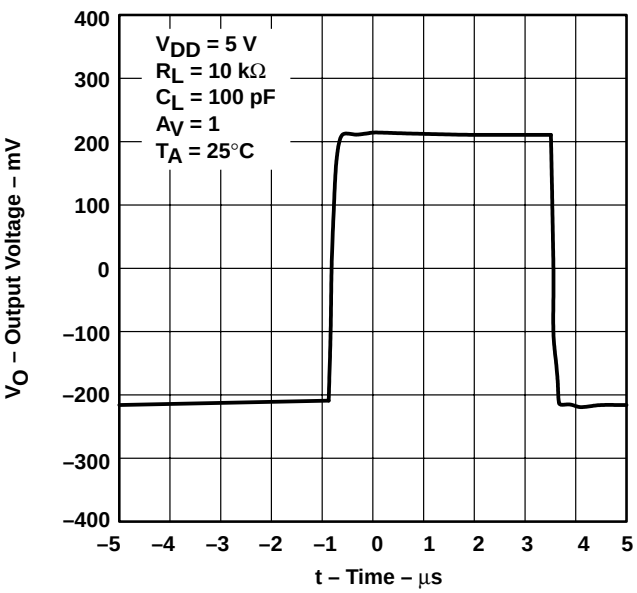


Figure 40

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

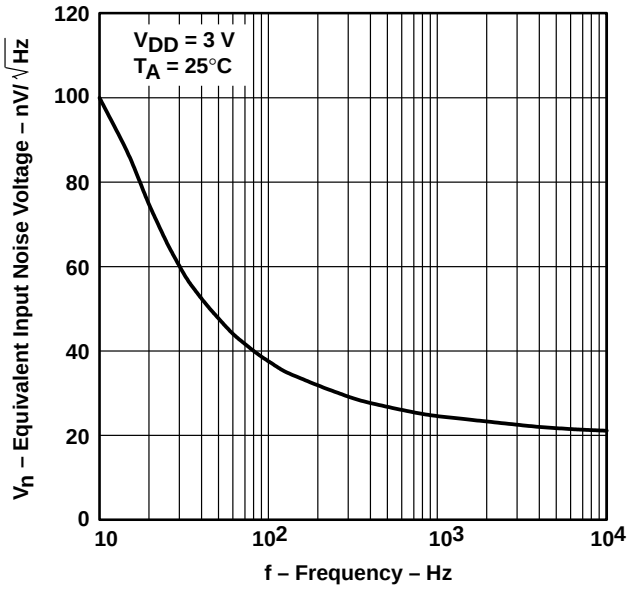


Figure 41

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

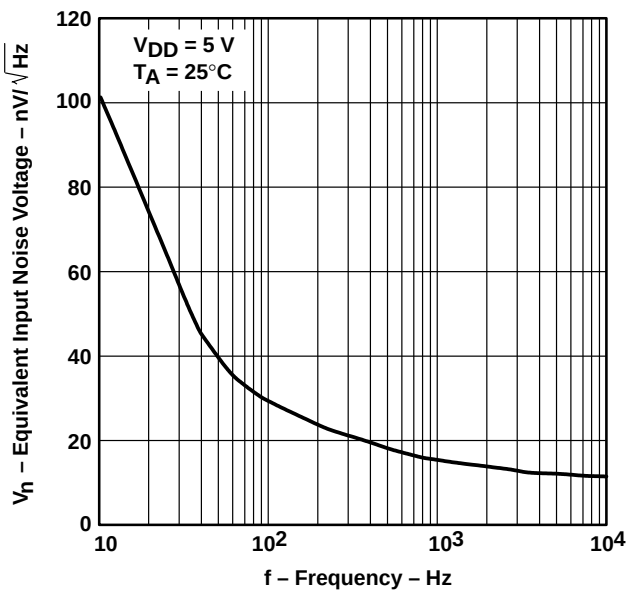


Figure 42

TYPICAL CHARACTERISTICS

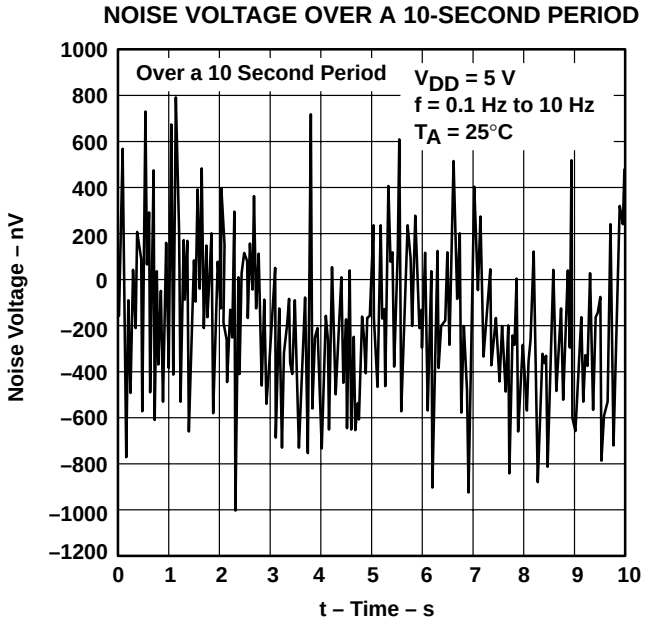


Figure 43

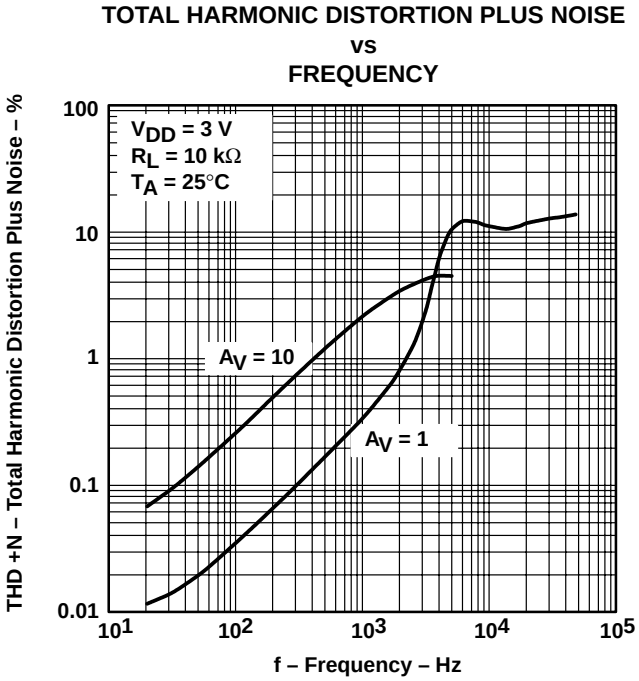


Figure 44

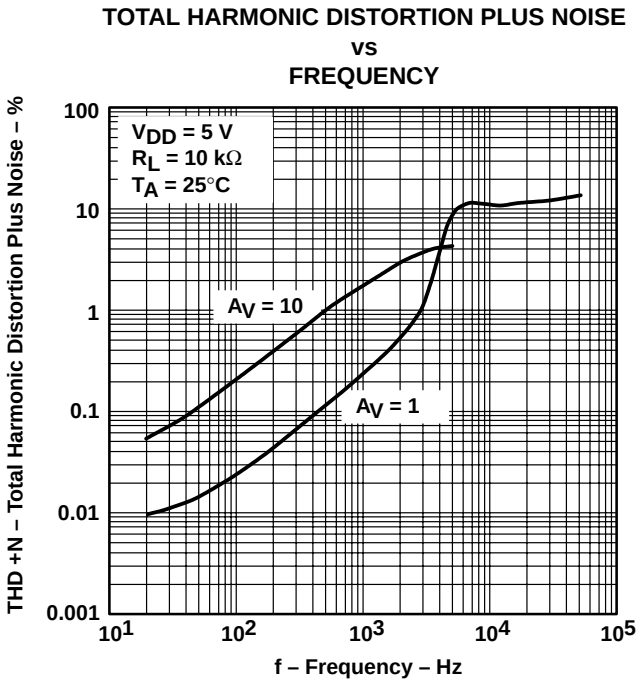


Figure 45

TYPICAL CHARACTERISTICS

GAIN-BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

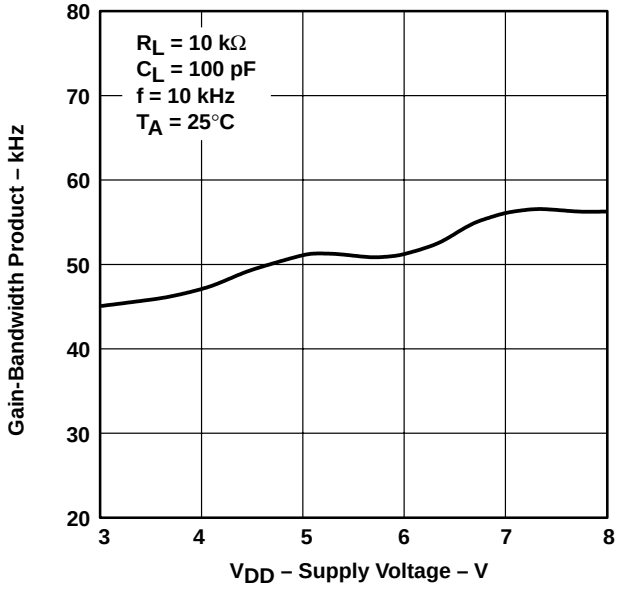


Figure 46

GAIN-BANDWIDTH PRODUCT vs FREE-AIR TEMPERATURE

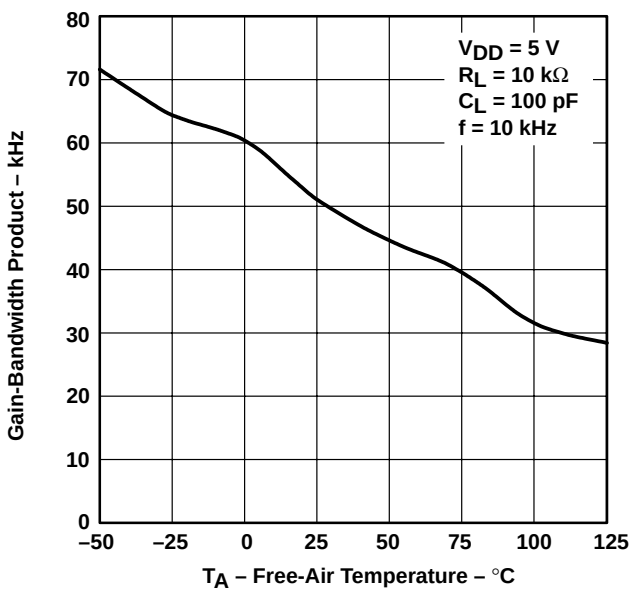


Figure 47

PHASE MARGIN vs LOAD CAPACITANCE

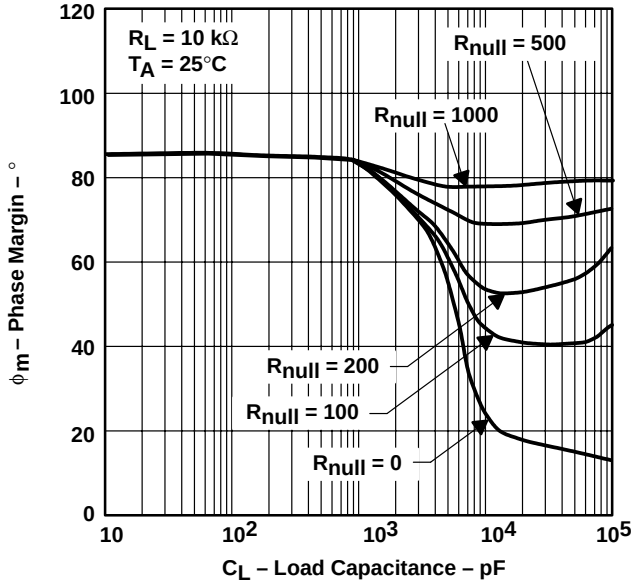


Figure 48

GAIN MARGIN vs LOAD CAPACITANCE

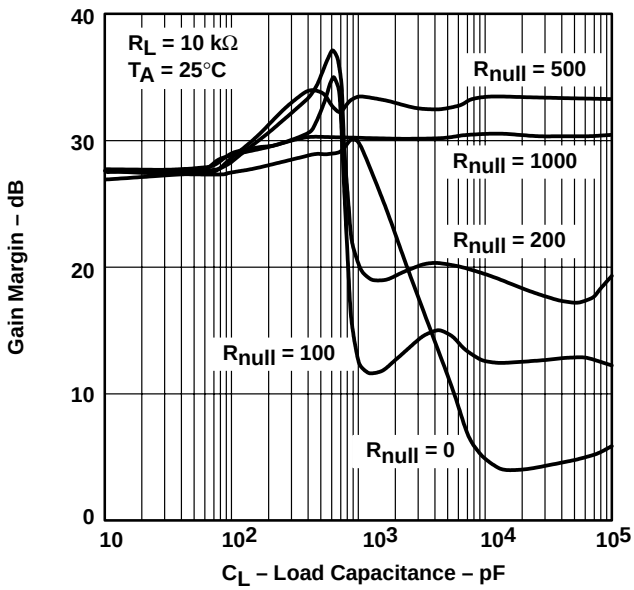


Figure 49

TYPICAL CHARACTERISTICS

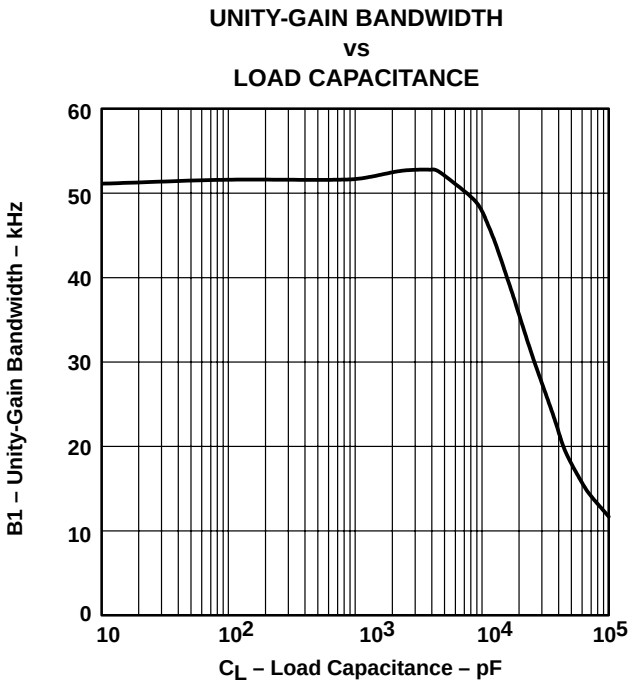
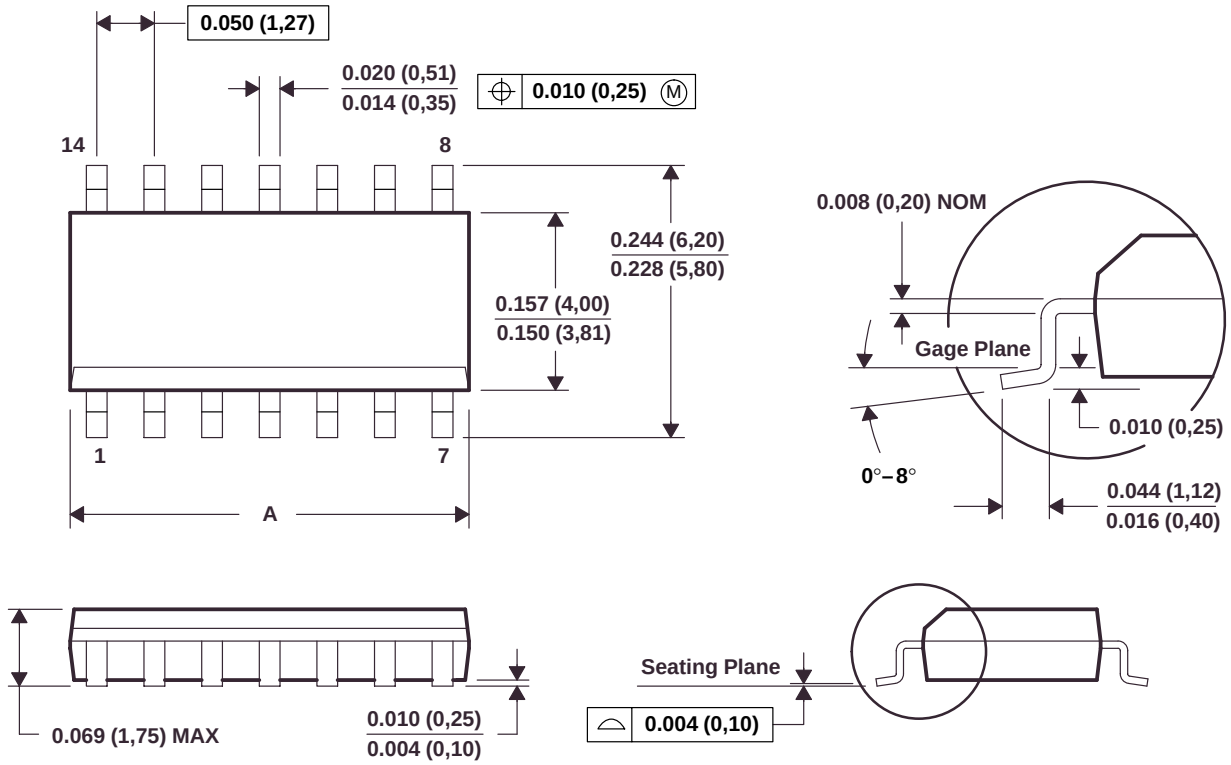


Figure 50

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

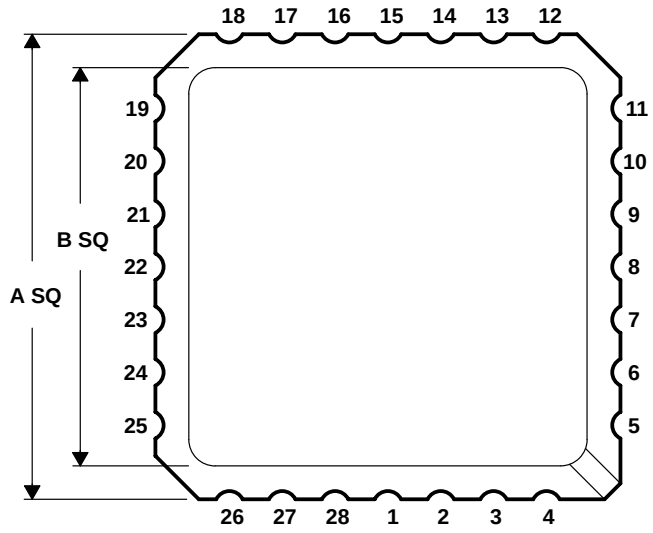
4040047/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

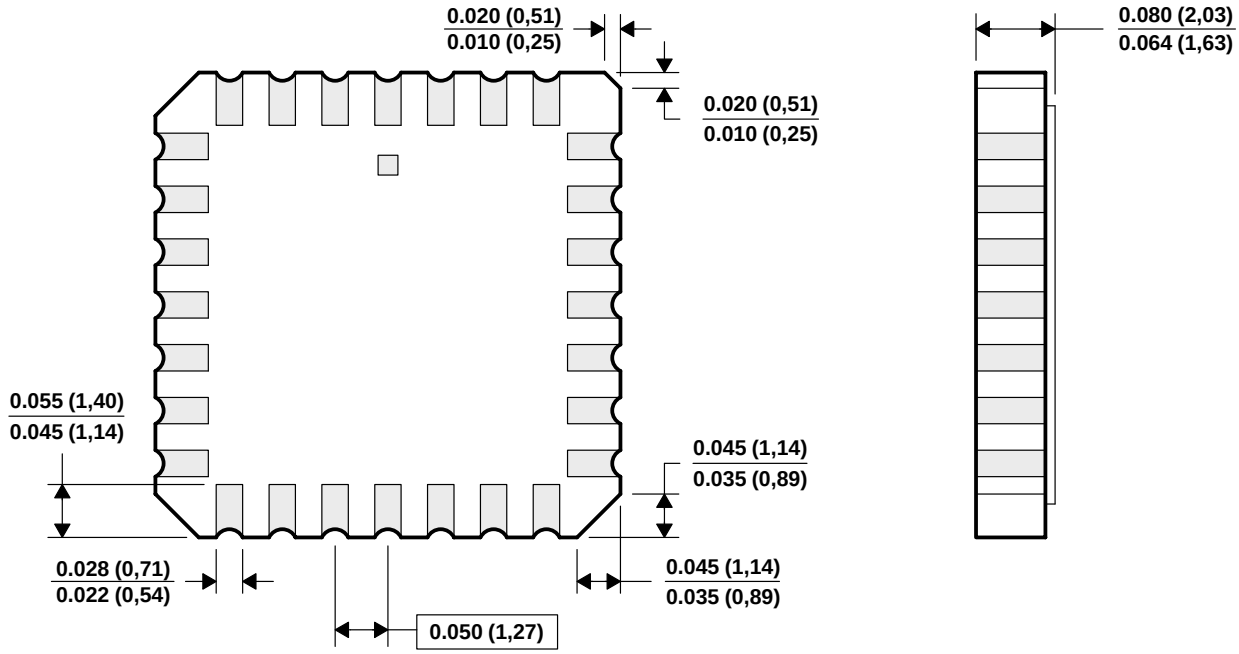
MECHANICAL DATA

FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

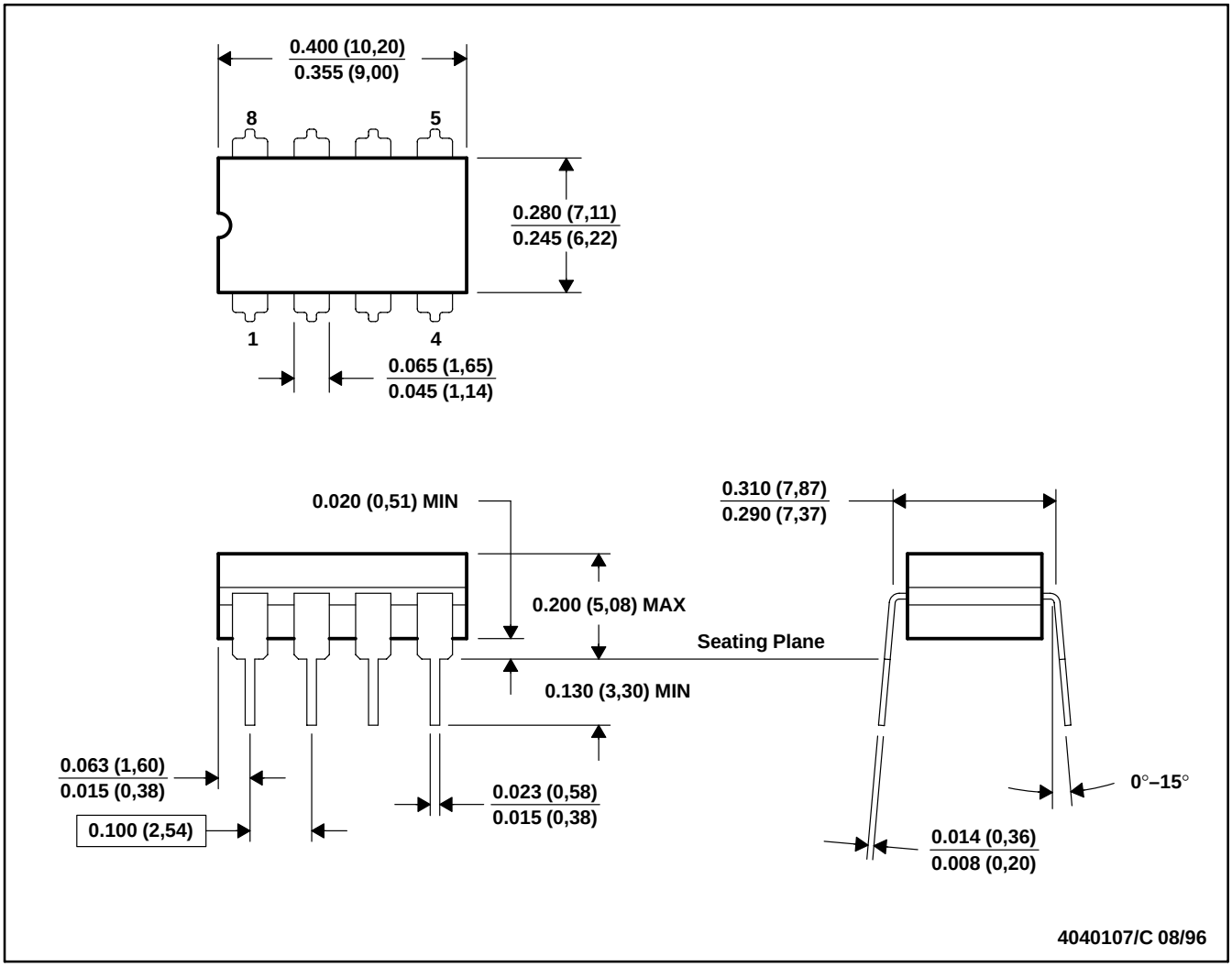


4040140/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

MECHANICAL DATA

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE PACKAGE**

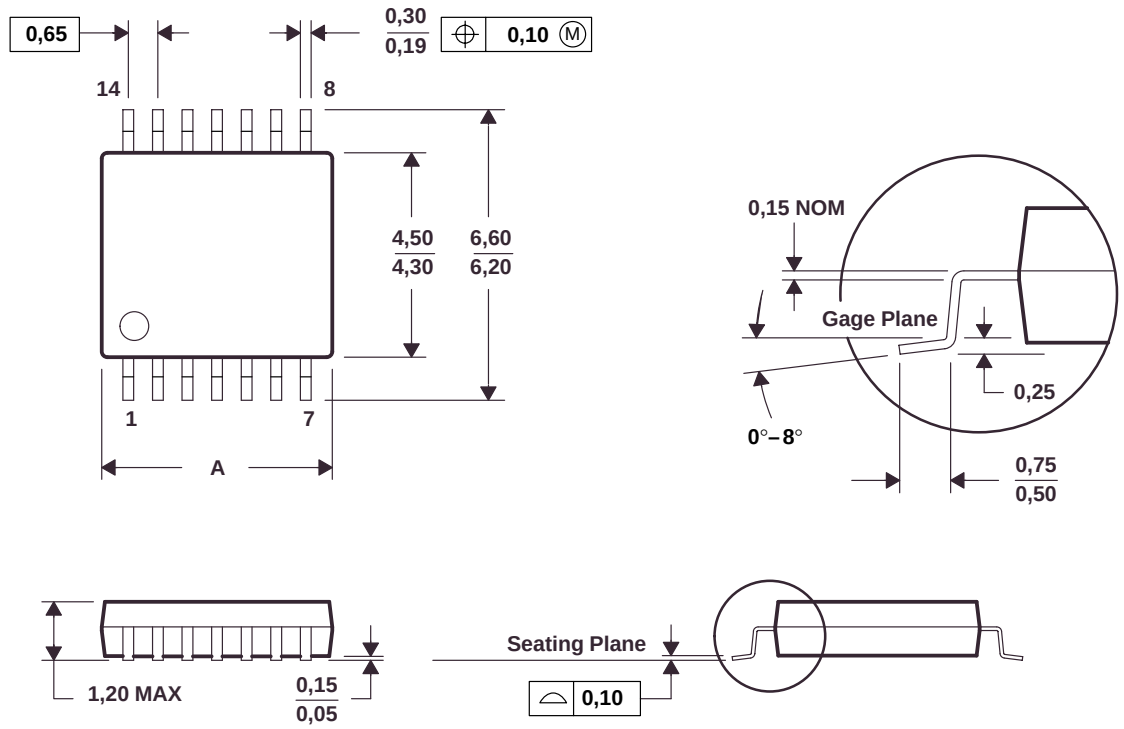


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification on press ceramic glass frit seal only.
E. Falls within MIL-STD-1835 GDIP1-T8

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



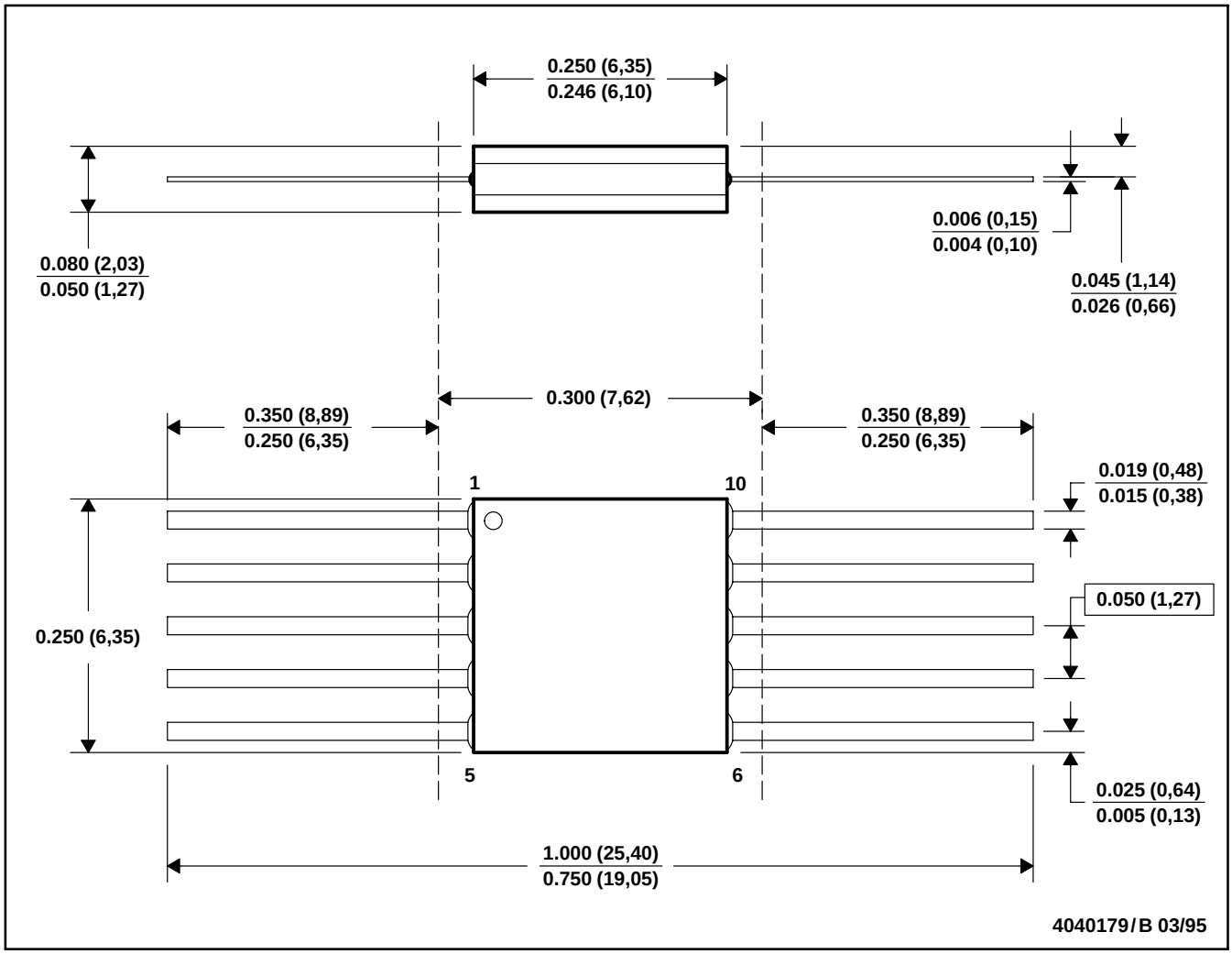
DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/E 08/96

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

MECHANICAL DATA

U (S-GDFP-F10) **CERAMIC DUAL FLATPACK**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1-F10 and JEDEC MO-092AA

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
5962-9751401Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9751401QHA	ACTIVE	CFP	U	10	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9751401QPA	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9751402Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9751402QHA	ACTIVE	CFP	U	10	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9751402QPA	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
TLV2422AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2422AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2422AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2422AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2422AIPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI
TLV2422AIPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2422AIPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2422AMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
TLV2422AMJGB	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
TLV2422AMUB	ACTIVE	CFP	U	10	1	TBD	A42 SNPB	N / A for Pkg Type
TLV2422AQD	ACTIVE	SOIC	D	8	75	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLV2422AQDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2422AQDR	ACTIVE	SOIC	D	8	2500	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLV2422AQDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2422CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2422CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2422CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2422CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2422CPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2422CPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2422ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2422IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2422IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2422IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS &	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
						no Sb/Br)		
TLV2422IPW	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI
TLV2422IPWR	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI
TLV2422MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
TLV2422MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
TLV2422MUB	ACTIVE	CFP	U	10	1	TBD	A42 SNPB	N / A for Pkg Type
TLV2422QD	ACTIVE	SOIC	D	8	75	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLV2422QDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2422QDR	ACTIVE	SOIC	D	8	2500	TBD	CU NIPDAU	Level-1-220C-UNLIM
TLV2422QDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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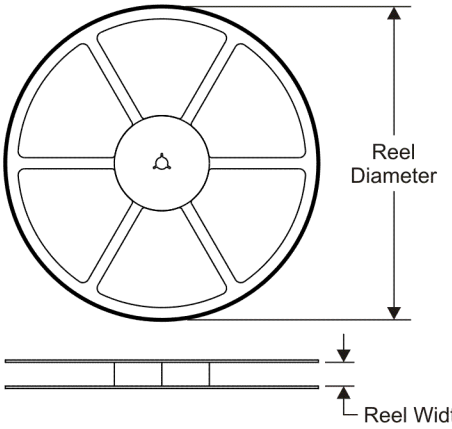
OTHER QUALIFIED VERSIONS OF TLV2422, TLV2422A, TLV2422AM, TLV2422M :
- Automotive: TLV2422-Q1, TLV2422A-Q1

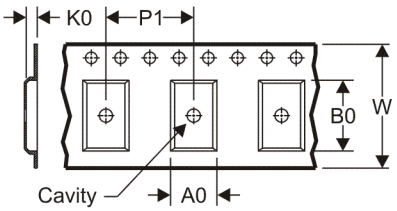
NOTE: Qualified Version Definitions:
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

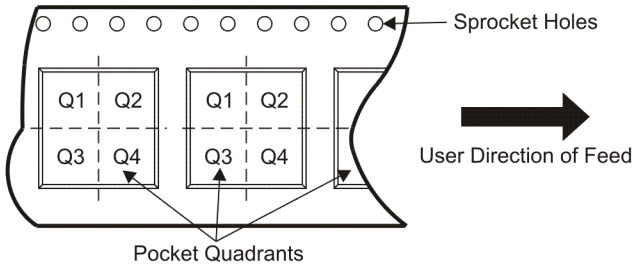


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

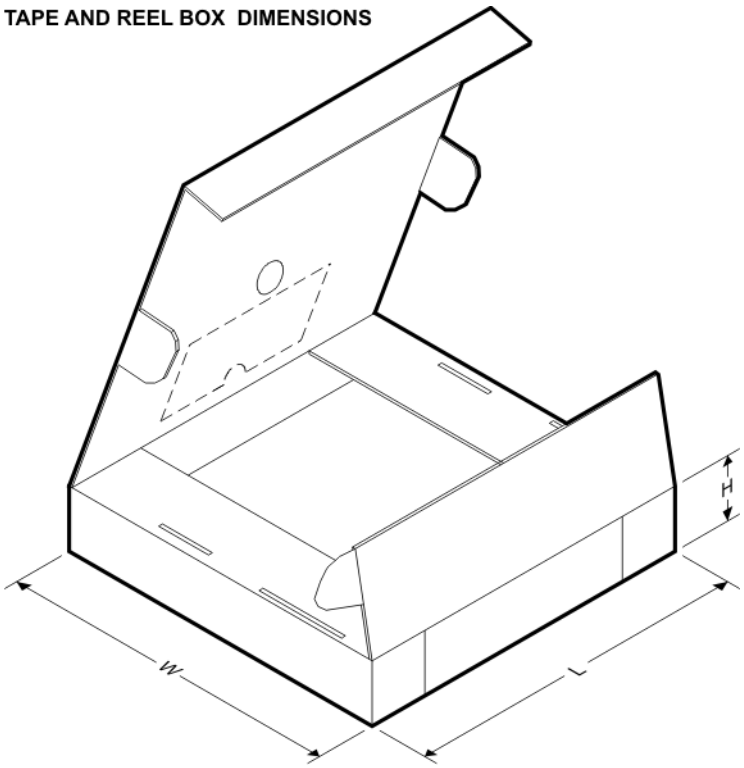
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2422AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2422AIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2422CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2422CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2422IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

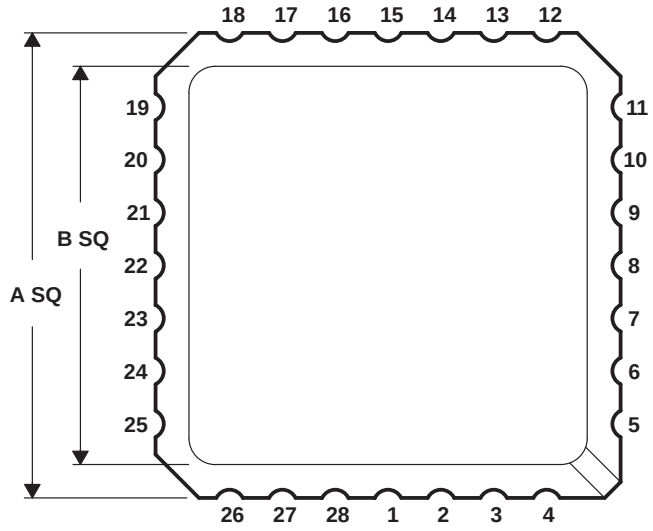


*All dimensions are nominal

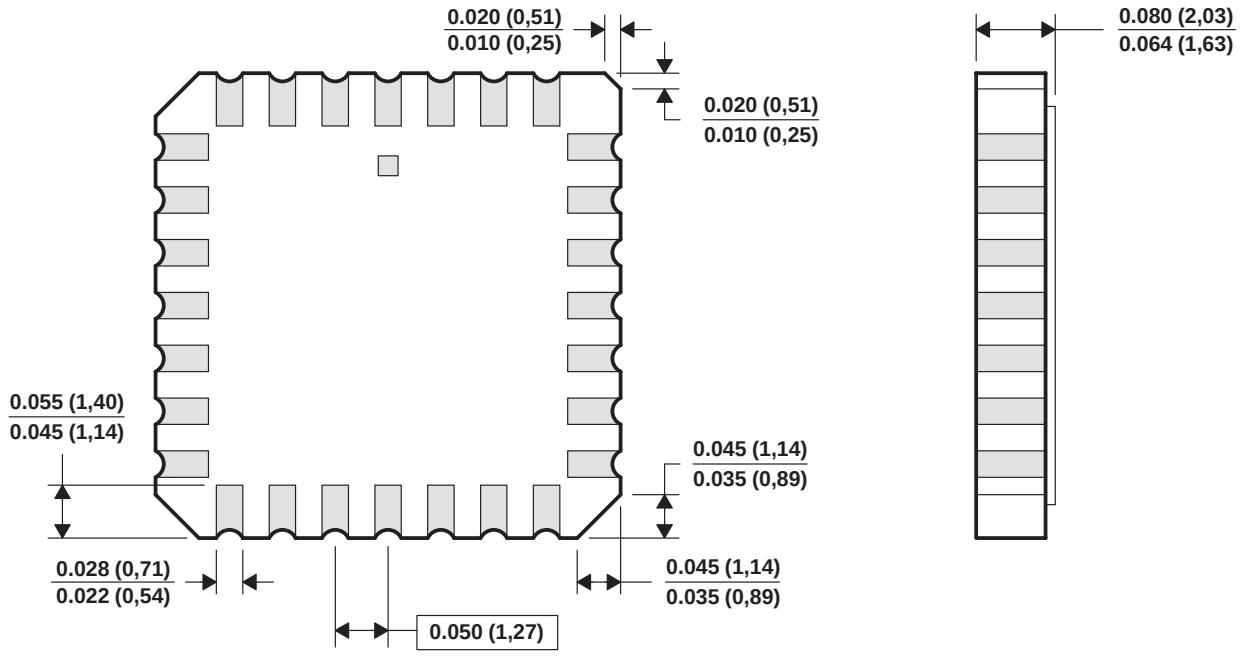
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2422AIDR	SOIC	D	8	2500	346.0	346.0	29.0
TLV2422AIPWR	TSSOP	PW	8	2000	346.0	346.0	29.0
TLV2422CDR	SOIC	D	8	2500	346.0	346.0	29.0
TLV2422CPWR	TSSOP	PW	8	2000	346.0	346.0	29.0
TLV2422IDR	SOIC	D	8	2500	346.0	346.0	29.0

FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

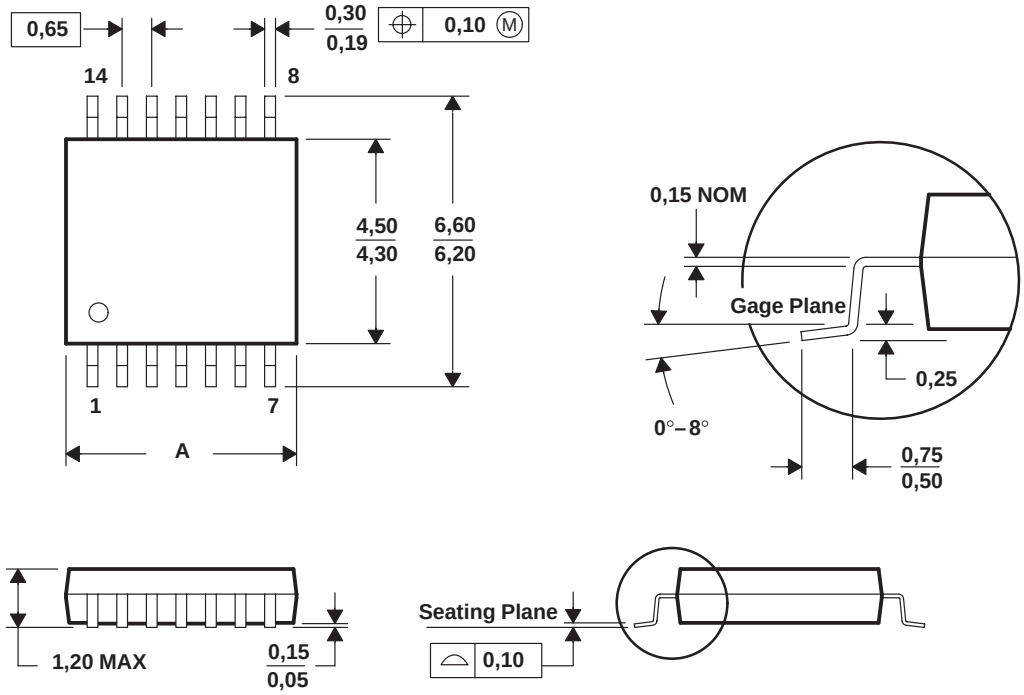


4040140/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

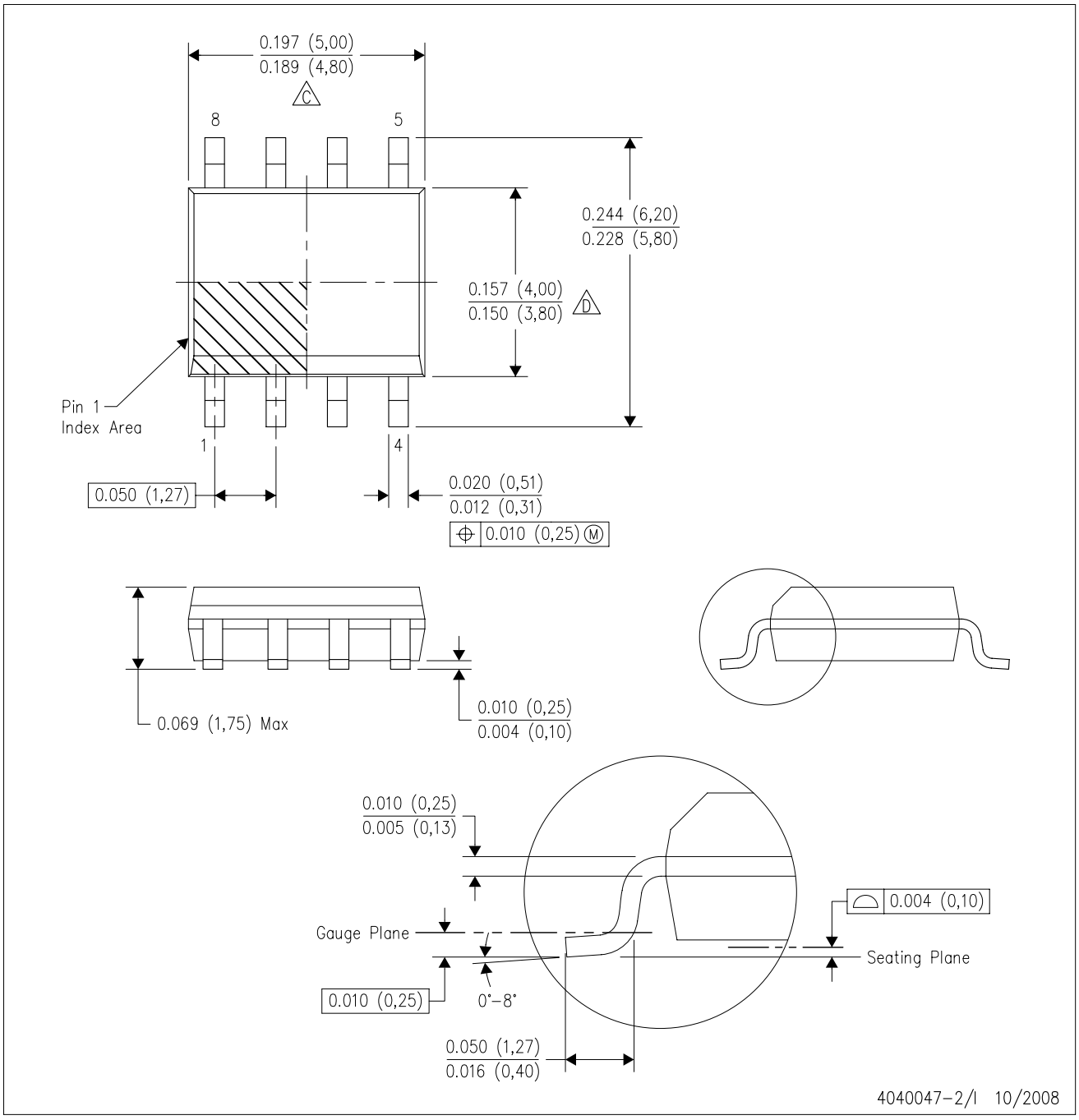


DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

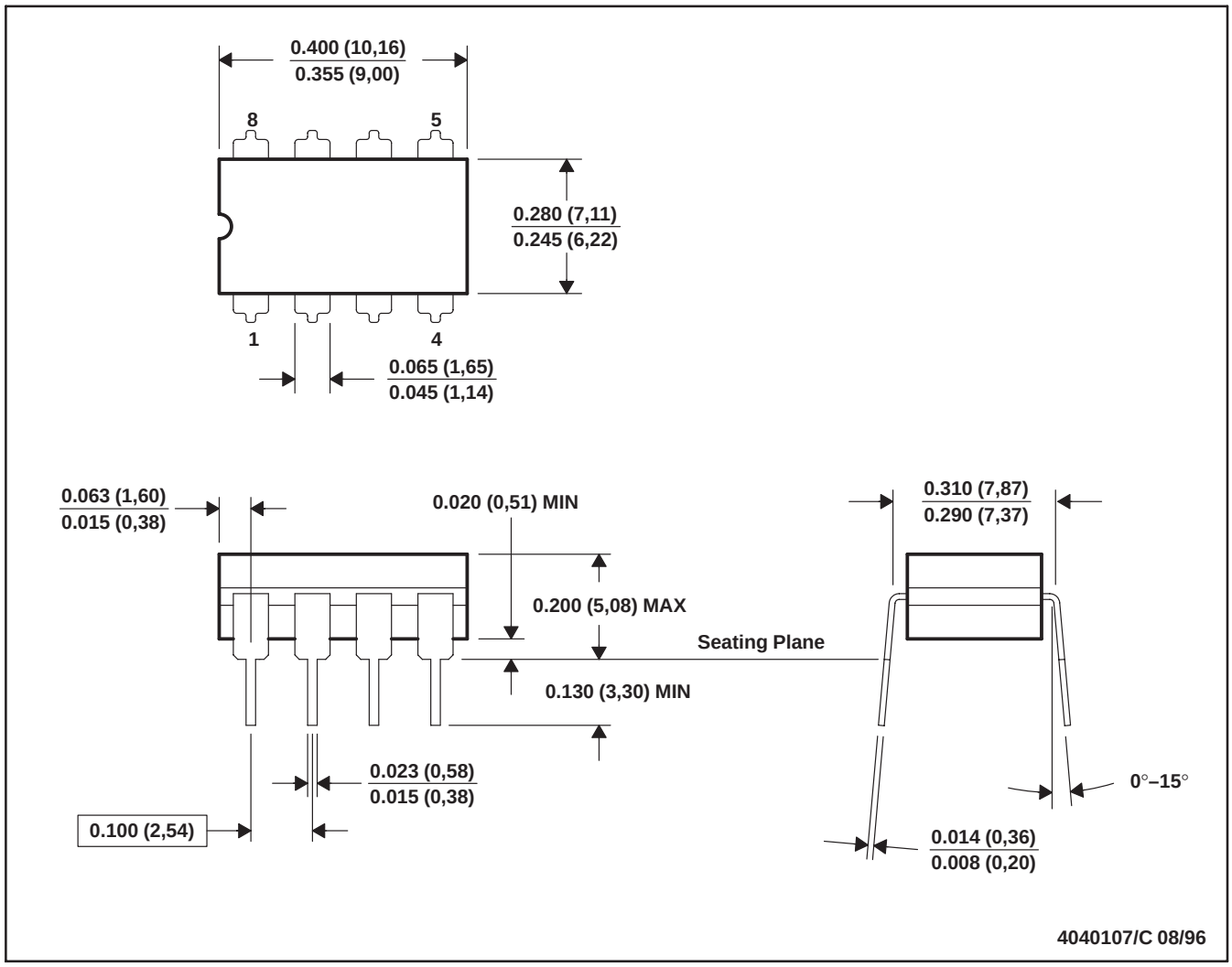
D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

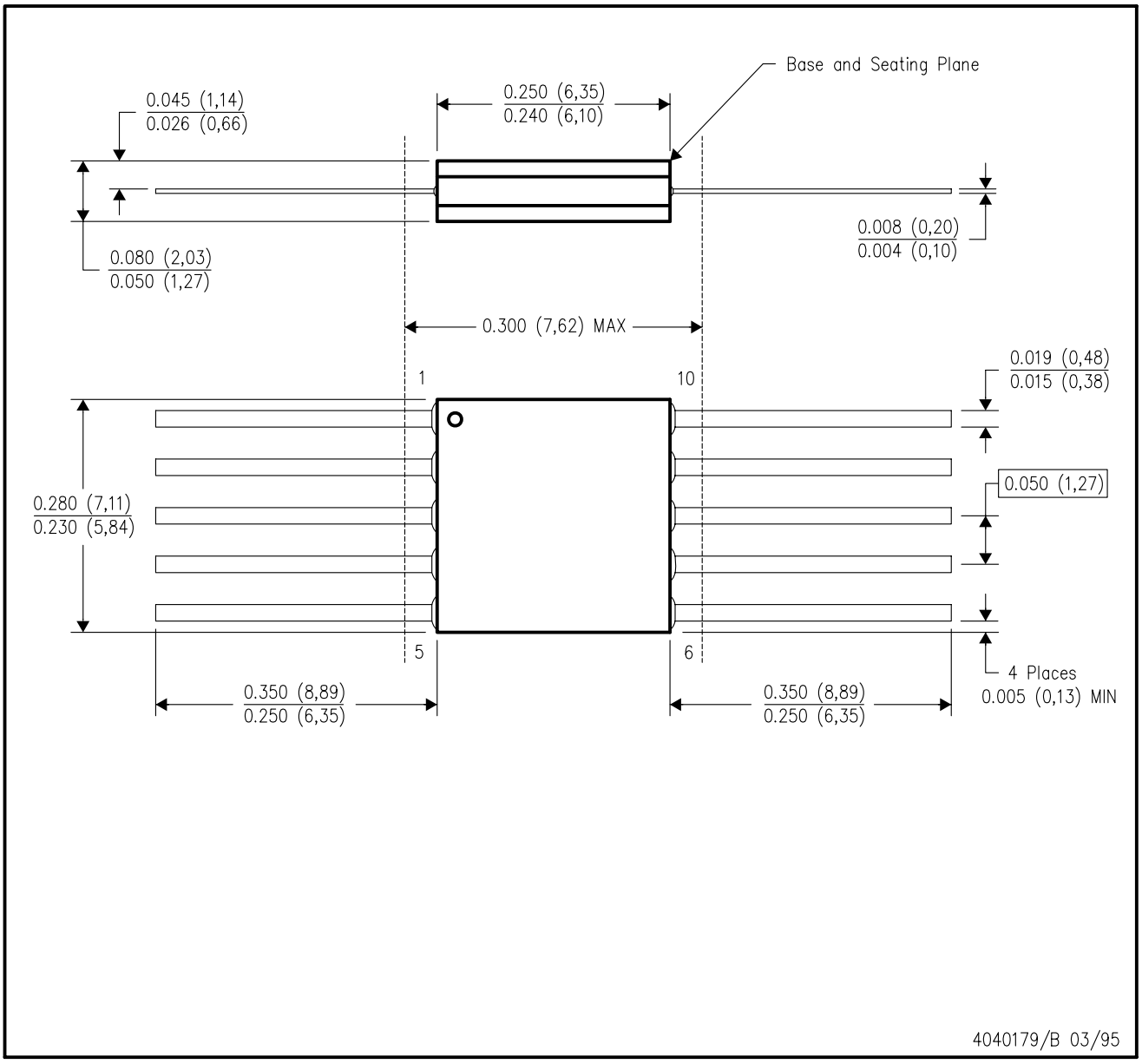
MCER001A – JANUARY 1995 – REVISED JANUARY 1997

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

U (S–GDFP–F10) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F10 and JEDEC MO–092AA

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