National Semiconductor

MM54HC192/MM74HC192 Synchronous Decade Up/Down Counters
MM54HC193/MM74HC193 Synchronous Binary Up/Down Counters

General Description

These high speed synchronous counters utilize advanced silicon-gate CMOS technology to achieve the high noise immunity and low power consumption of CMOS technology, along with the speeds of low power Schottky TTL. The MM54HC192/MM74HC192 is a decade counter, and the MM54HC193/MM74HC193 is a binary counter. Both counters have two separate clock inputs, an UP COUNT input and a DOWN COUNT input. All outputs of the flip-flops are simultaneously triggered on the low to high transition of either clock while the other input is held high. The direction of counting is determined by which input is clocked.

These counters may be preset by entering the desired data on the DATA A, DATA B, DATA C, and DATA D inputs. When the LOAD input is taken low the data is loaded independently of either clock input. This feature allows the counters to be used as divide-by-n counters by modifying the count length with the preset inputs.

In addition both counters can also be cleared. This is accomplished by inputting a high on the CLEAR input. All 4 internal stages are set to a low level independently of either COUNT input.

Both a BORROW and CARRY output are provided to enable cascading of both up and down counting functions. The BORROW output produces a negative going pulse when the counter underflows and the CARRY outputs a pulse when the counter overflows. The counters can be cascaded by connecting the CARRY and BORROW outputs of one device to the COUNT UP and COUNT DOWN inputs, respectively, of the next device.

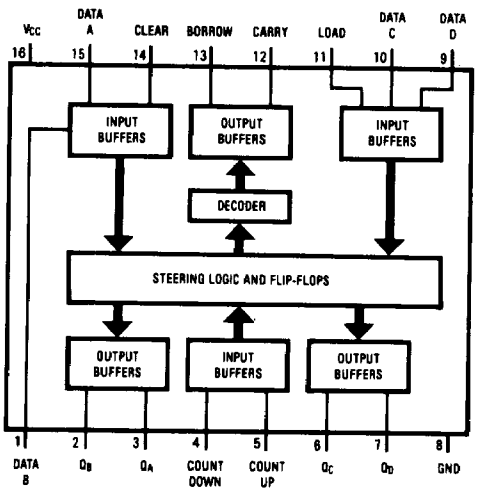
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay, Count up to Q: 28 ns
- Typical operating frequency: 27 MHz
- Wide power supply range: 2–6V
- Low quiescent supply current: 80 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- 4 mA output drive

Connection Diagram

Dual-In-Line Package



TL/F/5011–1

Order Number MM54HC192/193* or MM74HC192/193*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Count		Clear	Load	Function
Up	Down			
↑	H	L	H	Count Up
H	↑	L	H	Count Down
X	X	H	X	Clear
X	X	L	L	Load

H = high level

L = low level

↑ = transition from low-to-high

X = don't care

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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $T_A = 25°C$, $V_{CC} = 5.0V$, $t_r = t_f = 6$ ns, $C_L = 15$ pF (unless otherwise specified)

Symbol	Parameter	Conditions		Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Clock Frequency	Count Up		27	20	MHz
		Count Down		31	24	MHz
t_{PLH}	Maximum Propagation Delay Low to High	Count Up to Carry		17	26	ns
t_{PHL}	Maximum Propagation Delay High to Low			18	24	ns
t_{PLH}	Maximum Propagation Delay Low to High	Count Down to Borrow		16	24	ns
t_{PHL}	Maximum Propagation Delay High to Low			15	24	ns
t_{PLH}	Maximum Propagation Delay Low to High	Count Up Or Down to Q		28	40	ns
t_{PHL}	Maximum Propagation Delay High to Low			36	52	ns
t_{PLH}	Maximum Propagation Delay Low to High	Data or Load to Q		30	42	ns
t_{PHL}	Maximum Propagation Delay High to Low			40	55	ns
t_{PHL}	Maximum Propagation Delay High to Low	Clear to Q		35	47	ns
t_W	Minimum Pulse Width	Clear	'HC192	40	52	ns
			'HC193	20	26	ns
		Load	'HC192	40	52	ns
			'HC193	10	20	ns
		Count Up/Down		15	22	ns
t_{SD}	Minimum Setup time	Data to Load		10	20	ns
t_{HD}	Minimum Hold Time			−3	0	ns
t_{REM}	Minimum Removal Time	Clear Inactive to Clock			10	ns

AC Electrical Characteristics $V_{CC} = 2.0V$ to $6.0V$, $C_L = 50$ pF, $t_r = t_f = 6$ ns

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Clock Frequency	Count Up	2.0V	5	3	2.5	2 MHz
			4.5V	25	18	14	12 MHz
			6.0V	29	20	16	13 MHz
		Count Down	2.0V	5	4	3	2 MHz
			4.5V	27	20	16	11 MHz
			6.0V	31	23	18	12 MHz
t_{PLH}	Maximum Propagation Delay Low to High	Count Up to Carry	2.0V	30	140	175	210 ns
			4.5V	13	28	35	42 ns
			6.0V	11	24	30	36 ns
t_{PHL}	Maximum Propagation Delay High to Low		2.0V	39	130	163	195 ns
			4.5V	16	26	33	39 ns
			6.0V	14	22	28	33 ns

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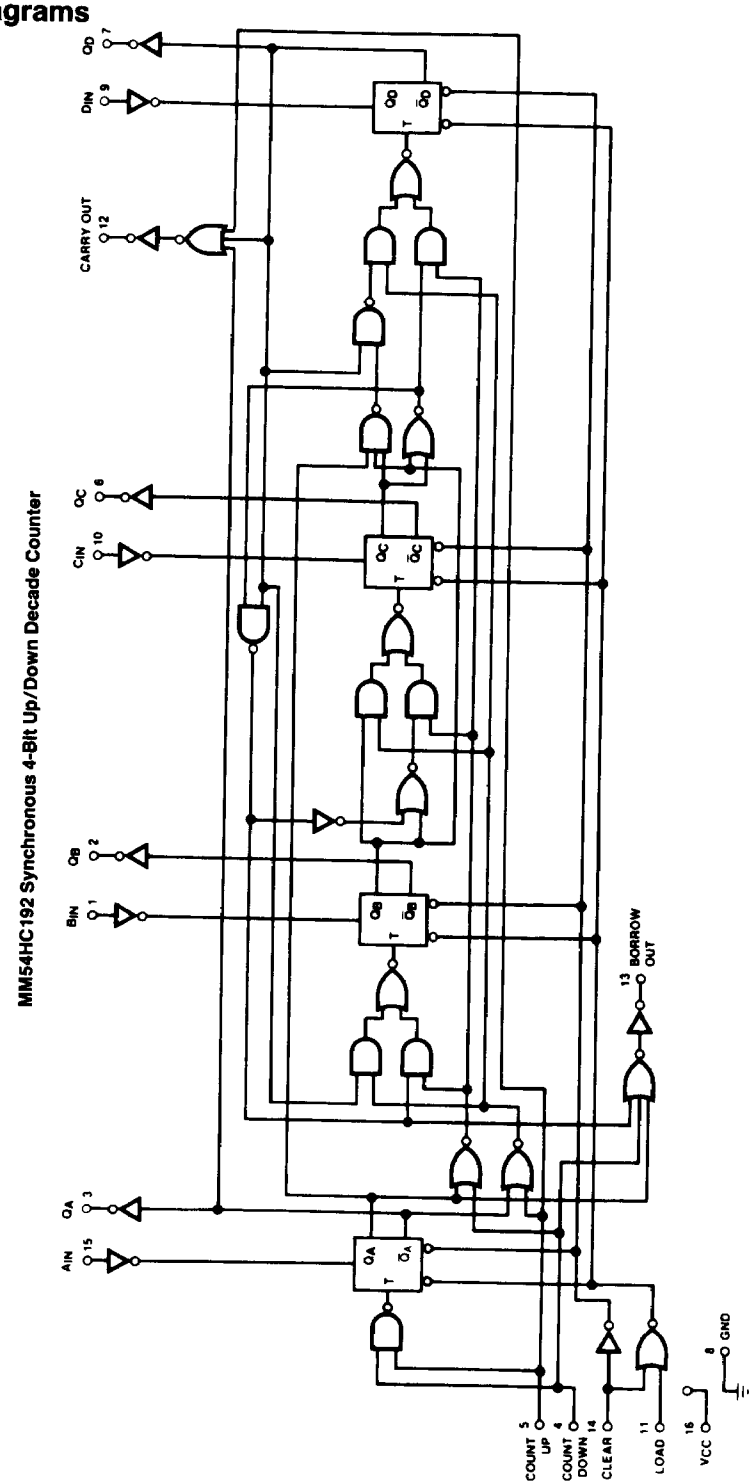
AC Electrical Characteristics (Continued) V_{CC} = 2.0V to 6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to 85°C	54HC $T_A = -55$ to 125°C	Units
				Typ	Guaranteed Limits		
t_{PLH}, t_{PHL}	Maximum Propagation Delay	Count Down to Borrow	2.0V	39	130	163	195	ns
			4.5V	16	26	33	39	ns
			6.0V	14	22	28	33	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_{PLH}	Maximum Propagation Delay Low to High	Count Up Or Down to Q	2.0V	77	215	269	323	ns
			4.5V	35	43	54	65	ns
			6.0V	30	37	46	55	ns
t_{PHL}	Maximum Propagation Delay High to Low		2.0V	95	275	344	413	ns
			4.5V	45	55	69	83	ns
			6.0V	38	47	59	71	ns
t_{PLH}	Maximum Propagation Delay Low to High	Data or Load to Q	2.0V	85	230	288	345	ns
			4.5V	37	46	58	69	ns
			6.0V	30	39	49	59	ns
t_{PHL}	Maximum Propagation Delay High to Low		2.0V	102	290	363	435	ns
			4.5V	47	58	73	87	ns
			6.0V	39	49	61	74	ns
t_{PHL}	Maximum Propagation Delay High to Low	Clear to Q	2.0V	85	265	331	398	ns
			4.5V	42	53	66	80	ns
			6.0V	38	45	56	68	ns
t_W	Minimum Pulse Width	Clear or Load 'HC192	2.0V	119	260	325	390	ns
			4.5V	42	52	65	78	ns
			6.0V	38	45	56	68	ns
		Load 'HC193	2.0V	31	100	125	150	ns
			4.5V	10	20	25	30	ns
			6.0V	9	17	21	26	ns
		Count Up/Down	2.0V	43	110	138	165	ns
			4.5V	17	22	28	33	ns
			6.0V	15	19	24	29	ns
		Clear 'HC193	2.0V	70	130	163	195	ns
			4.5V	21	26	33	39	ns
			6.0V	19	22	28	33	ns
t_{SD}	Minimum Setup Time	Data To Load	2.0V	30	100	125	150	ns
			4.5V	10	20	25	30	ns
			6.0V	9	17	22	25	ns
t_{HD}	Minimum Hold Time		2.0V	−30	0	0	0	ns
			4.5V	−3	0	0	0	ns
			6.0V	−3	0	0	0	ns
t_{REM}	Minimum Removal Time	Clear Inactive to Clock	2.0V	−20	10	10	10	ns
			4.5V	−3	10	10	10	ns
			6.0V	−2	10	10	10	ns
t_r, t_f	Maximum Count Up or Down Input Rise & Fall Time		2.0V		500	500	500	ns
			4.5V		300	300	300	ns
			6.0V		200	200	200	ns
C_{IN}	Input Capacitance			5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance (Note 5)			100				pF

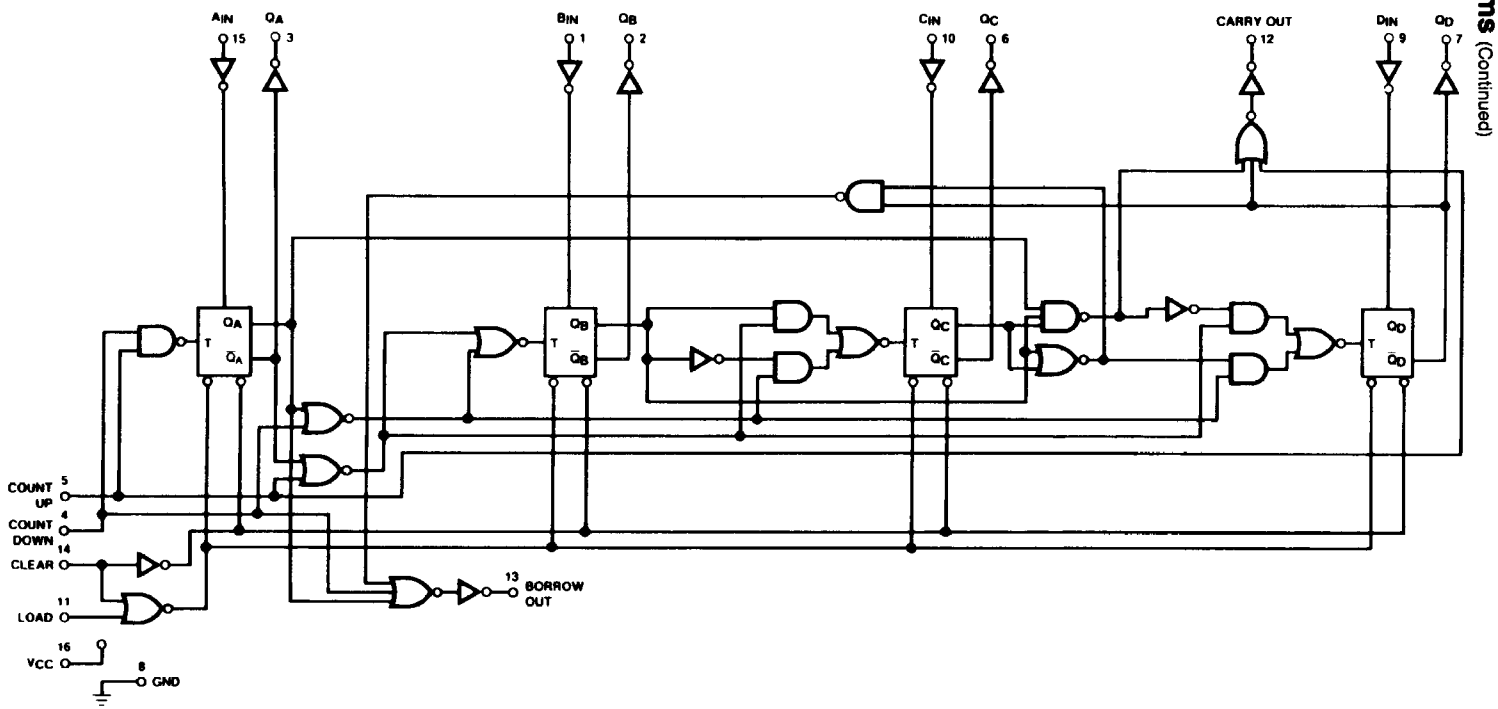
Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Logic Diagrams



Logic Diagrams (Continued)

MM54HC193 Synchronous 4-Bit Up/Down Binary Counter



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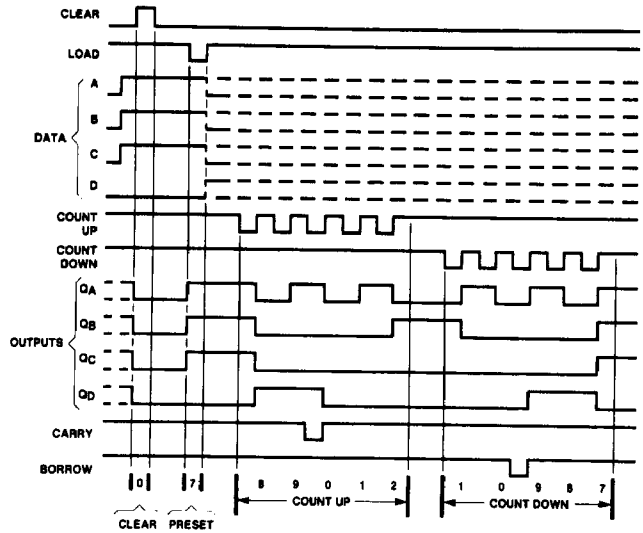
Logic Waveforms

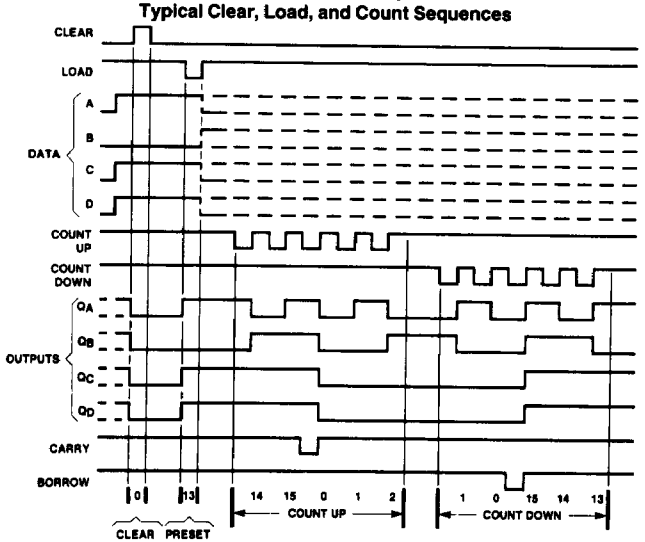
'HC192 Synchronous Decade Counters
Typical Clear, Load, and Count Sequences



TL/F/5011–4

Sequences:
(1) Clear outputs to zero
(2) Load (preset) to BCD seven.
(3) Count up to eight, nine, carry, zero, one and two.
(4) Count down to one, zero, borrow, nine, eight, and seven.

'HC193 Synchronous Binary Counters
Typical Clear, Load, and Count Sequences



TL/F/5011–5

Sequence:
(1) Clear outputs to zero.
(2) Load (preset) to binary thirteen
(3) Count up to fourteen, fifteen, carry, zero, one, and two.
(4) Count down to one, zero, borrow, fifteen, fourteen, and thirteen.
Note A: Clear overrides load data, and count inputs.
Note B: When counting up, count-down input must be high; when counting down, count-up input must be high.