National Semiconductor

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CLC505
High Speed, Programmable Supply Current, Monolithic Op Amp

General Description

The CLC505 is a monolithic, high speed op amp with a unique combination of high performance, low power consumption, and flexibility of application. The supply current is programmable over a 10 to 1 continuous range with a single resistor, R_p. This feature enables the amplifier to be used in a wide variety of high performance applications. Typical performance at any supply current is exceptional:

Parameter	Supply Current (I_{CC})			Units
	9mA	3.4mA	1mA	
−3dB Bandwidth	150	100	50	MHz
Settling Time	12	14	35	nsec
Slew Rate	1700	1200	800	V/µsec
Output Current	45	25	7	mA

The CLC505's combination of high performance, low power consumption, and large signal performance makes the CLC505 ideal for a wide variety of remote site equipment applications, such as battery powered test instrumentation and communications gear. Some other power applications are video switching matrices, ATE, and phased-array radar systems.

The CLC505 has been designed for ease of use and has been specified to ensure design confidence and final system predictability. The product performance is specified for 1mA, 3mA ad 9mA supply current. The CLC505 is available in 8-pin Dip SOIC packages offered for the industrial temperature range.

Enhanced Solutions (Military/Aerospace)

SMD Number: contact factory

Space level versions also available.

For more information, visit http://www.national.com/mil

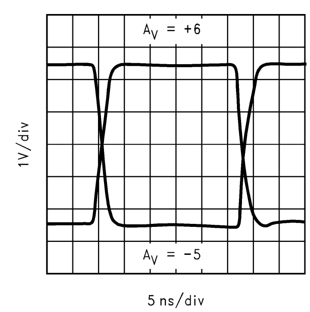
Features

- 10mW power consumption with 50MHz BW
- Single resistor programming of supply current
- 3.4mA I_{CC} provides 100MHz bandwidth and 14ns settling (0.05%)
- Fast disable capability
- 0.04% differential gain at I_{CC} = 3.4mA
- 0.06% differential phase at I_{CC} = 3.4mA

Applications

- Low power battery applications
- Remote site instrumentation
- Mobile communications gear
- Video switching matrix
- Phased-array radar

Large-Signal Pulse Response



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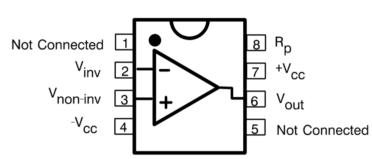
Connection Diagram



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Pinout
DIP & SOIC

Ordering Information

Package	Temperature Range Industrial	Part Number	Package Marking	NSC Drawing
8-pin plastic DIP	−40˚C to +85˚C	CLC505AJP	CLC505AJP	N08E
8-pin plastic SOIC	−40˚C to +85˚C	CLC505AJE	CLC505AJE	M08A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	±7V
I_{OUT} Output is short circuit protected to ground, but maximum reliability will be maintained if I_{OUT} does not exceed...	60mA
Common Mode Input Voltage	$\pm V_{CC}$
Differential Input Voltage	10V
Junction Temperature	+150˚C
Operating Temperature	−40˚C to +85˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Solder Duration (+300˚C)	10 sec
ESD rating (human body model)	2000V

Operating Ratings

Thermal Resistance (SOIC)

θ_{JC}	60˚C/W
θ_{JA}	140˚C/W

Electrical Characteristics

A_V = +6, V_{CC} = ±5V, R_f = 1000Ω, C_p = 100pF; unless specified

Symbol	Parameter	Conditions	Typ	Max/Min Ratings (Note 2)			Units
Ambient Temperature		CLC505AJ	+25˚C	−40˚C	+25˚C	+85˚C	
Frequency Domain Response							
SSBW	-3dB Bandwidth	V_{OUT} <2V_{PP}	150	>115	>115	>100	MHz
LSBW	-3dB Large Signal	V_{OUT} <5V_{PP}	135	>95	>95	>80	MHz
	Gain Flatness	V_{OUT} < 2V_{PP}					
GFPL	Peaking	<25/20/10MHz (Note 7)	0	<0.4	<0.3	<0.4	dB
GFPH	Peaking	>25/20/10MHz (Note 7)	0	<0.6	<0.5	<0.6	dB
GFR	Rolloff	<50/40/20MHz (Note 7)	0.2	<1.0	<1.0	<1.3	dB
LPD	Linear Phase Deviation	DC to 50/40/20MHz (Note 7)	0.6	<1.0	<1.0	<1.2	deg
Time Domain Response							
TRS	Rise and Fall Time	2V Step	2.3	<3.0	<3.0	<3.5	ns
TRL		5V Step	2.6	<3.7	<3.7	<4.4	ns
TSP	Settling time to 0.1/0.05/0.05% (Note 7)	2V Step	12	<16	<16	<16	ns
OS	Overshoot	2V Step	5	<15	<12	<15	%
SR	Slew Rate (A_V +2)		1700	>1000	>1200	>1200	V/µs
Distortion And Noise Response							
HD2	2nd Harmonic Distortion	2V_{PP},20/10/5MHz (Note 7)	−50	<−40	<−45	<−45	dBc
HD3	3rd Harmonic Distortion	2V_{PP},20/10/5MHz (Note 7)	−65	<−55	<−55	<−55	dBc
	Equivalent Input Noise						
SNF	Noise Floor	>1MHz	−156	<−154	<−154	<−153	dBm (1Hz)
INV	Integrated Noise	1MHz to 200/200/100MHz (Note 7)	50	<65	<65	<70	µV
DG	Differential Gain (Note 6)		0.04	-	-	-	%
DP	Differential Phase (Note 6)		0.06	-	-	-	deg
Static, DC Performance							
VIO	Input Offset Voltage (Note 3)		2	<±12.8	<±8.0	<±14	mV
DVIO	Average Temperature Coefficient		30	<±50	-	<±50	µV/˚C
IBN	Input Bias Current (Note 3)	Non Inverting	8	<±36	<±18	<±18	µA
DIBN	Average Temperature Coefficient		80	<±225	-	<±100	nA/˚C
IBI	Input Bias Current (Note 3)	Inverting	10	<±60	<±38	<±40	µA
DIBI	Average Temperature Coefficient		80	<±275	-	<±125	nA/˚C
PSRR	Power Supply Rejection Ratio		50	>45	>48	>45	dB
CMRR	Common Mode Rejection Ratio		50	>45	>48	>45	dB

Electrical Characteristics (Continued)

A_V = +6, V_{CC} = ±5V, R_f = 1000Ω, C_p = 100pF; unless specified

Symbol	Parameter	Conditions	Typ	Max/Min Ratings (Note 2)			Units
Static, DC Performance							
ICC	**Supply Current** (Note 3)	**No Load, Quiescent**	**9**	**<11**	**<11**	**<12**	**mA**
Miscellaneous Performance							
RIN	Non-Inverting Input	Resistance	1200	>400	>800	>1600	kΩ
CIN		Capacitance	1	<2	<2	<2	pF
RO	Output Impedence	At DC	0.2	<1.2	<0.3	<0.2	ohm
VO	Output Voltage Range	No Load	±3.3	>±2.8	>±3.0	>±3.0	V
CMIR	Common Mode Input Range	For Rated Performance	±2.2	>±1.5	>±1.8	>±2.0	V
IO	Output Current	−40˚C to +85˚C	±45	>±20	>±36	>±36	mA

Electrical Characteristics

A_V = +6, V_{CC} = ±5V, R_f = 1000Ω, C_P = 100pF; unless specified

	SUPPLY CURRENT I_{CC} (TYP) = 3.4mA R_p =100kΩ, R_L = 500Ω				SUPPLY CURRENT I_{CC} (TYP) = 1mA R_p = 300kΩ, R_L =1000Ω				
Symbol	**Typ**	**Max & Min Ratings**			**Typ**	**Max & Min Ratings**			**Units**
	+25˚C	−40˚C	+25˚C	+85˚C	+25˚C	−40˚C	+25˚C	+85˚C	
SSBW	100	>80	>80	>65	50	>30	>35	>30	MHz
LSBW	80	>50	>50	>40	33	–1	>20	>18	MHz
GFPL	0	<0.3	<0.2	<0.3	0	<0.2	<0.1	<0.2	dB
GFPH	0	<0.5	<0.4	<0.5	0	<0.3	<0.2	<0.3	dB
GFR	0.2	<1.0	<1.0	<1.3	0.5	<1.0	<1.0	<1.3	dB
LPD	0.5	<1.0	<1.0	<1.2	0.2	<0.5	<0.5	<1.0	deg
TRS	3.5	<4.4	<4.4	<5.4	7	<12	<10	<12	ns
TRL	4.4	<7.0	<7.0	<8.8	9	–1	<18	<20	ns
TSP	14	<22	<22	<22	35	<70	<60	<60	ns
OS	2	<12	<10	<12	0	<8	<5	<8	%
SR	1200	>700	>800	>800	800	>500	>600	>600	V/µs
HD2	−55	<−40	<−45	<−45	−55	<−40	<−45	<−45	dBc
HD3	−65	<−55	<−55	<−55	−65	<−55	<−55	<−55	dBc
SNF	−155	<−153	<−153	<−152	−152	<−150	<−150	<−149	dBm (1Hz)
INV	56	<70	<70	<80	55	<70	<70	<80	µV
DG	0.04	–	–	–	0.1	–	–	–	%
DP	0.06	–	–	–	0.1	–	–	–	deg
VIO	3	<±11.8	<±7.0	<±13	3	<±13.0	<±7.0	<±14.5	mV
DVIO	40	<±60	–	<±60	50	<±75	–	<±75	µV/˚C
IBN	2	<±12	<±6	<±6	1	<±5.0	<±2.5	<±2.5	µA
DIBN	30	<±75	–	<±50	10	<±32	–	<±30	nA/˚C
IBI	4	<±22	<±14	<±15	2	<±10.0	<±7.0	<±8.0	µA
DIBI	40	<±100	–	<±60	20	<±38	–	<±35	nA/˚C
PSRR	50	>45	>48	>45	50	>45	>48	>45	dB
CMRR	50	>45	>48	>45	50	>45	>48	>45	dB
ICC	**3.4**	**<3.8**	**<3.8**	**<4.2**	**1.0**	**<1.4**	**<1.3**	**<1.4**	**mA**
RIN	3000	>1000	>2000	>4000	7500	>2500	>5000	>10000	kΩ
CIN	1	<2	<2	<2	1	<2	<2	<2	pF
RO	0.2	<1.6	<0.5	<0.2	0.5	<3.0	<1.0	<0.5	Ω
VO	±3.3	>±2.8	>±2.7	>±3.0	±3.3	>±2.5	>±3.0	>±3.0	V
CMIR	±2.2	>±1.5	>±1.8	>±2.0	±2.2	>±1.5	>±1.8	>±2.0	V

Electrical Characteristics (Continued)

A_V = +6, V_{CC} = ±5V, R_f = 1000Ω, C_P = 100pF; unless specified

	SUPPLY CURRENT I_{CC} (TYP) = 3.4mA R_p =100kΩ, R_L = 500Ω				SUPPLY CURRENT I_{CC} (TYP) = 1mA R_p = 300kΩ, R_L =1000Ω				
IO	±25	>±10	>±18	>±18	±7	>±3.0	>±5	>±5	mA
IO	±25	>±9	>±18	>±18	±7	>±2.5	>±5	>±5	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Max/min ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Note 3: AJ-level: spec. is 100% tested at +25˚C = 3.4mA & parameter is 100% @25˚C in die form @ I_{CC}= 1mA, 3.4mA and 9mA.

Note 4: Not applicable due to output current limitations.

Note 5: See Text on the back page of data sheet.

Note 6: Differential gain and phase is characterized with a $1V_{PP}$ equivalent video signal, 0-100 IRE_{PP}, $40IRE_{pp}$, and 0IRE = 0V at the load resistor and 3.58 MHz.

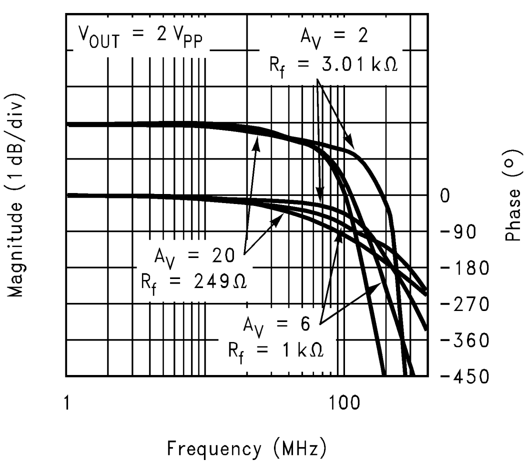
Note 7: xx/yy/zz MHz indicates that the CLC505 is specified at xxMHz for I_{CC} = 9mA, yyMHz for I_{cc} = 3.4mA, and zzMHz for I_{cc} = 1 mA.

Conditions are different for the three supply currents:

I_{CC}	R_L	R_{OUT}	A_V
9mA	75Ω	75Ω	+2
3.4mA	500Ω	0Ω	+6
1mA	1000Ω	0Ω	+6

Typical Performance Characteristics (T_A = 25˚C, A_V = +6, V_{CC} = ±5V, R_f = 1000Ω, V_H = +3V, C_p = 100pF)

I_{CC} 9mA, R_L 250Ω
Non-Inverting Gain Circuit



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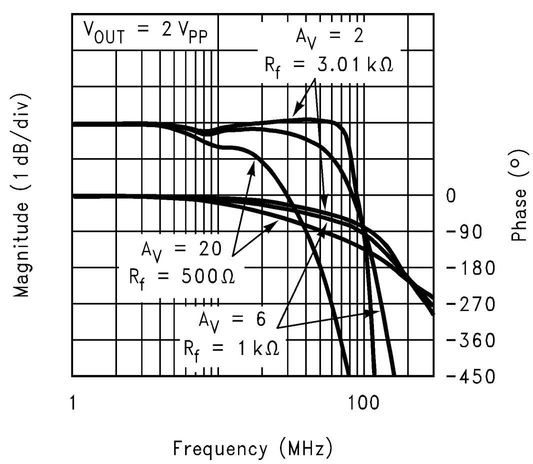
I_{CC} 3.4mA, R_L 500Ω
Non-Inverting Gain Circuit



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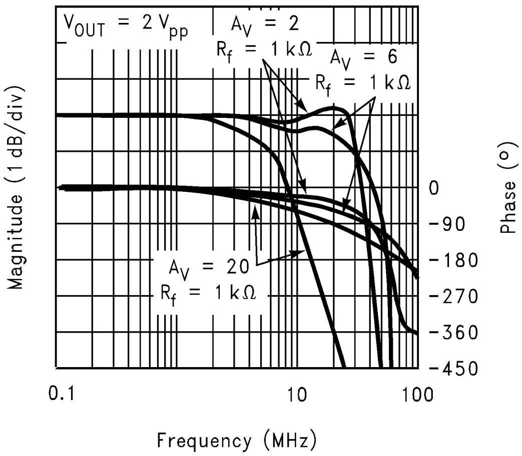
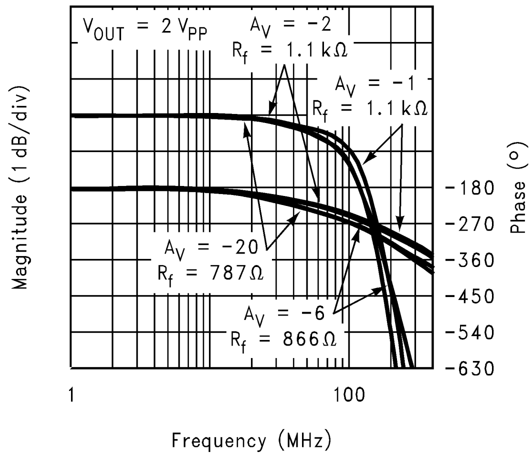
Typical Performance Characteristics (T_A = 25˚C, A_V = +6, V_{CC} = ±5V, R_f = 1000Ω, V_H = +3V, C_p = 100pF)) (Continued)

I_{CC} 1mA, R_L 1000Ω
Non-Inverting Gain Circuit



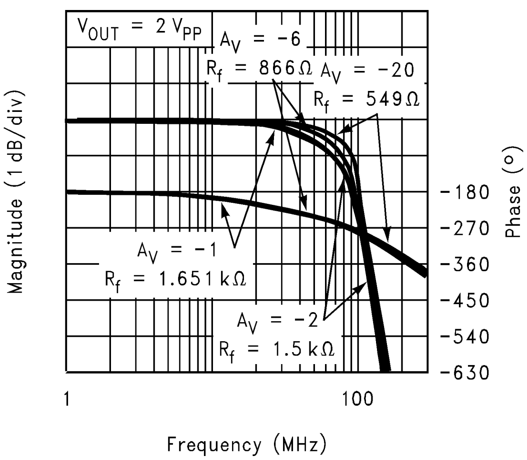
DS012755-3

Inverting Frequency Response



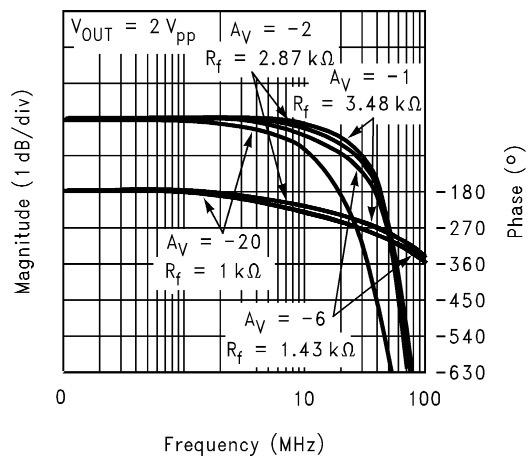
DS012755-4

Inverting Frequency Response



DS012755-5

Inverting Frequency Response



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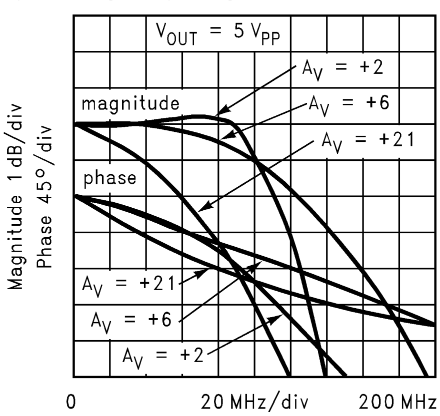
Large Signal Frequency Response



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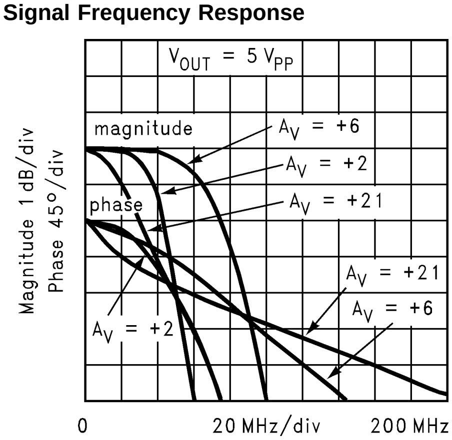
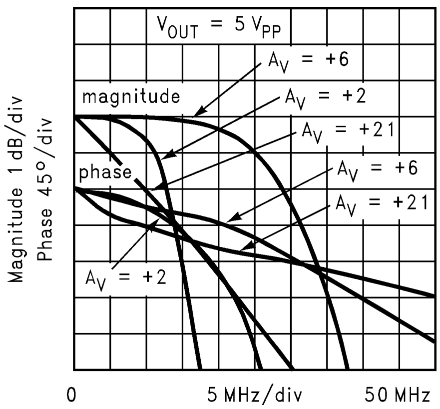
Large Signal Frequency Response



DS012755-8

Typical Performance Characteristics (T_A = 25˚C, A_V = +6, V_{CC} = ±5V, R_f = 1000Ω, V_H = +3V, C_p = 100pF)) (Continued)

Large Signal Frequency Response



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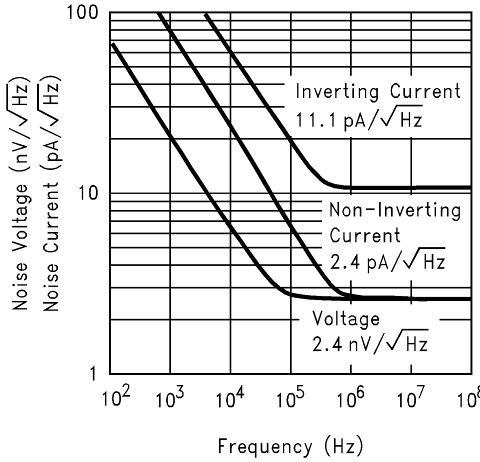
Equivalent Input Noise



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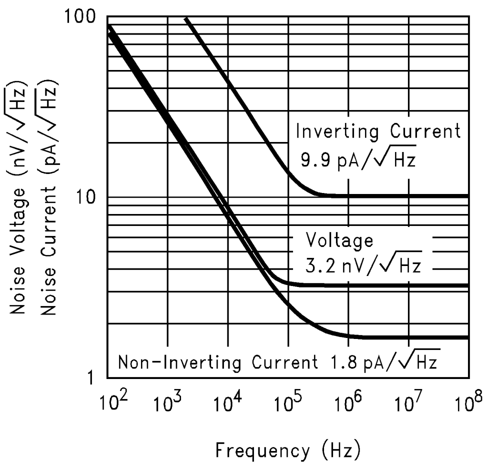
Equivalent Input Noise



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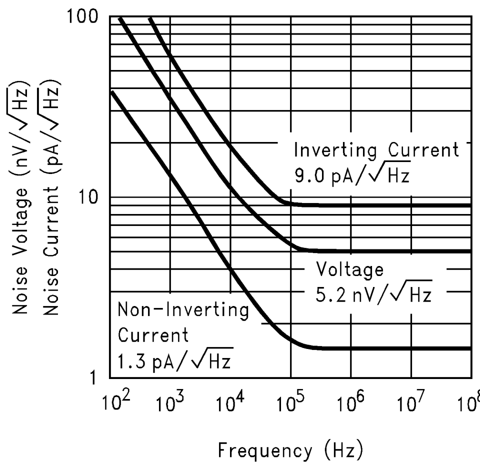
Equivalent Input Noise



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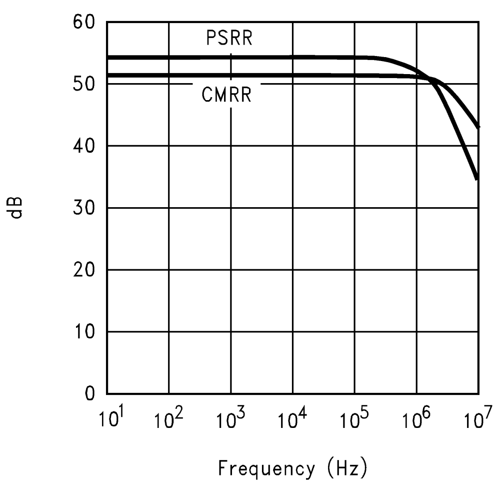
CMRR and PSRR



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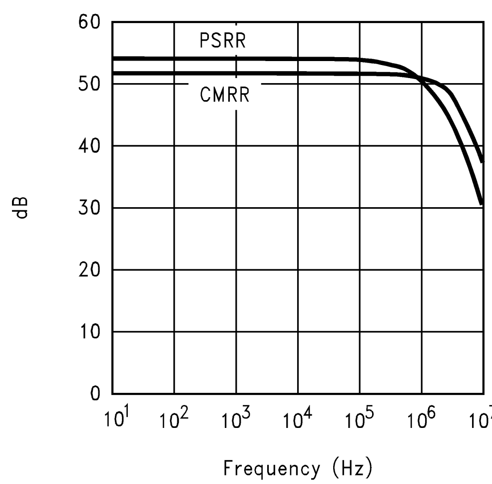
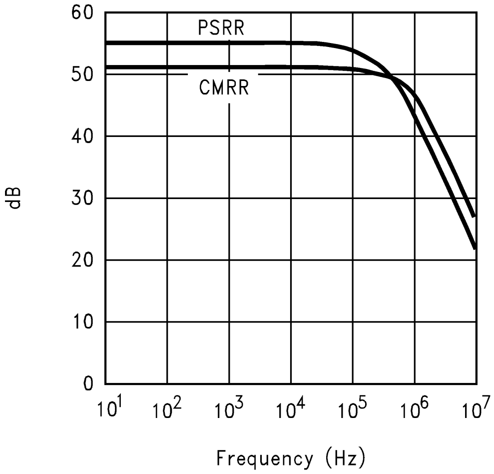
CMRR and PSRR



DS012755-14

Typical Performance Characteristics (T_A = 25˚C, A_V = +6, V_{CC} = ±5V, R_f = 1000Ω, V_H = +3V, C_p = 100pF)) (Continued)

CMRR and PSRR



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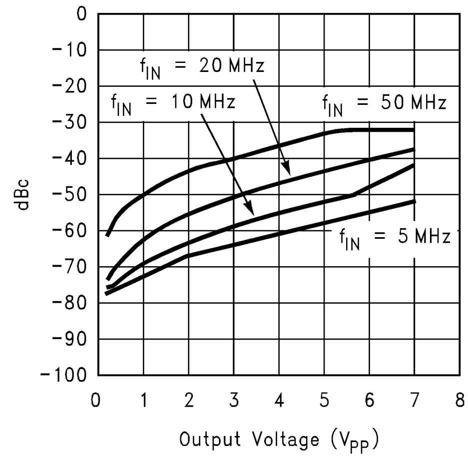
I_{CC} 9mA, R_L 250Ω
2nd Harmonic Distortion



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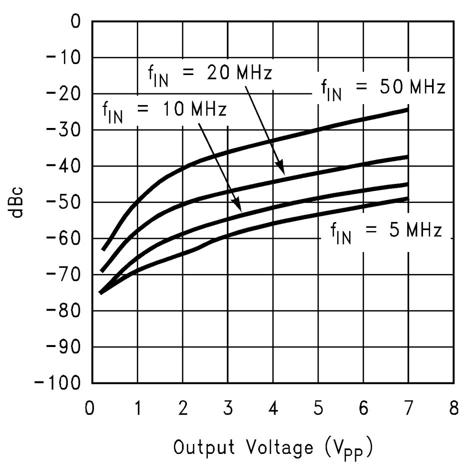
I_{CC} 34mA, R_L 500Ω
2nd Harmonic Distortion



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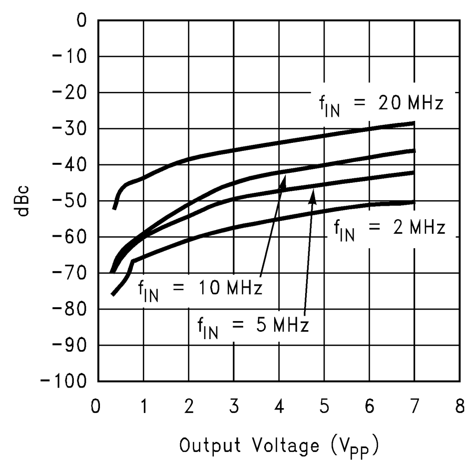
I_{CC} 1mA, R_L 1000Ω
2nd Harmonic Distortion



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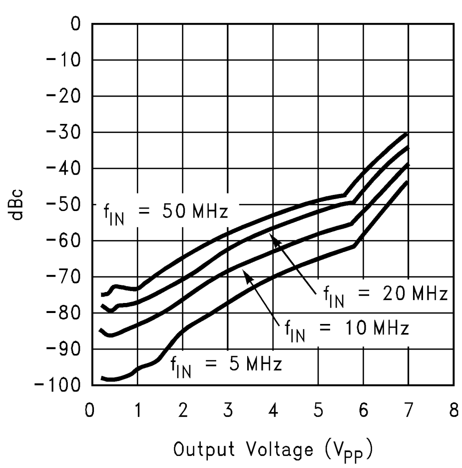
3rd Harmonic Distortion



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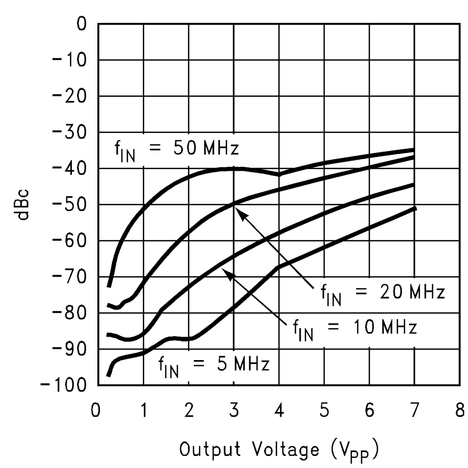
3rd Harmonic Distortion



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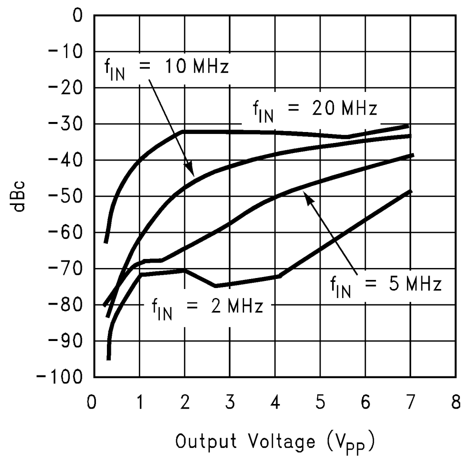
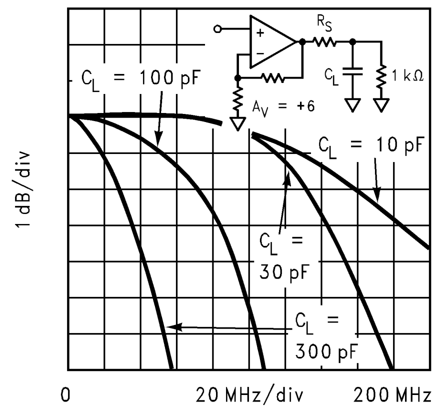
Typical Performance Characteristics (T_A = 25˚C, A_V = +6, V_{CC} = ±5V, R_f = 1000Ω, V_H = +3V, C_p = 100pF)) (Continued)

3rd Harmonic Distortion



DS012755-21

Bandwidth vs. Load Capacitance



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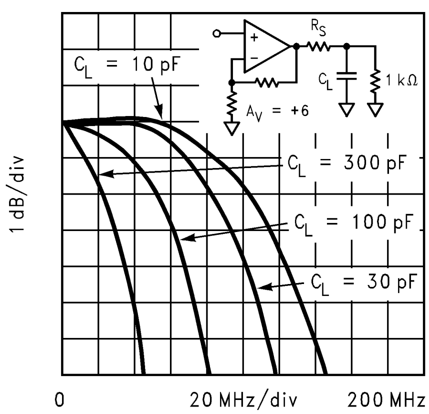
Bandwidth vs. Load Capacitance



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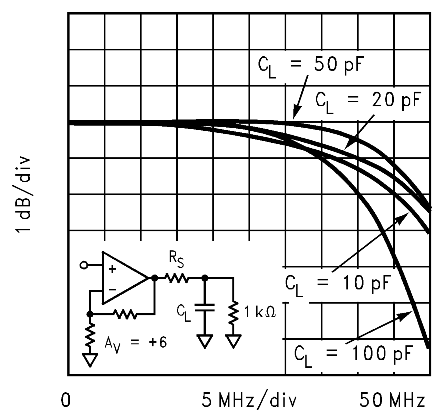
Bandwidth vs. Load Capacitance



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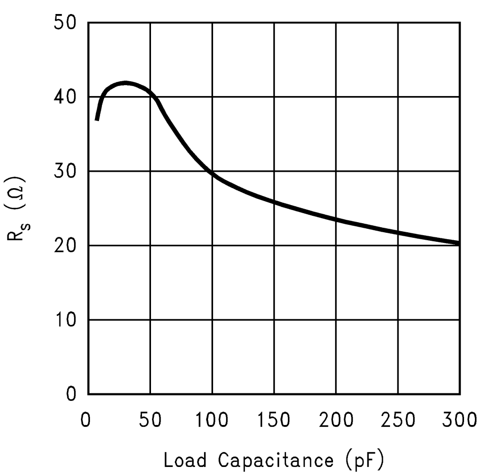
Recommended R_S vs. Load Capacitance



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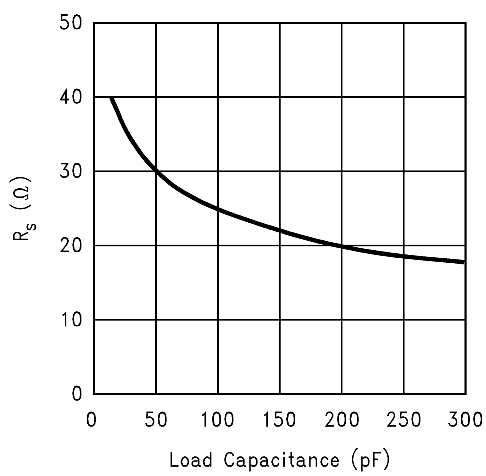
Recommended R_S vs. Load Capacitance



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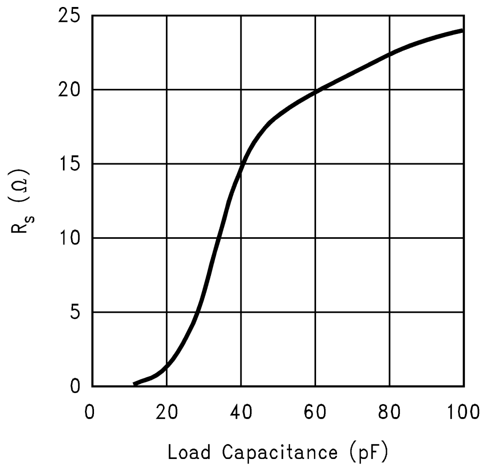
Typical Performance Characteristics (T_A = 25˚C, A_V = +6, V_{CC} = ±5V, R_f = 1000Ω, V_H = +3V, C_p = 100pF)) (Continued)

Recommended R_S vs. Load Capacitance



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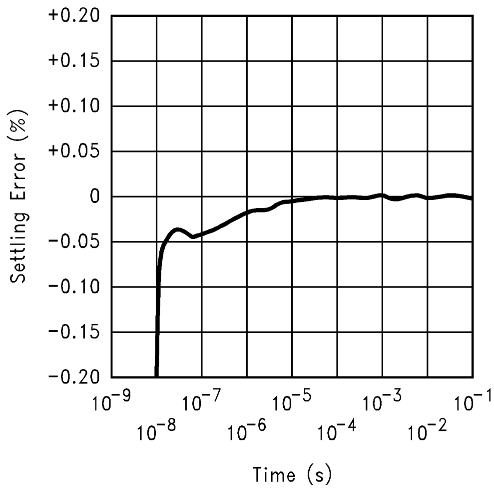
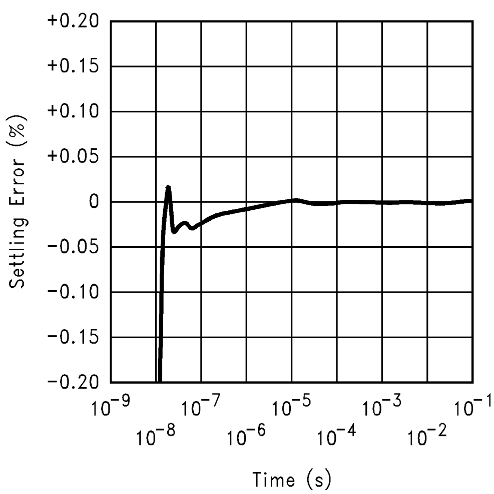
Settling Time



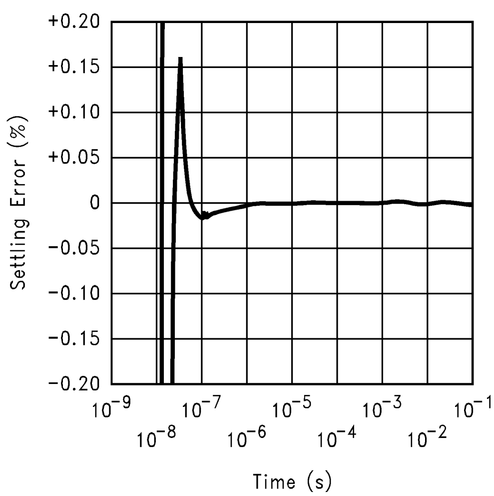
DS012755-28

Settling Time



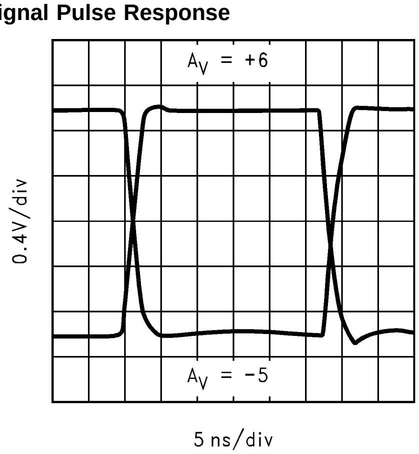
DS012755-29

Settling Time



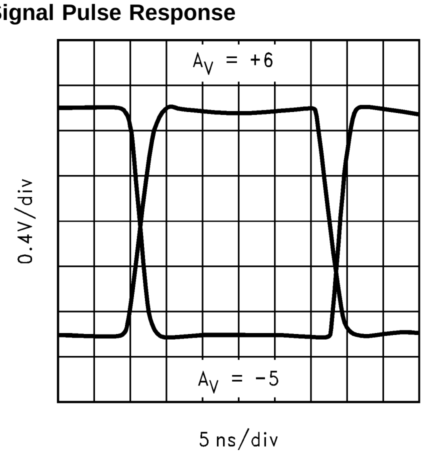
DS012755-30

I_{CC} 9mA, R_L 250Ω
Small-Signal Pulse Response



DS012755-34

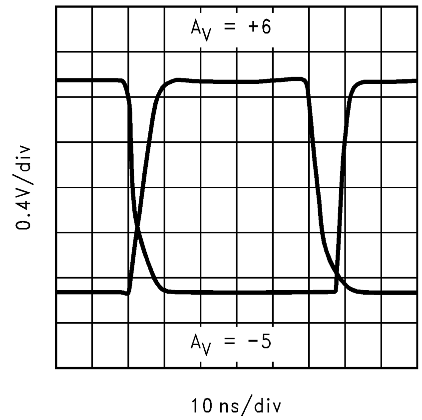
I_{CC} 34mA, R_L 500Ω
Small-Signal Pulse Response



DS012755-35

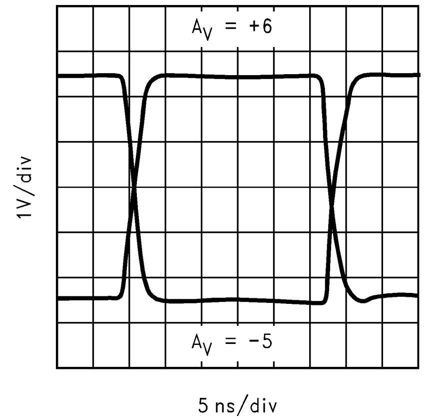
Typical Performance Characteristics (T_A = 25˚C, A_V = +6, V_{CC} = ±5V, R_f = 1000Ω, V_H = +3V, C_p = 100pF)) (Continued)

I_{CC} 1mA, R_L 1000Ω Small-Signal Pulse Response



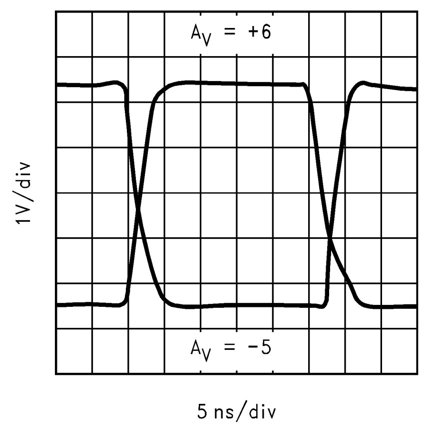
DS012755-36

Large-Signal Pulse Response



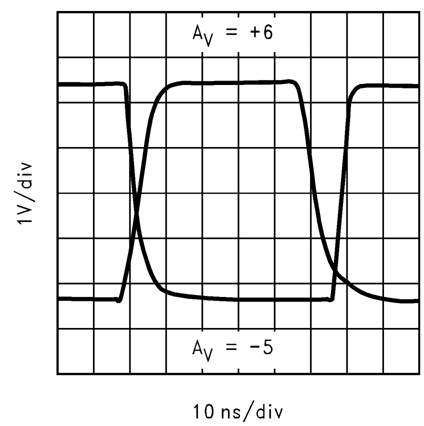
DS012755-37

Large-Signal Pulse Response



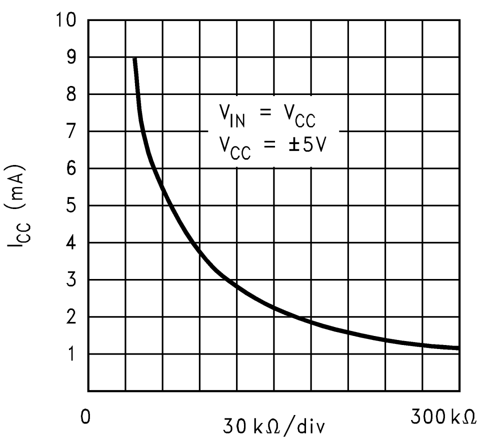
DS012755-38

Large-Signal Pulse Response



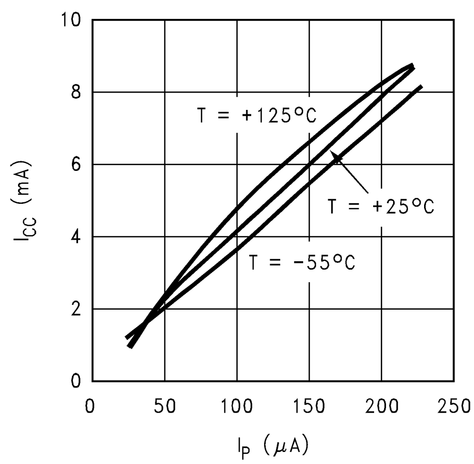
DS012755-39

I_{CC} vs. R_P



DS012755-40

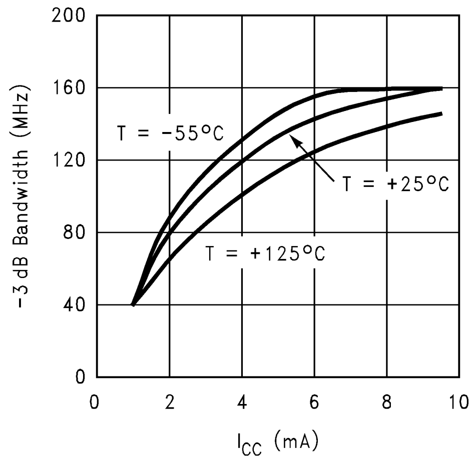
I_{CC} vs. I_P



DS012755-41

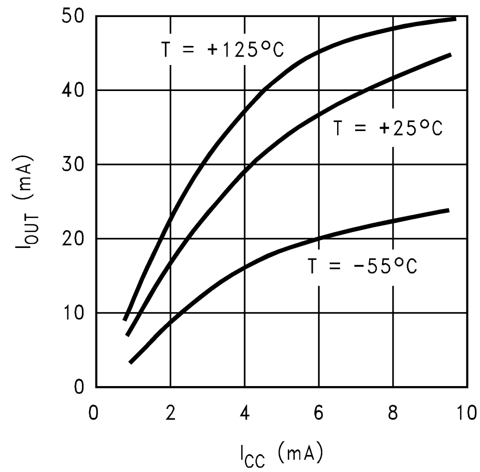
Typical Performance Characteristics (T_A = 25˚C, A_V = +6, V_{CC} = ±5V, R_f = 1000Ω, V_H = +3V, C_p = 100pF)) (Continued)

Bandwidth vs. I_{CC}



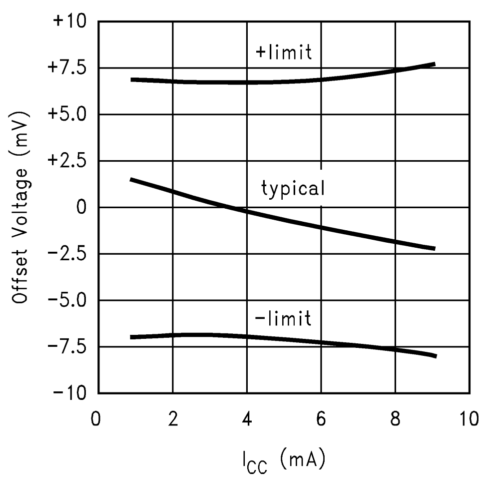
DS012755-42

Maximum Output Current vs. I_{CC}



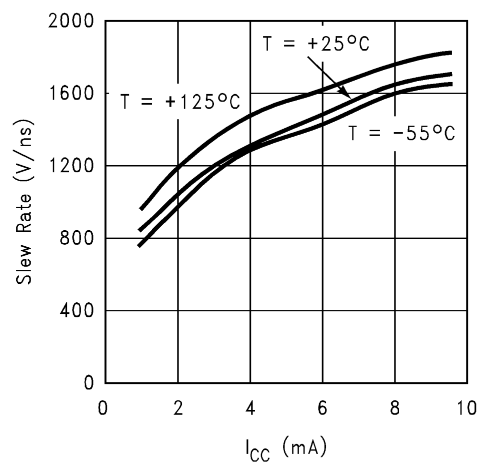
DS012755-43

Offset Voltage vs. I_{CC}



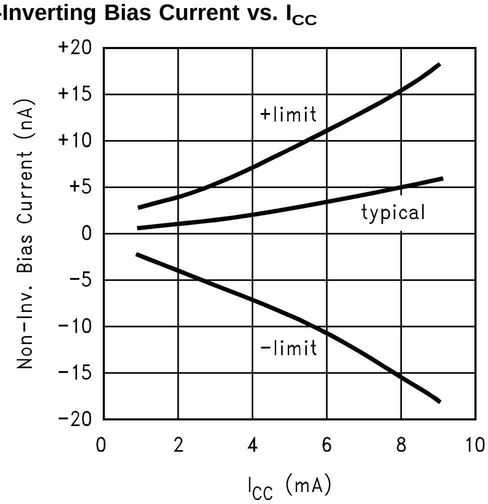
DS012755-44

Slew Rate vs. I_{CC}



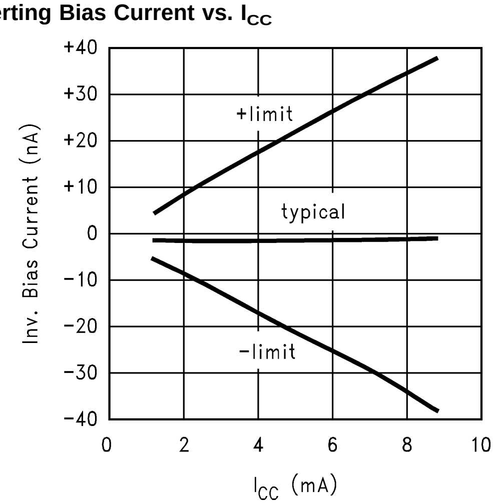
DS012755-45

Non-Inverting Bias Current vs. I_{CC}



DS012755-46

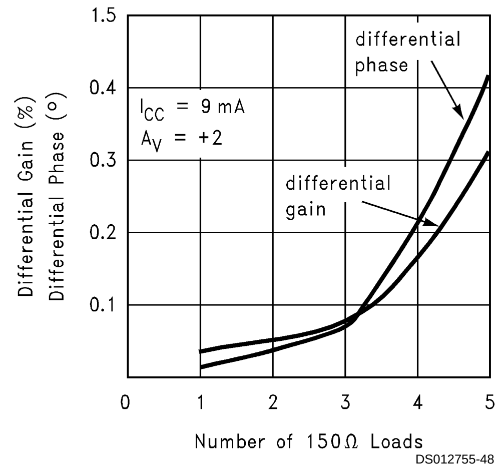
Inverting Bias Current vs. I_{CC}



DS012755-47

Typical Performance Characteristics (T_A = 25˚C, A_V = +6, V_{CC} = ±5V, R_f = 1000Ω, V_H = +3V, C_p = 100pF)) (Continued)

Differential Gain and Phase vs. Load



Application Information

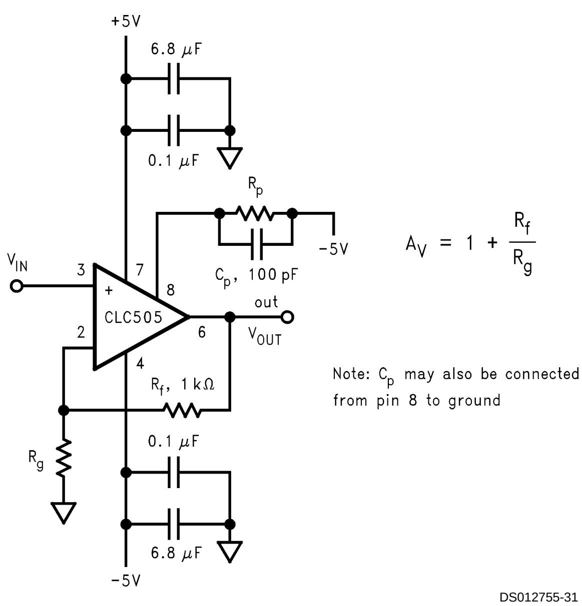


FIGURE 1. Recommended Non-Inverting Gain Circuit

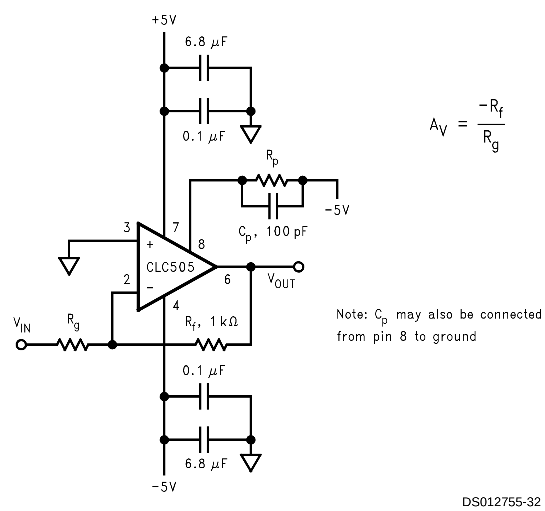


FIGURE 2. Recommended Inverting Gain Circuit

Description

The CLC505 is a programmable-supply current, current-feedback operational amplifier. Supply current and consequently dynamic performance can be easily adjusted by selecting the value of a single external resistor (R_p).

Application Information (Continued)

Selecting an Operating Point

The operating point is determined by the supply current, which in turn is determined by current (I_p) flowing out of pin 8. As the supply current is reduced the following effects will be observed:

Specification	Effect as I_{CC} Decreases
Bandwidth	Decreases
Rise TIme	increases
Output Drive	Decreases
Input Bias Current	Decreases
Input Impedance	Increases (see source impedance discussion)

Both the specification pages and the plot pages illustrate these effects to help make the supply current vs. performance tradeoff. Performance is specified and tested at I_{CC} =1mA, 3.4mA, and 9mA as indicated in the datasheet. (Note some test conditions and especially the load resistance are different for the three supply current settlings.) The performance plots show typical performance for all three supply currents levels.

When making the supply current vs. performance tradeoff, it is first a good idea to see if one of the standard operating points (I_{CC} = 9mA, 3.4mA, or 1mA) fits the application. If it does, performance guaranteed on the specification pages will apply directly to your application. In addition, the value of R_p may be obtained directly from the specification page.

The following discussion will assist in selecting I_{CC} for applications that cannot operate at one of the specified supply current settlings.

Use the typical performance plots for critical specifications to select the best I_{CC}. Now interpolate between the values of I_{CC} in the plots & specification tables to estimate the max/min values in the application.

From the selected value of I_{CC} the "programming current" (I_p) may be easily calculated:

$$I_P = I_{CC}/39$$

The plot of I_{CC} vs I_p in the plot pages shows this relationship graphically. Knowing I_p leads to a direct calculation of R_p.

$$R_p = [(+V_{PP} - 1.6) - V_n] / I_p$$

$$R_p = 8.4/I_p \text{ (for } +V_{CC} = +5V \text{ and } V_n = -5V)$$

V_n is the voltage externally applied to R_p. (Throughout the data sheet and in most applications, V_n and $-V_{CC}$ are −5V.) The term ($+V_{CC}$−1.6V) is the voltage at pin 8.

Now standard V_{CC}, V_{EE} and R_p does not have to be connected to $-V_{CC}$. In applications where non-standard supply voltages are used or when there is a need to power down the op amp via digital logic control. The value of R_p is adjusted accordingly.

First, an operating point needs to be determined from the plots & specifications as discussed above. From this, I_p is obtained. I_p, in concert with the available V_n determines R_p.

Example

An application requires that V_{CC} = ±3V and performance in the 1mA operating point range. The required I_p can therefore be determined as follows:

$$I_p = 26\mu A$$

R_p is connected from pin 8 to $-V_{CC}$ and V_{CC}=+/−3V. Now calculate R_p under new conditions:

$$R_p = [(+V_{CC} - 1.6V) - (-V_{CC})]/I_p$$

$$R_p = [(+3V - 1.6V) - (-3V)]/26\mu A$$

$$R_p = 169k\Omega$$

The CLC505 will have performance similar to R_p = 300kΩ shown on the datasheet, but with 40% less power dissipation due to the reduced supply voltages. (The op amp will also have a more restricted common-mode range and output swing.) This calculation is approximate and a prudent design would include substantial performance margin for max/min limits.

Dynamic Shutdown Capability

The CLC505 may be powered on and off very quickly by controlling the voltage applied to R_p. If R_p is connected between pin 8 and the output of a CMOS gate powered from ±5V supplies, the gate can be used to turn the amplifier on and off. This is shown in *Figure 3* below:

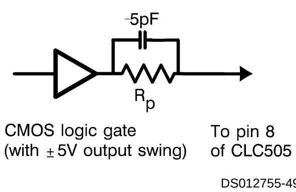


FIGURE 3. Dynamic Control of Power Consumption

When the gate output is switched from high to low, the CLC505 will turn on. In the off state, the supply current typically reduces to 0.2mA or less. The speed with which the CLC505 turns on or off is limited by the capacitance at pin 8. To improve switching time, a speed up capacitor from the gate output to pin 8 is recommended. The value of this capacitor will depend on the total capacitance connected to pin 8 and is best established experimentally. Turn-on and turn-off times of 100ns to 200ns are achievable with ordinary CMOS gates.

Example:

An open collector logic device is used to dynamically control the power dissipation of the circuit. Here, the desired connection for R_p is from pin 8 to the open collector logic device.

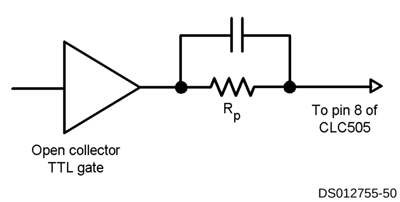


FIGURE 4. Controlling Power on State with TTL Logic

When the logic gate goes low, the CLC505 is turned on. Performance desired is that given for I_{CC} = 3.4mA under standard conditions. From the I_{CC} vs. I_p plot, I_p = 84µA. Then calculating R_p:

$$R_p = [(+V_{CC} - 1.6V) - (V_n)]/I_p$$

$$R_p = [(+5V - 1.6V) - (0)]84\mu A$$

$$R_p = 40k\Omega$$

Application Information (Continued)

Slew Rate

The rapid turn on and off ability of the CLC505 is not recommended for signal isolation applications (such as multiplexing). While the power dissipation of the amplifier drops in the off state, the amplifier may still have some gain at low frequencies. Causing feed through in multiplex application.

The performance desired is that given for I_{CC} = 3.4mA under standard conditions. From the I_{CC} vs. I_p plot, I_p=84µA. Is obtained now calculating R_p:

Slew rate limiting is a nonlinear response which occurs in amplifiers when the output voltage swing cannot change as rapidly as the applied input signal. The CLC505 has been designed to avoid slew rate limiting in most circuit configurations. The large signal ($5V_{PP}$) bandwidth of 80MHz at I_{CC} = 3.4mA, is only slightly less than the 100MHz small signal bandwidth. The result is a low distortion, linear system for both small and large signals over the required system frequency range.

The CLC505 reaches slew rate limits only for small non-inverting gains. In other words, slew rate limiting is constrained by common mode voltage swings at the input. The large signal frequency response plot at a gain of +2 was a break in the response, which indicates that a slew rate limit has been reached. Note also that the frequency response plots at a gain of +21 for large and small signal responses are nearly identical.

Differential Gain and Phase

Differential gain and phase are measurements useful primarily in composite video channels. They are measured by monitoring the gain and phase changes of a high frequency carrier (3.58MHz typically) as the output of the amplifier is swept over a range of DC voltages.

Specifications for the CLC505 include differential gain and phase. Test signals based on a $1V_{PP}$ video level. Test conditions used are the following:

DC sweep range: 0 to 100 IRE units (black to white)

Carrier: 3.58MHz at 40 IRE units peak to peak

The amplifier conditions are significantly different for the three values of supply current specified. At I_{CC} = 9mA, the amplifier is specified for a gain of +2 and 150Ω load (for a backmatched 75Ω system). IRE amplitudes at I_{CC} = 9mA, are referred to the 75Ω load resistor.

At I_{CC} = 1mA and I_{CC} = 3.4mA, the CLC505 is less capable of driving a 150Ω load due to output current limitations. For this reason lighter loads are used and the termination resistor is omitted. The gain and load resistance for I_{CC} = 3.4mA are A_V = +6 and R_L = 500Ω and for I_{CC} = 1mA; A_V = +6 and R_L = 1kΩ.

Source Impedance

For best results, source impedance in the non-inverting circuit configuration (see *Figure 1*) should be kept below 5kΩ. Above 5kΩ it is possible for oscillation to occur, depending on other circuit board parasitics. For high signal source impedances, a resistor with a value of less than 5kΩ may be used to terminate the non-inverting input to ground.

Feedback Resistor

In current-feedback op amps, the value of the feedback resistor plays a major role in determining amplifier dynamics. It is important to select the correct value. The CLC505 provides optimum performance with a 1kΩ feedback resistor. Selection of an incorrect value can lead to severe rolloff in frequency response, (if the resistor value is too large) or peaking or oscillation, (if the value is too low.)

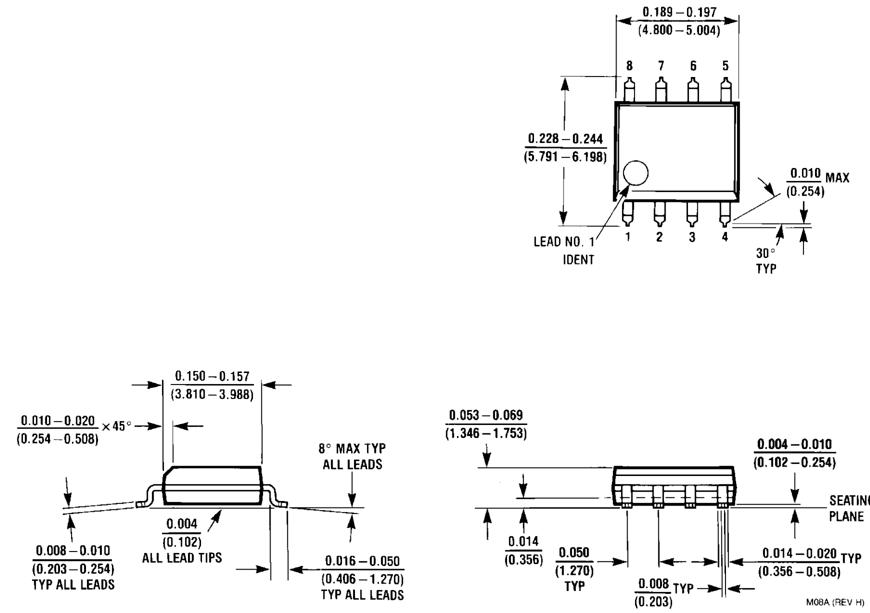
Printed Circuit Layout

As with any high frequency device, a good PCB layout will enhance performance. Ground plane construction and good power supply bypassing close to the package are critical to achieving full performance. In the non-inverting configuration, the amplifier is sensitive to stray capacitance to ground at the inverting input. Hence, the inverting node connections should be small with minimal coupling to the ground plane. Shunt capacitance across the feedback resistor should not be used to compensate for this effect.

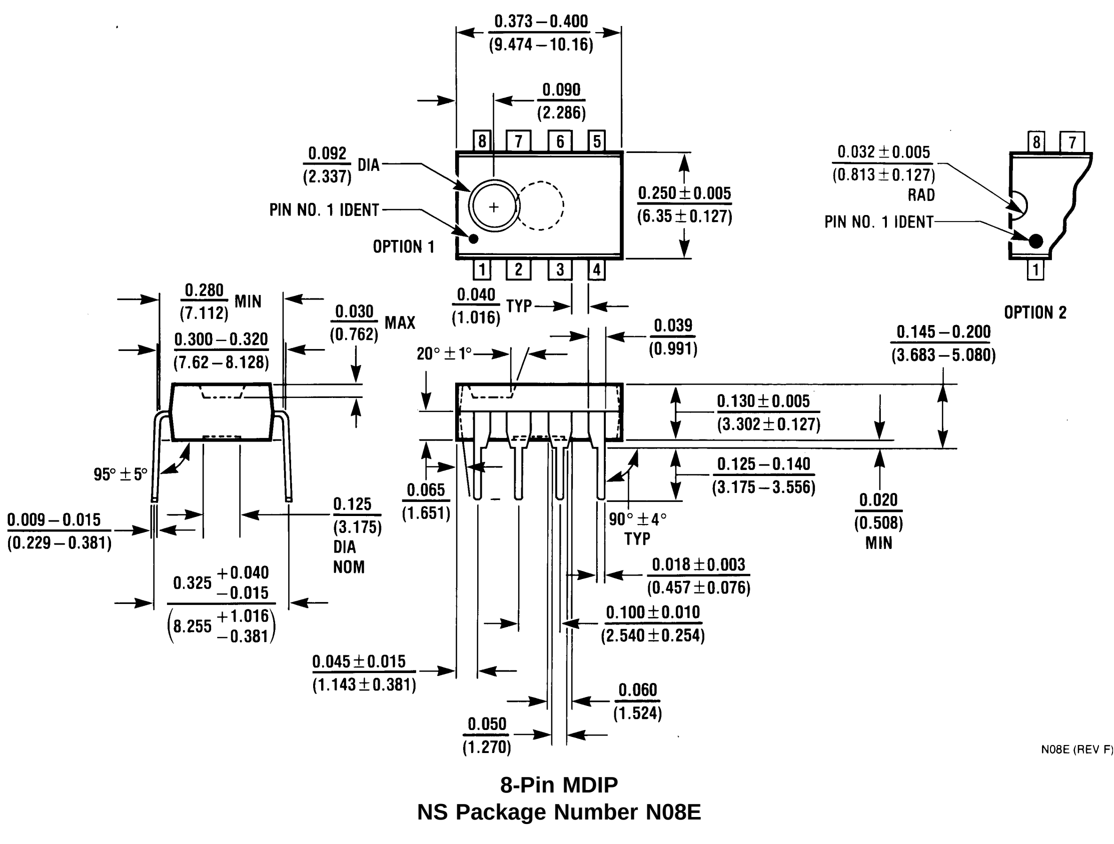
Precision buffed resistors (PRP8351 series from Precision Resistive Products) with low parasitic reactances were used to develop the data sheet specifications. Precision carbon composition resistors will also yield excellent results. Standard spirally-trimmed RN55D metal film resistors will work with a slight decrease in bandwidth due to their reactive nature at high frequencies.

Evaluation PC boards (part number 730013 for through-hole and 730027 for SOIC) for the CLC505 are available.

Physical Dimensions inches (millimeters) unless otherwise noted



8-Pin SOIC
NS Package Number M08A



8-Pin MDIP
NS Package Number N08E

Notes

National Semiconductor Corporation
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Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com
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National Semiconductor Japan Ltd.
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Fax: 81-3-5639-7507

Product Folder

CLC505 High Speed, Programmable Supply Current, Monolithic Op Amp

Contents

Parametric Table	
Channels (Channels)	1
Input Output Type	Not Rail to Rail
Bandwidth, typ (MHz)	220
Slew Rate, typ (Volts/usec)	1700
Supply Current per Channel, typ (mA)	9
Minimum Supply Voltage (Volt)	10
Maximum Supply Voltage (Volt)	14
Offset Voltage, Max (mV)	8
Input Bias Current, Temp Max (nA)	36000
Output Current, typ (mA)	45
Voltage Noise, typ (nV/Hz)	2.40
Shut down	No
Feedback Type	Current
BW at Av+1 (MHz)	220
BW at Av+2 (MHz)	210
BW at Av+5 (MHz)	140
BW at Av+10 (MHz)	135
BW at Av+20 (MHz)	122
HD 2nd, typ (dB)	-50
HD 3rd, typ (dB)	-65
DG, typ (dB)	.04
DP, typ (%)	.06
Settling Time	12nS to 0.1%
Special Features	Adj Is

General Description

The CLC505 is a monolithic, high speed op amp with a unique combination of high performance, low power consumption, and flexibility of application. The supply current is programmable over a 10 to 1 continuous range with a single resistor, R_p. This feature enables the amplifier to be used in a wide variety of high performance applications. Typical performance at any supply current is exceptional:

Parameter	**Supply Current (I_{CC})**			**Units**
	9mA	3.4mA	1mA	
-3dB Bandwidth	150	100	50	MHz
Settling Time	12	14	35	nsec
Slew Rate	1700	1200	800	V/μsec
Output Current	45	25	7	mA

The CLC505's combination of high performance, low power consumption, and large signal performance makes the CLC505 ideal for a wide variety of remote site equipment applications, such as battery powered test instrumentation and communications gear. Some other power applications are video switching matrices, ATE, and phased-array radar systems.

The CLC505 has been designed for ease of use and has been specified to ensure design confidence and final system predictability. The product performance is specified for 1mA, 3mA ad 9mA supply current. The CLC505 is available in 8-pin Dip SOIC packages offered for the industrial temperature range.

Enhanced Solutions (Military/Aerospace)

SMD Number: contact factory

Space level versions also available.

For more information, visit http://www.national.com/mil

Features

- 10mW power consumption with 50MHz BW
- Single resistor programming of supply current
- 3.4mA I_{CC} provides 100MHz bandwidth and 14ns settling (0.05%)
- Fast disable capability
- 0.04% differential gain at I_{CC} = 3.4mA
- 0.06% differential phase at I_{CC} = 3.4mA

Applications

- Low power battery applications
- Remote site instrumentation
- Mobile communications gear
- Video switching matrix
- Phased-array radar

Datasheet

Title	Size (in Kbytes)	Date	View Online	Download	Receive via Email
CLC505 High Speed, Programmable Supply Current, Monolithic Op Amp	480 Kbytes	12-Dec-00	View Online	Download	Receive via Email
CLC505 High Speed, Programmable Supply Current, Monolithic Op Amp (**JAPANESE**)	498 Kbytes		View Online	Download	Receive via Email
CLC505 Mil-Aero Datasheet MNCLC505A-X	102 Kbytes		View Online	Download	Receive via Email

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Package Availability, Models, Samples & Pricing

Part Number	Package		Status	Models		Samples & Electronic Orders	Budgetary Pricing		Std Pack Size	Package Marking
	Type	# pins		SPICE	IBIS		Quantity	$US each		
CLC505AJE	SOIC NARROW	8	Full production	clc505.cir	N/A	Samples Buy Now	1K+	$3.1900	tube of 95	[logo]¢2¢T CLC50 5AJE
CLC505AJE-TR13	SOIC NARROW	8	Full production	clc505.cir	N/A	Buy Now	1K+	$3.2300	reel of 2500	[logo]¢2¢T CLC50 5AJE
CLC505AJP	MDIP	8	Full production	clc505.cir	N/A	Samples Buy Now	1K+	$3.1900	tube of 40	[logo]¢U¢Z¢2¢T CLC505AJP
5962-9099301MPA	Cerdip	8	Full production	clc505.cir	N/A		50+	$37.5000	tube of 40	[logo]¢Z¢S¢4¢A$E CLC505AJ-QML 5962-9099301 MPA
CLC505AD-MLS	SB Cerdip	8	Full production	clc505.cir	N/A				tube of N/A	[logo]¢Z¢S¢4¢A CLC505AD -MLS $E

Design Tools

Title	Size (in Kbytes)	Date	View Online	Download	Receive via Email
Amplifiers Selection Guide software for Windows	9 Kbytes	19-Mar-2001		View	

CLC730013EB 8-pin Op Amp Evaluation Board	130 Kbytes	2-Jan-2001	View Online	Download	Receive via Email
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Application Notes

Title	Size (in Kbytes)	Date	View Online	Download	Receive via Email
AD-04: AD-04 Reducing the power Requirements of Comlinear CLC949 support Circuitry	40 Kbytes	28-Oct-96	View Online	Download	Receive via Email
OA-07: OA-07 Current- Feedback Op Amp Applications Circuit Guide	308 Kbytes	28-Oct-96	View Online	Download	Receive via Email
OA-11: OA-11 A Tutorial on Applying Op Amps to RF Applications	769 Kbytes	2-Apr-99	View Online	Download	Receive via Email
OA-12: OA-12 Noise Analysis for Comlinear's Op Amps	108 Kbytes	24-Feb-99	View Online	Download	Receive via Email
OA-13: OA-13 Current- Feedback Loop Gain Analysis	527 Kbytes	28-Oct-96	View Online	Download	Receive via Email
OA-14: OA-14 Improving Amplifier Noise Figure for High 3rd Intercept Amplifiers	92 Kbytes	15-Dec-00	View Online	Download	Receive via Email
OA-15: OA-15 Frequent Faux Pas in Applying Wideband Current Feedback Amplifiers	527 Kbytes	28-Jan-99	View Online	Download	Receive via Email
OA-18: OA-18 Simulation SPICE Models for Comlinear's Op Amps	337 Kbytes	23-May-00	View Online	Download	Receive via Email
OA-20: OA-20 Current Feedback Myths Debunked	139 Kbytes	10-Jul-97	View Online	Download	Receive via Email
OA-25: OA-25 Stability Analysis of Current Feedback Amplifier	262 Kbytes	10-Oct-96	View Online	Download	Receive via Email
OA-30: OA-30 Current vs. Voltage Feedback Amplifiers	56 Kbytes	5-Jun-98	View Online	Download	Receive via Email

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