

T-46-07-71



# 54FCT/74FCT574

## Octal D Flip-Flop with TRI-STATE® Outputs

### General Description

The 'FCT574 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ( $\overline{OE}$ ). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

FACT™ FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCT features GTOT™ output control and undershoot corrector in addition to a split ground bus for superior performance.

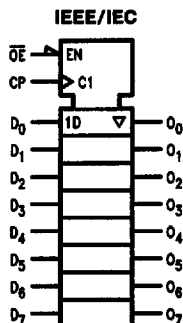
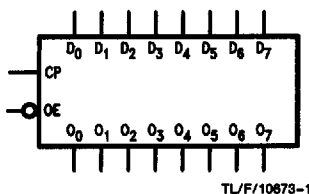
The 'FCT574 is functionally identical to the 'FCT374 except for the pinouts.

### Features

- $I_{CC}$  and  $I_{OZ}$  reduced to 40.0  $\mu A$  and  $\pm 2.5 \mu A$  respectively
- NSC 54FCT/74FCT574 is pin and functionally equivalent to IDT 54FCT/74FCT574
- Controlled output edge rates and undershoot for improved noise immunity. Internal split ground for improved noise immunity.
- Input clamp diodes to limit bus reflections.
- TTL/CMOS input and output level compatible.
- $I_{OL} = 48 \text{ mA (Com)}$  and 32 mA (Mil)
- CMOS power levels
- ESD immunity  $\geq 4 \text{ kV}$  typ
- Military Product compliant to MIL-STD 883

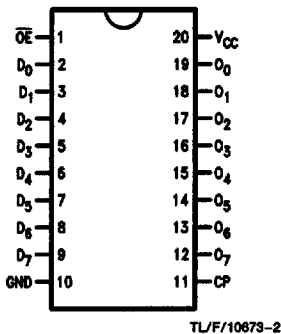
**Ordering Code:** See Section 8

### Logic Symbols

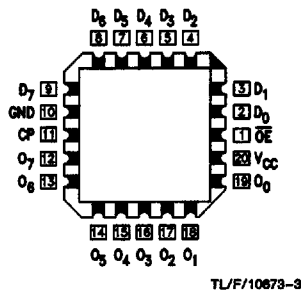


### Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC



Pin Names	Description
D <sub>0</sub> -D <sub>7</sub>	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
O <sub>0</sub> -O <sub>7</sub>	TRI-STATE Outputs

### Functional Description

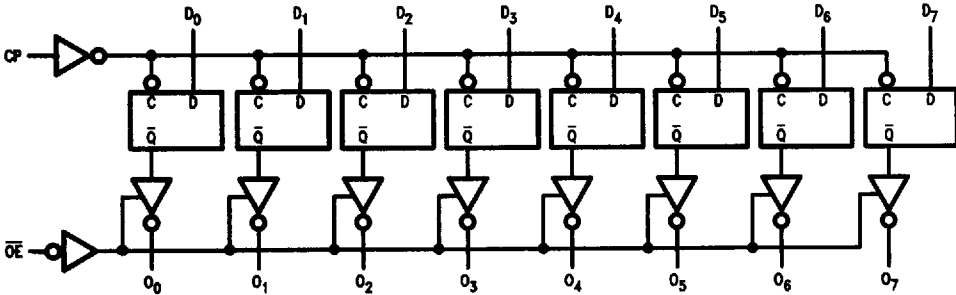
The 'FCT574 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ( $\overline{OE}$ ) LOW, the contents of the eight flip-flops are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	$O_N$	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	↗	L	L	Z	Load
H	↗	H	H	Z	Load
L	↗	L	L	L	Data Available
L	↗	H	H	H	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance  
 ↗ = LOW-to-HIGH Transition  
 NC = No Change

### Logic Diagram



TL/F/10673-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND ( $V_{TERM}$ )  
 54FCT -0.5V to +7.0V  
 74FCT -0.5V to +7.0V.

Temperature under Bias ( $T_{BIAS}$ )  
 74FCT -55°C to +125°C  
 54FCT -65°C to +135°C

Storage Temperature ( $T_{STG}$ )  
 74FCT -55°C to +125°C  
 54FCT -65°C to +150°C

DC Output Current ( $I_{OUT}$ ) 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum ratings conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

### Recommended Operating Conditions

Supply Voltage ( $V_{CC}$ )  
 54FCT 4.5V to 5.5V  
 74FCT 4.75V to 5.25V

Input Voltage 0V to  $V_{CC}$   
 Output Voltage 0V to  $V_{CC}$

Operating Temperature ( $T_A$ )  
 54FCT -55°C to +125°C  
 74FCT 0°C to +70°C

Junction Temperature ( $T_J$ )  
 CDIP 175°C  
 PDIP 140°C

Note: All commercial packaging is not recommended for applications requiring greater than 2000 temperature cycles from -40°C to +125°C.

### DC Characteristics for 'FCT Family Devices

Typical values are at  $V_{CC} = 5.0V$ , 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC} = 5.0V \pm 5\%$ ,  $T_A = 0^\circ C$  to +70°C; Mil:  $V_{CC} = 5.0V \pm 10\%$ ,  $T_A = -55^\circ C$  to +125°C,  $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	54FCT/74FCT			Units	Conditions	
		Min	Typ	Max			
$V_{IH}$	Minimum High Level Input Voltage	2.0			V		
$V_{IL}$	Maximum Low Level Input Voltage			0.8	V		
$I_{IH}$	Input High Current			5.0 5.0	$\mu A$	$V_{CC} = \text{Max}$	$V_I = V_{CC}$ $V_I = 2.7V$ (Note 2)
$I_{IL}$	Input Low Current			-5.0 -5.0	$\mu A$	$V_{CC} = \text{Max}$	$V_I = 0.5V$ (Note 2) $V_I = GND$
$I_{OZ}$	Maximum TRI-STATE Current			2.5 2.5 -2.5 -2.5	$\mu A$	$V_{CC} = \text{Max}$	$V_O = V_{CC}$ $V_O = 2.7V$ (Note 2) $V_O = 0.5V$ (Note 2) $V_O = GND$
$V_{IK}$	Clamp Diode Voltage			-0.7 -1.2	V	$V_{CC} = \text{Min}; I_N = -18 \text{ mA}$	
$I_{OS}$	Short Circuit Current	-60	-120		mA	$V_{CC} = \text{Max}$ (Note 1); $V_O = GND$	
$V_{OH}$	Minimum High Level Output Voltage	2.8	3.0		V	$V_{CC} = 3V; V_{IN} = 0.2V$ or $V_{HC}; I_{OH} = -32 \mu A$	
		$V_{HC}$	$V_{CC}$			$V_{CC} = \text{Min}$	$I_{OH} = -300 \mu A$
		2.4	4.3			$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -12 \text{ mA}$ (Mil) $I_{OH} = -15 \text{ mA}$ (Com)
$V_{OL}$	Maximum Low Level Output Voltage		GND	0.2	V	$V_{CC} = 3V; V_{IN} = 0.2V$ or $V_{HC}; I_{OL} = 300 \mu A$	
			GND	0.2		$V_{CC} = \text{Min}$	$I_{OL} = 300 \mu A$
			0.3	0.5		$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 32 \text{ mA}$ (Mil) $I_{OL} = 48 \text{ mA}$ (Com)
		0.3	0.5				

### DC Characteristics for 'FCT Family Devices

Typical values are at  $V_{CC} = 5.0V$ ,  $25^{\circ}C$  ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC} = 5.0V \pm 5\%$ ,  $T_A = 0^{\circ}C$  to  $+70^{\circ}C$ ; Mil:  $V_{CC} = 5.0V \pm 10\%$ ,  $T_A = -55^{\circ}C$  to  $+125^{\circ}C$ ,  $V_{HC} = V_{CC} - 0.2V$  (Continued)

Symbol	Parameter	54FCT/74FCT			Units	Conditions	
		Min	Typ	Max			
$I_{CC}$	Maximum Quiescent Supply Current		1.0	40.0	$\mu A$	$V_{CC} = \text{Max}$ $V_{IN} \geq V_{HC}$ , $V_{IN} \leq 0.2V$ $f_i = 0$	
$\Delta I_{CC}$	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	$V_{CC} = \text{Max}$ $V_{IN} = 3.4V$ (Note 3)	
$I_{CCD}$	Dynamic Power Supply Current (Note 4)		0.15	0.25	mA/MHz	$V_{CC} = \text{Max}$ Outputs Open $\overline{OE} = GND$ One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
$I_C$	Total Power Supply Current (Note 6)		1.5	4.0	mA	$V_{CC} = \text{Max}$ Outputs Open $\overline{OE} = GND$ $f_{CP} = 10 \text{ MHz}$ $f_i = 5.0 \text{ MHz}$ One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			1.8	6.0		$V_{IN} = 3.4V$ $V_{IN} = GND$	
			3.0	7.8		(Note 5) $V_{CC} = \text{Max}$ Outputs Open $\overline{OE} = GND$ $f_{CP} = 10 \text{ MHz}$ $f_i = 2.5 \text{ MHz}$ Eight Bits Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			5.0	16.8		$V_{IN} = 3.4V$ $V_{IN} = GND$	
$V_H$	Input Hysteresis on Clock Only		200		mV		

**Note 1:** Maximum test duration not to exceed one second, not more than one output shorted at one time.

**Note 2:** This parameter guaranteed but not tested.

**Note 3:** Per TTL driven input ( $V_{IN} = 3.4V$ ); all other inputs at  $V_{CC}$  or GND.

**Note 4:** This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

**Note 5:** Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.

**Note 6:**  $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$$

$I_{CC}$  = Quiescent Current

$\Delta I_{CC}$  = Power Supply Current for a TTL High Input ( $V_{IN} = 3.4V$ )

$D_H$  = Duty Cycle for TTL inputs High

$N_T$  = Number of Inputs at  $D_H$

$I_{CCD}$  = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

$f_{CP}$  = Clock Frequency for Register Devices (Zero for Non-Register Devices)

$f_i$  = Input Frequency

$N_i$  = Number of Inputs at  $f_i$

All currents are in milliamps and all frequencies are in megahertz.

**Note 7:** For 54FCT,  $I_{CCD} = 0.40 \text{ mA/MHz}$ .

Refer to applicable standard military drawing or NSC Table I for test conditions and  $I_C/I_{CC}$  limits.

574

**AC Electrical Characteristics:** See Section 2 for Waveforms

Symbol	Parameter	54FCT/74FCT	74FCT		54FCT		Units	Fig. No.
		$T_A = +25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$	$T_A, V_{CC} = \text{Min}$ $R_L = 500\Omega$ $C_L = 50\text{pF}$		$T_A, V_{CC} = \text{Com}$ $R_L = 500\Omega$ $C_L = 50\text{pF}$			
		Typ	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay CP to $O_n$	6.6	2.0	10.0	2.0	11.0	ns	2-8
$t_{PZH}$ $t_{PZL}$	Output Enable Time	9.0	1.5	12.5	1.5	14.0	ns	2-11
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time	6.0	1.5	8.0	1.5	8.0	ns	2-11
$t_{SU}$	Set-Up Time High or Low $D_n$ to CP	1.0	2.0		3.5		ns	2-10
$t_H$	Hold Time High or Low $D_n$ to CP	0.5	2.0		2.0		ns	2-10
$t_W$	CP Pulse Width High or Low	4.0	7.0		7.0		ns	2-9

Note: Minimum limits are guaranteed but not tested on propagation delays.

**Capacitance** ( $T_A = +25^\circ\text{C}, f = 1.0\text{ MHz}$ )

Symbol	Parameter (Note)	Typ	Max	Units	Conditions
$C_{IN}$	Input Capacitance	6	10	pF	$V_{IN} = 0\text{V}$
$C_{OUT}$	Output Capacitance	8	12	pF	$V_{OUT} = 0\text{V}$

Note: This parameter is measured during characterization but not tested.  
 $C_{OUT}$  for 74FCT only.