Very High Common-Mode Voltage Precision Difference Amplifier

Enhanced Product

AD8479-EP

FEATURES

- ±600 V dc common-mode voltage range
- Rail-to-rail output
- Fixed gain of 1
- Wide power supply operating voltage range of ±2.5 V to ±18 V
- 550 µA typical power supply current
- Excellent ac specifications
  - 80 dB minimum CMRR
  - 130 kHz small signal −3 dB bandwidth
- High accuracy dc performance
  - 10 ppm maximum gain nonlinearity
  - 15 µV/°C maximum offset voltage drift
  - 5 ppm/°C maximum gain drift

ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Military temperature range (−55°C to +125°C)
- Controlled manufacturing baseline
- One assembly/test site
- One fabrication site
- Product change notification
- Qualification data available on request

APPLICATIONS

- Avionics
- Unmanned systems
- High voltage current sensing
- Motor controls
- Isolation

GENERAL DESCRIPTION

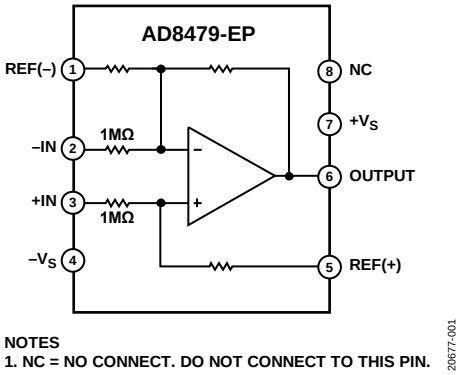
The AD8479-EP is a difference amplifier with a very high input common-mode voltage (V_{CM}) range. The AD8479-EP is a precision device that allows the user to accurately measure differential signals in the presence of high V_{CM} up to ±600 V dc.

The AD8479-EP can replace costly isolation amplifiers in applications that do not require galvanic isolation. The device operates over a ±600 V dc V_{CM} range and has inputs that are protected from common-mode or differential mode transients up to ±600 V.

The AD8479-EP has low offset voltage, low offset voltage drift, low gain drift, low common-mode rejection drift, and excellent common-mode rejection ratio (CMRR) over a wide frequency range.

The AD8479-EP is available in a space-saving 8-lead SOIC package and is operational over the −55°C to +125°C temperature range.

FUNCTIONAL BLOCK DIAGRAM



NOTES
1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.

Figure 1.

Additional application and technical information can be found in the AD8479 data sheet.

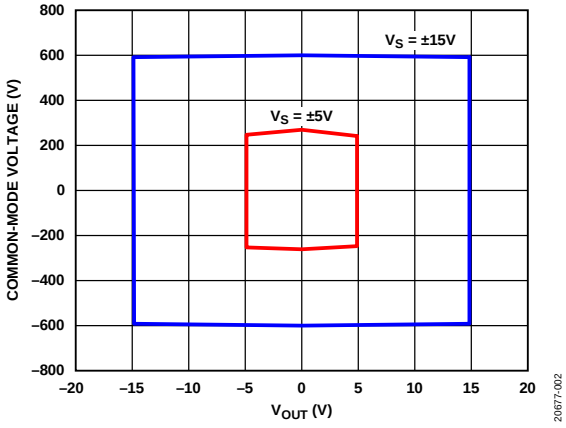


Figure 2. Input Common-Mode Voltage vs. Output Voltage (V_{OUT})

Rev. 0 Document Feedback

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REVISION HISTORY

6/2019—Revision 0: Initial Version

SPECIFICATIONS

Supply voltage (V_S) = ±15 V, REF(−) = REF(+) = 0 V, load resistor (R_L) = 2 kΩ, and T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
GAIN	V_{OUT} = ±10 V, R_L = 2 kΩ				
Nominal Gain			1		V/V
Gain Error			0.01	0.02	%
Gain Nonlinearity			4	10	ppm
Gain Drift	$T_A = T_{MIN}$ to T_{MAX}		3	5	ppm/°C
OFFSET VOLTAGE					
Offset Voltage	V_S = ±15 V		0.5	3	mV
	V_S = ±5 V		0.5	3	mV
Offset Voltage Drift	$T_A = T_{MIN}$ to T_{MAX}		3	15	µV/°C
Power Supply Rejection Ratio (PSRR)	V_S = ±2.5 V to ±15 V	84	100		dB
INPUT					
Common-Mode Rejection Ratio (CMRR)	V_{CM} = ±600 V dc				
	T_A = 25°C	80	90		dB
	$T_A = T_{MIN}$ to T_{MAX}	80			dB
	V_{CM} = 1200 V p-p, dc to 12 kHz	80			dB
Operating Voltage Range	Common-mode			±600	V
	Differential			±14.7	V
Input Operating Impedance	Common-mode		500		kΩ
	Differential		2		MΩ
OUTPUT					
Output Voltage Swing	R_L = 2 kΩ	$-V_S$ + 0.3		$+V_S$ − 0.3	V
Output Short-Circuit Current			±55		mA
Capacitive Load	Stable operation		500		pF
DYNAMIC RESPONSE					
Small Signal −3 dB Bandwidth			130		kHz
Slew Rate			9	9.3	V/µs
Full Power Bandwidth	V_{OUT} = 20 V p-p		100		kHz
Settling Time	0.01%, V_{OUT} = 10 V step		11		µs
	0.001%, V_{CM} = 10 V step		15.4		µs
OUTPUT VOLTAGE NOISE					
0.01 Hz to 10 Hz			30	35	µV p-p
Noise Spectral Density	Frequency ≥ 100 Hz		1.6		µV/√Hz
POWER SUPPLY					
Operating Voltage Range		±2.5		±18	V
Supply Current	V_{OUT} = 0 V		550	650	µA
	$T_A = T_{MIN}$ to T_{MAX}		850		µA
TEMPERATURE					
Operating Range (T_{MIN} to T_{MAX})		−55		+125	°C

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
V_S	±18 V
Input Voltage Range	
Continuous	±600 V
Common-Mode and Differential, 10 sec	±900 V
Output Short-Circuit Duration	Indefinite
REF(−) and REF(+)	$-V_S - 0.3$ V to $+V_S + 0.3$ V
Maximum Junction Temperature	150°C
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection, junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction to case thermal resistance.

Table 3. Thermal Resistance

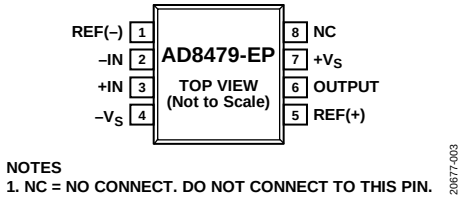
Package Type	θ_{JA}[1]	θ_{JC}[2]	Unit
R-8	122	87	°C/W

[1] Thermal impedance simulated values are based on JEDEC 2S2P thermal test board. See JEDEC JESD-51.
[2] Thermal impedance simulated values are based on JEDEC 1S0P thermal test board. See JEDEC JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	REF(–)	Negative Reference Voltage Input.
2	–IN	Inverting Input.
3	+IN	Noninverting Input.
4	$-V_S$	Negative Supply Voltage.
5	REF(+)	Positive Reference Voltage Input.
6	OUTPUT	Output.
7	$+V_S$	Positive Supply Voltage.
8	NC	No Connect. Do not connect to this pin.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = ±15 V, unless otherwise noted.

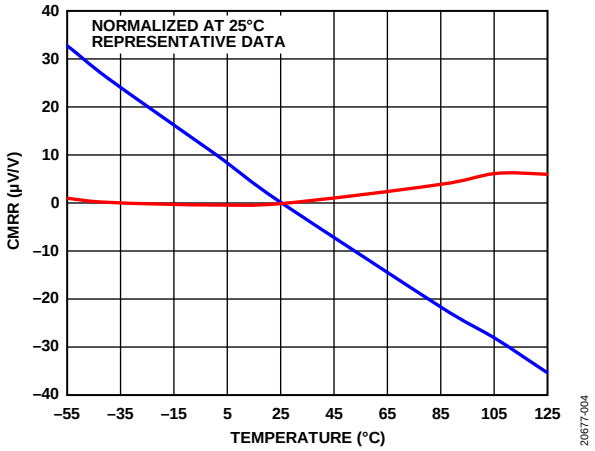


Figure 4. CMRR vs. Temperature, V_{CM} = ±20 V

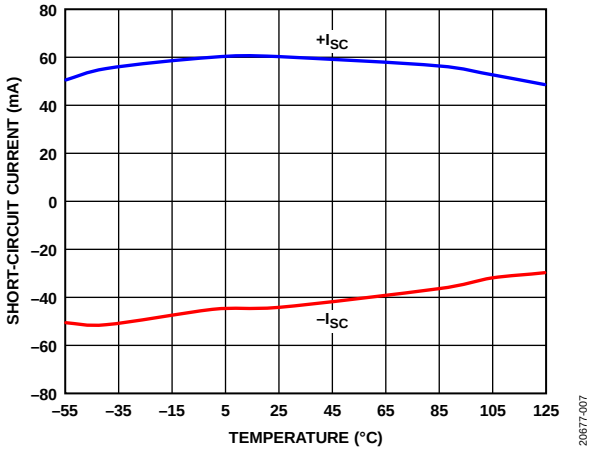


Figure 7. Short-Circuit Current (±I_{SC}) vs. Temperature

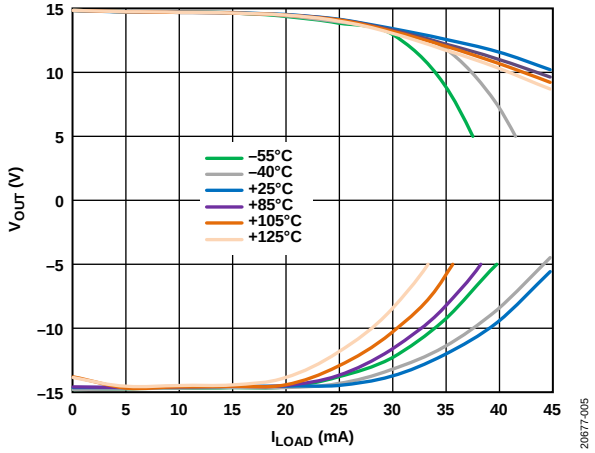


Figure 5. V_{OUT} vs. Output Current (I_{LOAD}) at Various Temperatures

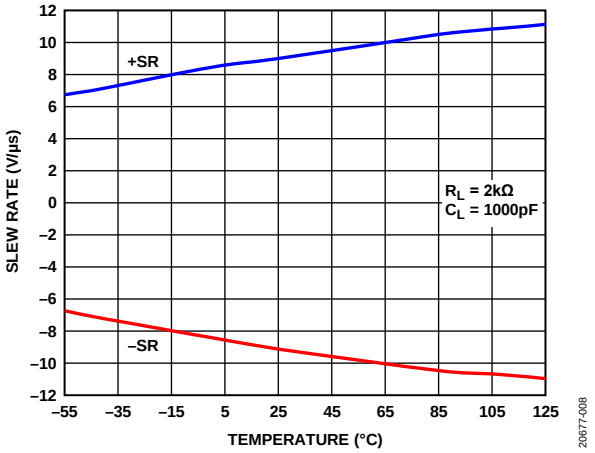


Figure 8. Slew Rate (±SR) vs. Temperature

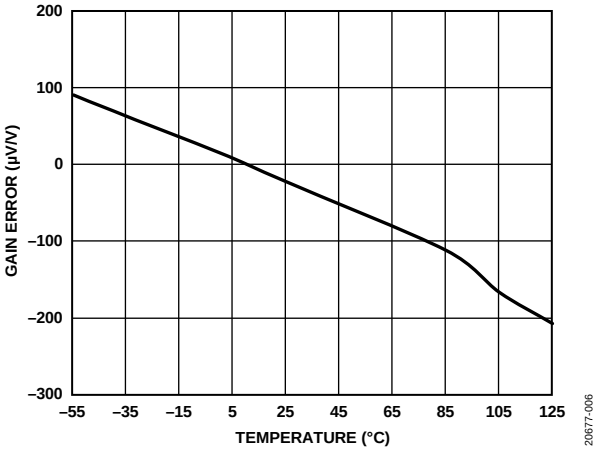


Figure 6. Gain Error vs. Temperature

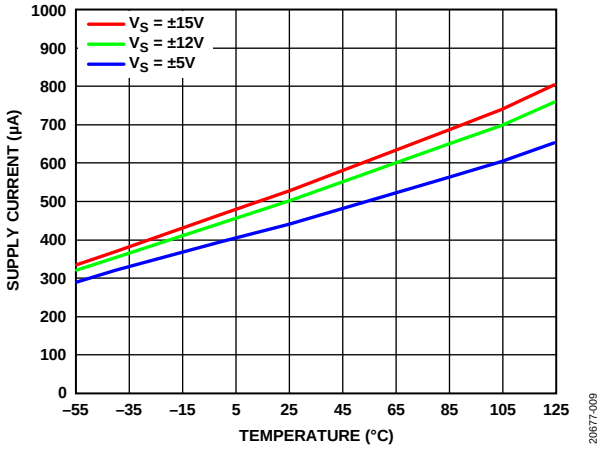
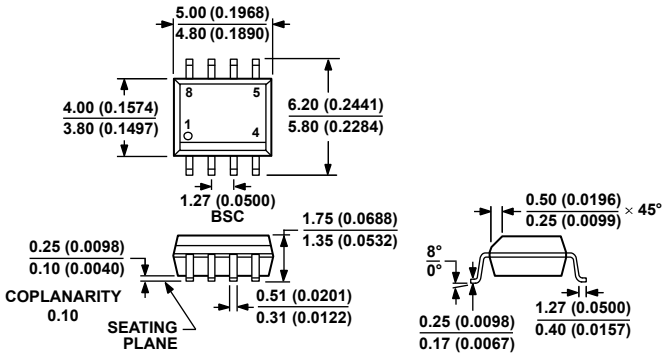


Figure 9. Supply Current vs. Temperature

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 10. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Ordering Quantity	Package Option
AD8479TRZ-EP	−55°C to +125°C	8-Lead SOIC_N		R-8
AD8479TRZ-EP-R7	−55°C to +125°C	8-Lead SOIC_N, 7-Inch Tape and Reel	1000 pieces	R-8

[1] Z = RoHS Compliant Part.