ANALOG DEVICES

Ultralow Power, Rail-to-Rail Output Operational Amplifiers

OP181/OP281/OP481

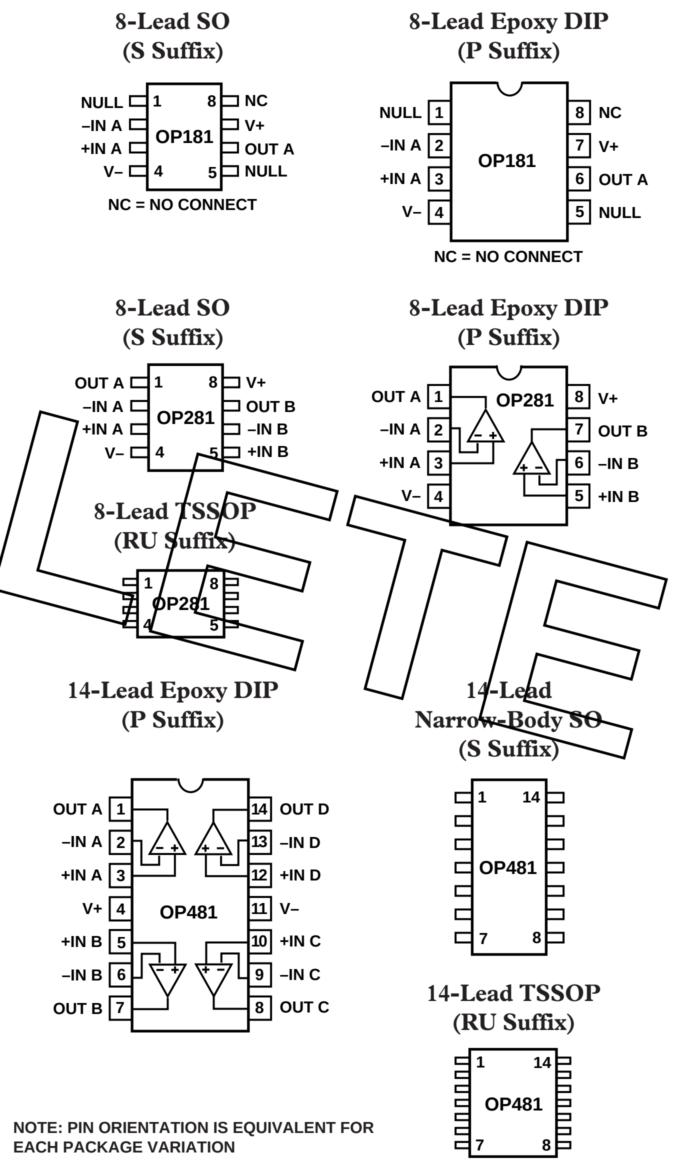
FEATURES

Low Supply Current: 4 μA/Amplifier max
Single-Supply Operation: 2.7 V to 12 V
Wide Input Voltage Range
Rail-to-Rail Output Swing
Low Offset Voltage: 1.5 mV
No Phase Reversal

APPLICATIONS

Comparator
Battery Powered Instrumentation
Safety Monitoring
Remote Sensors
Low Voltage Strain Gage Amplifiers

PIN CONFIGURATIONS



GENERAL DESCRIPTION

The OP181, OP281 and OP481 are single, dual and quad ultralow power, single-supply amplifiers featuring rail-to-rail outputs. All operate from supplies as low as 2.0 V and are specified at +3 V and +5 V single supply as well as ±5 V dual supplies.

Fabricated on Analog Devices' CBCMOS process, the OP181 family features a precision bipolar input and an output that swings to within millivolts of the supplies and continues to sink or source current all the way to the supplies.

Applications for these amplifiers include safety monitoring, portable equipment, battery and power supply control, and signal conditioning and interface for transducers in very low power systems.

The output's ability to swing rail-to-rail and not increase supply current, when the output is driven to a supply voltage, enables the OP181 family to be used as comparators in very low power systems. This is enhanced by their fast saturation recovery time. Propagation delays are 250 μs.

The OP181/OP281/OP481 are specified over the extended industrial (–40°C to +85°C) temperature range. The OP181, single, and OP281, dual, amplifiers are available in 8-pin plastic DIPs and SO surface mount packages. The OP281 is also available in 8-lead TSSOP. The OP481 quad is available in 14-pin DIPs, narrow 14-pin SO and TSSOP packages.

REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 World Wide Web Site: http://www.analog.com
Fax: 617/326-8703

OP181/OP281/OP481–SPECIFICATIONS

ELECTRICAL SPECIFICATIONS (@ V_S = +3.0 V, V_{CM} = 1.5 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	Note 1			1.5	mV
		$-40°C \le T_A \le +85°C$			2.5	mV
Input Bias Current	I_B	$-40°C \le T_A \le +85°C$		3	10	nA
Input Offset Current	I_{OS}	$-40°C \le T_A \le +85°C$		0.1	7	nA
Input Voltage Range			0		2	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 2.0 V,				
		$-40°C \le T_A \le +85°C$	65	95		dB
Large Signal Voltage Gain	A_{VO}	R_L = 1 MΩ, V_O = 0.3 V to 2.7 V	5	13		V/mV
		$-40°C \le T_A \le +85°C$	2			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			10		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			20		pA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$			2		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100 kΩ to GND,				
		$-40°C \le T_A \le +85°C$	2.925	2.96		V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to V+,				
		$-40°C \le T_A \le +85°C$		25	75	mV
Short Circuit Limit	I_{SC}			±1.1		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 12 V				
		$-40°C \le T_A \le +85°C$	76	95		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		3	4	µA
		$-40°C \le T_A \le +85°C$			5	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 100 kΩ, C_L = 50 pF		25		V/ms
Turn On Time		A_V = 1, V_O = 1		40		µs
Turn On Time		A_V = 20, V_O = 1		50		µs
Saturation Recovery Time				65		µs
Gain Bandwidth Product	GBP			95		kHz
Phase Margin	ϕo			70		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		10		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		75		$nV/\sqrt{Hz}$
Current Noise Density	i_n			<1		$pA/\sqrt{Hz}$

NOTES
[1] V_{OS} is tested under no load condition.

Specifications subject to change without notice.

ELECTRICAL SPECIFICATIONS (@ V_S = +5.0 V, V_{CM} = 2.5 V, T_A = +25°C unless otherwise noted[1])

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	Note 1		0.1	1.5	mV
		–40°C ≤ T_A ≤ +85°C			2.5	mV
Input Bias Current	I_B	–40°C ≤ T_A ≤ +85°C		3	10	nA
Input Offset Current	I_{OS}	–40°C ≤ T_A ≤ +85°C		0.1	7	nA
Input Voltage Range			0		4	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 4.0 V,				
		–40°C ≤ T_A ≤ +85°C	65	90		dB
Large Signal Voltage Gain	A_{VO}	R_L = 1 MΩ , V_O = 0.5 V to 4.5 V	5	15		V/mV
		–40°C ≤ T_A ≤ +85°C	2			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	–40°C to +85°C		10		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			20		pA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$			2		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100 kΩ to GND,				
		–40°C ≤ T_A ≤ +85°C	4.925	4.96		V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to V+				
		–40°C ≤ T_A ≤ +85°C		25	75	mV
Short Circuit Limit	I_{SC}			±3.5		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 12 V,				
		–40°C ≤ T_A ≤ +85°C	76	95		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		3.2	4	µA
		–40°C ≤ T_A ≤ +85°C			5	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 100 kΩ, C_L = 50 pF		27		V/ms
Saturation Recovery Time				120		µs
Gain Bandwidth Product	GBP			100		kHz
Phase Margin	φo			74		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		10		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		75		nV/√Hz
Current Noise Density	i_n			<1		pA/√Hz

NOTES

[1]V_{OS} is tested under a no load condition.

Specifications subject to change without notice.

OP181/OP281/OP481–SPECIFICATIONS

ELECTRICAL SPECIFICATIONS (@ V_S = ±5 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	Note 1		0.1	1.5	mV
		$-40°C \le T_A \le +85°C$			2.5	mV
Input Bias Current	I_B	$-40°C \le T_A \le +85°C$		3	10	nA
Input Offset Current	I_{OS}	$-40°C \le T_A \le +85°C$		0.1	7	nA
Input Voltage Range			–5		+4	V
Common-Mode Rejection	CMRR	V_{CM} = –5.0 V to +4.0 V,				
		$-40°C \le T_A \le +85°C$	65	95		dB
Large Signal Voltage Gain	A_{VO}	R_L = 1 MΩ, V_O = ±4.0 V,	5	13		V/mV
		$-40°C \le T_A \le +85°C$	2			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	–40°C to +85°C		10		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			20		pA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$			2		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 100 kΩ to GND,				
		$-40°C \le T_A \le +85°C$	±4.925	±4.98		V
Short Circuit Limit	I_{SC}			12		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±1.35 V to ±6 V,				
		$-40°C \le T_A \le +85°C$	76	95		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		3.3	5	µA
		$-40°C \le T_A \le +85°C$			6	µA
DYNAMIC PERFORMANCE						
Slew Rate	±SR	R_L = 100 kΩ, C_L = 50 pF		28		V/ms
Gain Bandwidth Product	GBP			105		kHz
Phase Margin	φo			75		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		10		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		85		$nV/\sqrt{Hz}$
Voltage Noise Density	e_n	f = 10 kHz		75		$nV/\sqrt{Hz}$
Current Noise Density	i_n			<1		$pA/\sqrt{Hz}$

NOTES

[1]V_{OS} is tested under no load condition.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . +16 V
Input Voltage . . . . Gnd to V_S + 10 V
Differential Input Voltage . . . . ±3.5 V
Output Short-Circuit Duration to Gnd . . . . Indefinite
Storage Temperature Range
  P, S, RU Package . . . . –65°C to +150°C
Operating Temperature Range
  OP181/OP281/OP481G . . . . –40°C to +85°C
Junction Temperature Range
  P, S, RU Package . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . +300°C

Package Type	θ_{JA}*	θ_{JC}	Units
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W
8-Pin TSSOP (RU)	240	43	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W
14-Pin SOIC (S)	120	36	°C/W
14-Pin TSSOP (RU)	240	43	°C/W

*θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP packages; θ_{JA} is specified for device soldered in circuit board for TSSOP and SOIC packages.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
OP181GP	–40°C to +85°C	8-Pin Plastic DIP	N-8
OP181GS	–40°C to +85°C	8-Pin SOIC	SO-8
OP281GP	–40°C to +85°C	8-Pin Plastic DIP	N-8
OP281GS	–40°C to +85°C	8-Pin SOIC	SO-8
OP281GRU	–40°C to +85°C	8-Pin TSSOP	RU-8
OP481GP	–40°C to +85°C	14-Pin Plastic DIP	N-14
OP481GS	–40°C to +85°C	14-Pin SOIC	SO-14
OP481GRU	–40°C to +85°C	14-Pin TSSOP	RU-14

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP181/OP281/OP481 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

OP181/OP281/OP481–Typical Characteristics

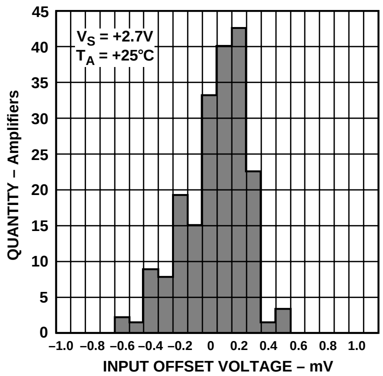


Figure 1. Input Offset Voltage Distribution

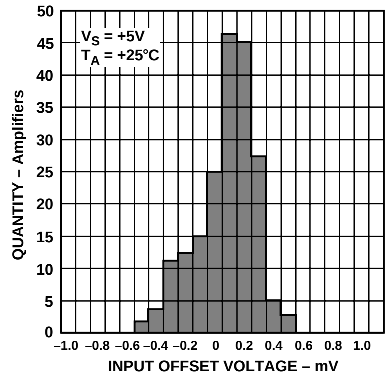


Figure 2. Input Offset Voltage Distribution

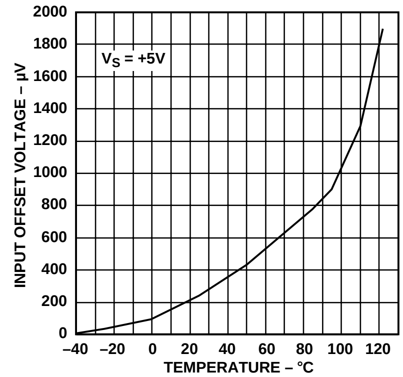


Figure 3. Input Offset Voltage vs. Temperature

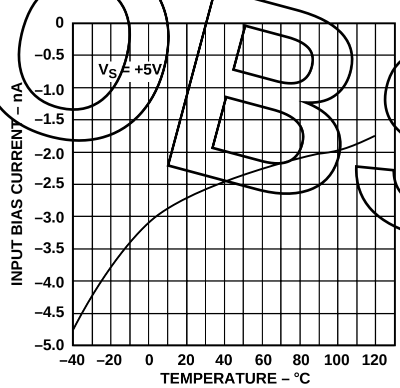


Figure 4. Input Bias Current vs. Temperature

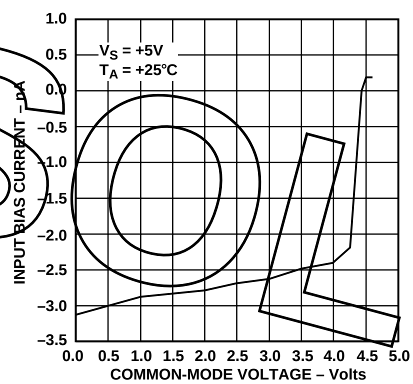


Figure 5. Input Bias Current vs. Common-Mode Voltage

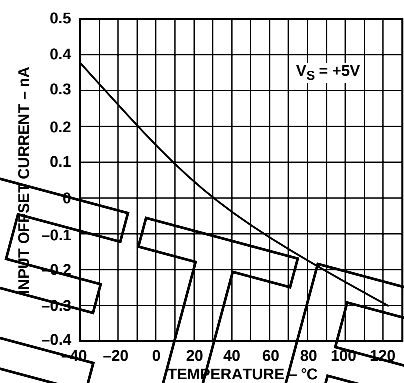


Figure 6. Input Offset Current vs. Temperature

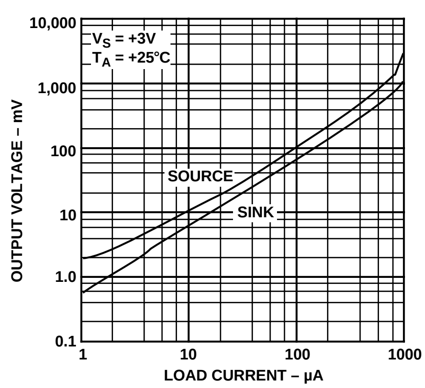


Figure 7. Output Voltage to Supply Rail vs. Load Current

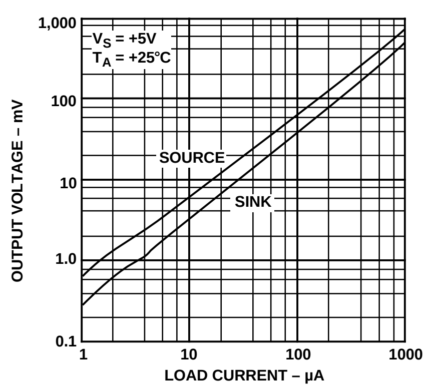


Figure 8. Output Voltage to Supply Rail vs. Load Current

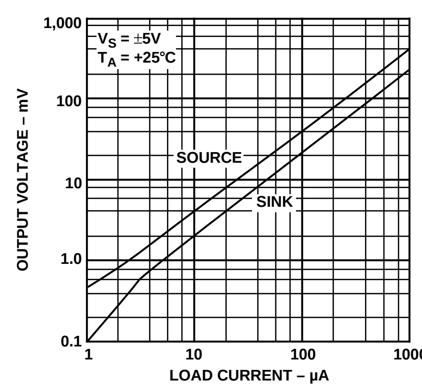


Figure 9. Output Voltage to Supply Rail vs. Load Current

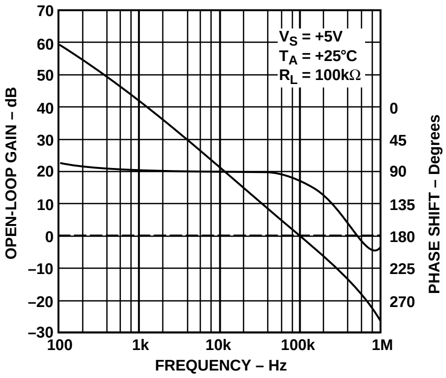


Figure 10. Open-Loop Gain and Phase vs. Frequency

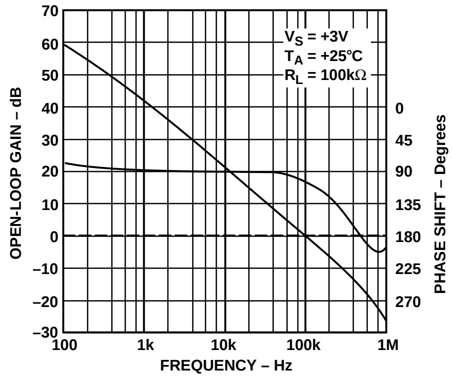


Figure 11. Open-Loop Gain and Phase vs. Frequency

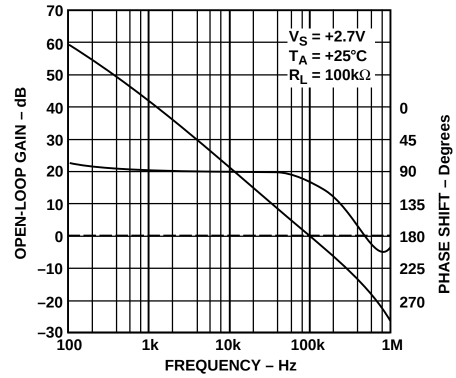


Figure 12. Open-Loop Gain and Phase vs. Frequency

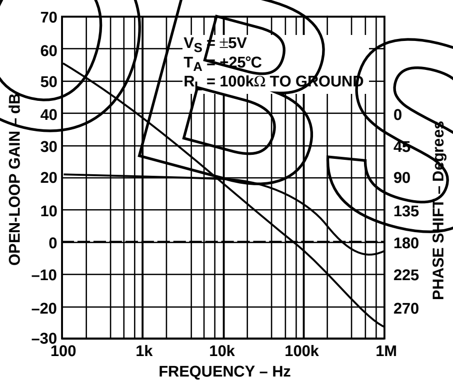


Figure 13. Open-Loop Gain and Phase vs. Frequency

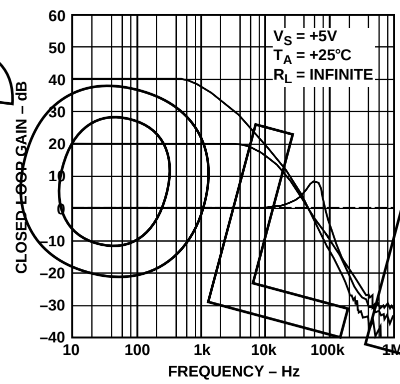


Figure 14. Closed-Loop Gain vs. Frequency

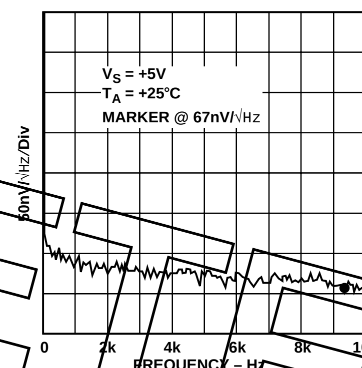


Figure 15. Voltage Noise Density vs. Frequency

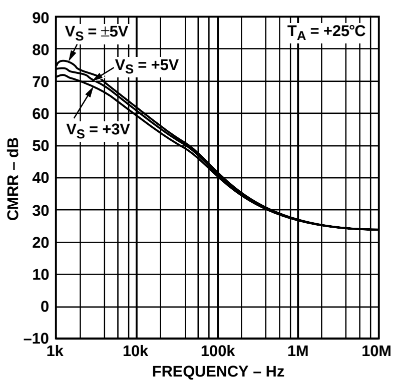


Figure 16. CMRR vs. Frequency

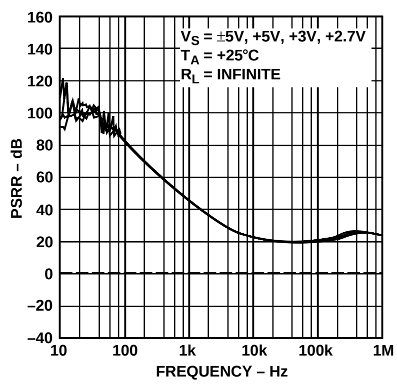


Figure 17. PSRR vs. Frequency

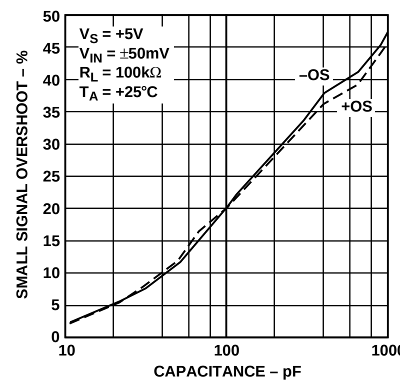


Figure 18. Small Signal Overshoot vs. Load Capacitance

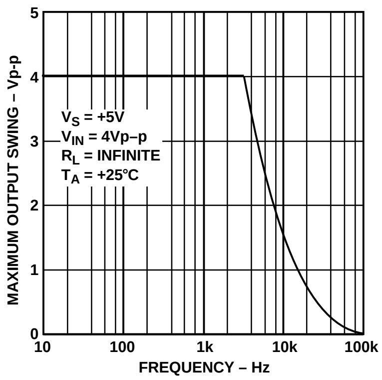


Figure 19. Maximum Output Swing vs. Frequency

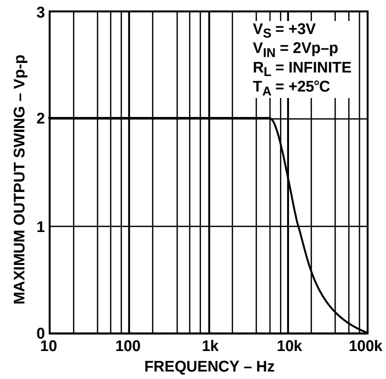


Figure 20. Maximum Output Swing vs. Frequency

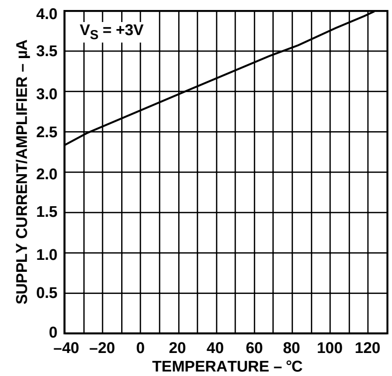


Figure 21. Supply Current/Amplifier vs. Temperature

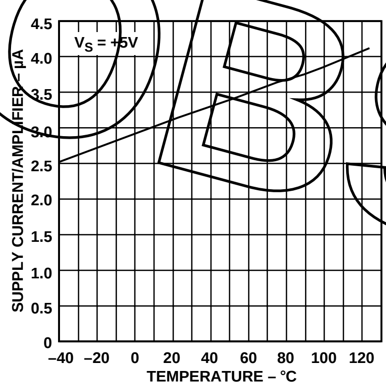


Figure 22. Supply Current/Amplifier vs. Temperature

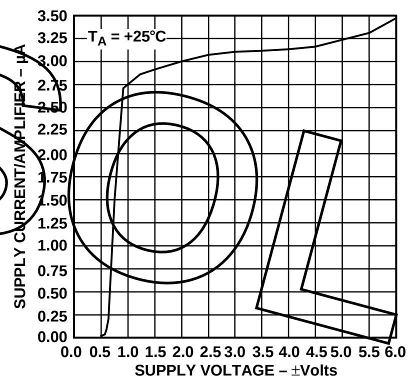


Figure 23. Supply Current/Amplifier vs. Supply Voltage

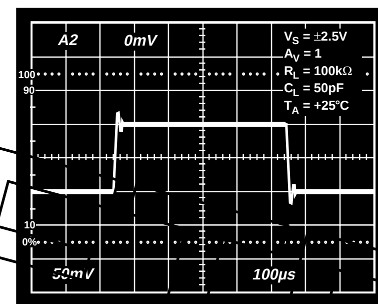


Figure 24. Small Signal Transient Response

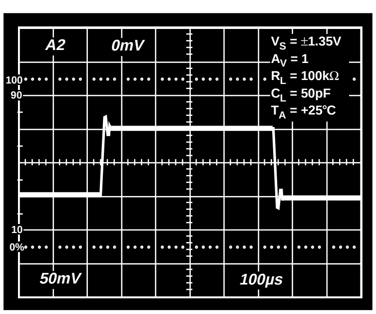


Figure 25. Small Signal Transient Response

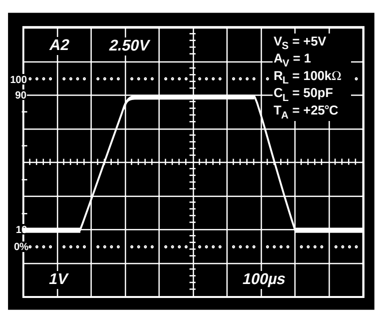


Figure 26. Large Signal Transient Response

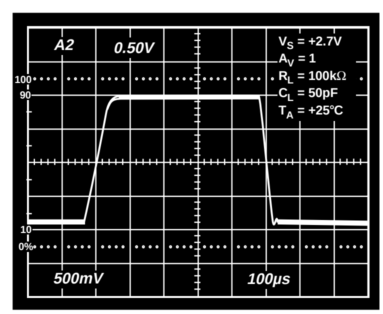


Figure 27. Large Signal Transient Response

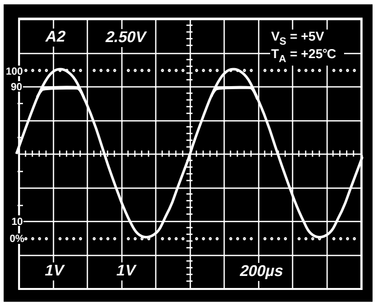


Figure 28. No Phase Reversal

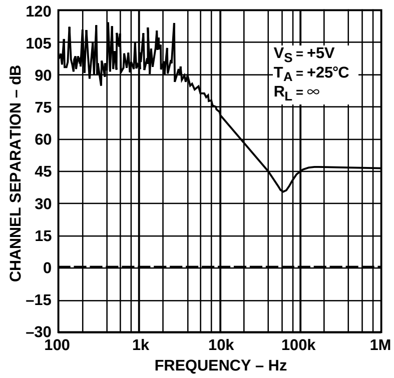


Figure 29. Channel Separation vs. Frequency

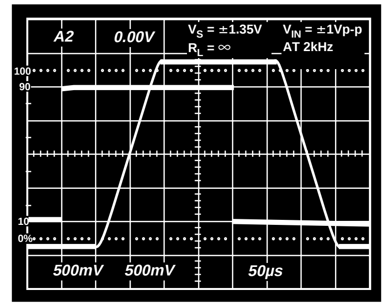


Figure 30. Saturation Recovery Time

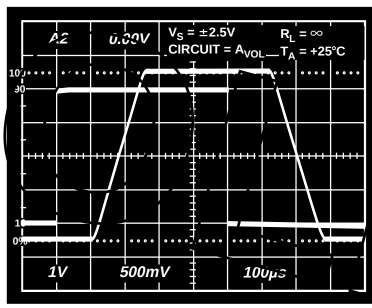


Figure 31. Saturation Recovery Time

APPLICATIONS

THEORY OF OPERATION

The OPx81 family of op amps is comprised of extremely low powered, rail-to-rail output amplifiers, requiring less than 4 μA of quiescent current per amplifier. Many other competitors' devices may be advertised as low supply current amplifiers but draw significantly more current as the outputs of these devices are driven to a supply rail. The OPx81's supply current remains under 4 μA even with the output driven to either supply rail. Supply currents should meet the specification as long as the inputs and outputs remain within the range of the power supplies.

Figure 32 shows a simplified schematic of the OP181. A bipolar differential pair is used in the input stage. PNP transistors are used to allow the input stage to remain linear with the common-mode range extending to ground. This is an important consideration for single supply applications. The bipolar front end also contributes less noise than a MOS front end with only nanoamps of bias currents. The output of the op amp consists of a pair of CMOS transistors in a common source configuration. This setup allows the output of the amplifier to swing to within millivolts of either supply rail. The headroom required by the output stage is limited by the amount of current being driven into the load. The lower the output current, the closer the output can go to either supply rail. Figures 7, 8 and 9 show the output voltage headroom versus load current. This behavior is typical of rail-to-rail output amplifiers.

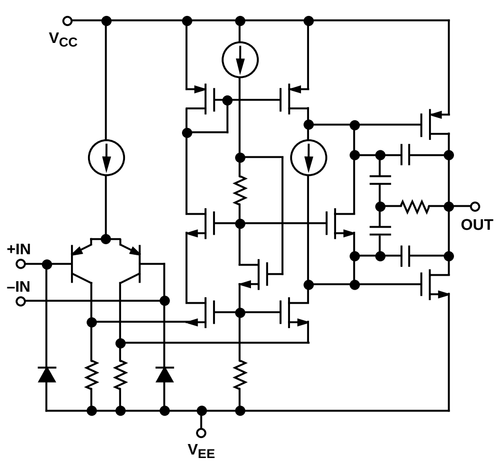


Figure 32. Simplified Schematic of the OP181

Input Overvoltage Protection

The input stage to the OPx81 family of op amps consists of a PNP differential pair. If the base voltage of either of these input transistors drops to more than 0.6 V below the negative supply, the input ESD protection diodes will become forward biased, and large currents will begin to flow. In addition to possibly damaging the device, this will create a phase reversal effect at the output. To prevent these effects from happening, the input current should be limited to less than 0.5 mA.

This can be done quite easily by placing a resistor in series with the input to the device. The size of the resistor should be proportional to the lowest possible input signal excursion and can be found using the following formula:

$$R = \frac{V_{EE} - V_{IN,\,MIN}}{0.5 \times 10^{-3}}$$

where: V_{EE} is the negative power supply for the amplifier, and

$V_{IN,\,MIN}$ is the lowest input voltage excursion expected

For example, an OP181 is to be used with a single supply voltage of 5 V where the input signal could possibly go as low as –1.0 V. Because the amplifier is powered from a single supply, V_{EE} is ground, so the necessary series resistance should be 2 kΩ.

Input Offset Voltage Nulling

The OPx81 family of op amps was designed for low offset voltages less than 1 mV. The single OP181 does provide two offset adjust terminals, should the user require greater precision. In general, these terminals should be used only to zero amplifier offsets and should not be used to adjust system offset voltages.

A 20 kΩ potentiometer connected to the offset adjust terminals, with the wiper connected to V_{EE}, can be used to reduce the offset voltage of the amplifier. The OP181 should be connected in the unity-gain configuration (as shown in Figure 33) or in a gain configuration. The potentiometer should be adjusted until V_{OUT} is minimized. The wiper of the potentiometer must be connected to V_{EE}; connecting it to the positive supply rail could damage the device.

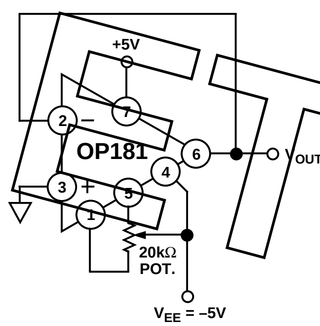


Figure 33. Offset Voltage Nulling Circuit

Input Common-Mode Voltage Range

The OPx81 is rated with an input common-mode voltage range from V_{EE} to 1 volt under V_{CC}. However, the op amp can still operate even with a common-mode voltage that is slightly *less* than V_{EE}. Figure 34 shows an OP181 configured as a difference amplifier with a single supply voltage of +3 V. Negative dc voltages are applied at both input terminals creating a common-mode voltage that is less than ground. A 400 mV p-p input signal is then applied to the noninverting input. Figure 35 shows a picture of the input and output waves. Notice how the output of the amplifier also drops slightly *negative* without distortion.

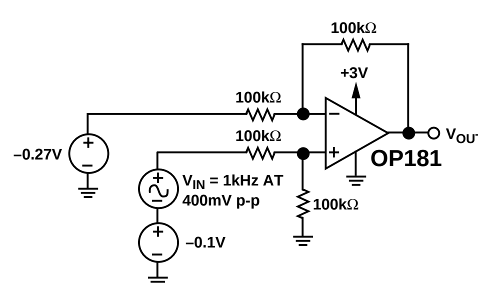


Figure 34. OP181 Configured as a Difference Amplifier Operating at V_{CM} < 0 V

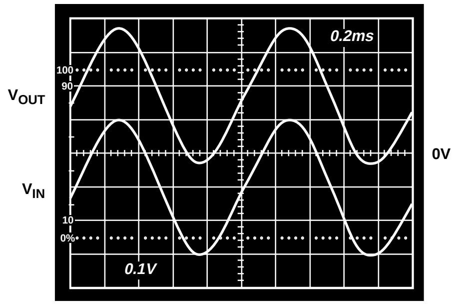


Figure 35. Input and Output Signals with V_{CM} < 0 V

Overdrive Recovery Time

The amount of time it takes for an amplifier to recover from saturation can be an important consideration when using an amplifier as a comparator or when outputs can be driven to the supplies. The overdrive recovery time for the OP181 is 50 µs with the amplifier running from a 3 volt supply and increases to 100 µs with a 10 volt supply. Figure 36 shows the result of the OP181 running from a 3 V supply with its output being overdriven.

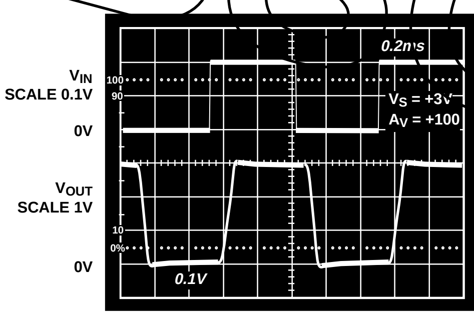


Figure 36. Output of the Op Amp Recovering from Saturation

Capacitive Loading

Most low supply current amplifiers have difficulty driving capacitive loads due to the higher currents required from the output stage for such loads. Higher capacitance at the output will increase the amount of overshoot and ringing in the amplifier's step response and could even affect the stability of the device. However, through careful design of the output stage and its high phase margin, the OPx81 family can tolerate some degree of capacitive loading. Figure 37 shows the step response of an OP181 with a 10 nF capacitor connected at the output. Notice that the overshoot of the output does not exceed more than 10% with such a load, even with a supply voltage of only +3 V.

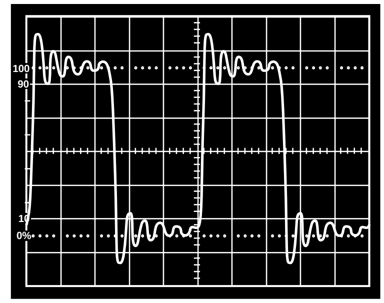


Figure 37. Ringing and Overshoot of the Output of the Amplifier

A Micropower Reference Voltage Generator

Many single supply circuits are configured with the circuit biased to 1/2 of the supply voltage. In these cases, a false-ground reference can be created by using a voltage divider buffered by an amplifier. Figure 38 shows the schematic for such a circuit.

The two 1 MΩ resistors generate the reference voltage while drawing only 1.5 µA of current from a 3 V supply. A capacitor connected from the inverting terminal to the output of the op amp provides compensation to allow for a bypass capacitor to be connected at the reference output. This bypass capacitor helps establish an ac ground for the reference output. The entire reference generator draws less than 5 µA from a 3 V supply source.

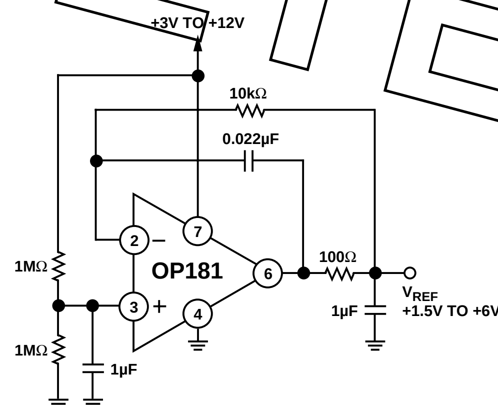


Figure 38. A Micropower Bias Voltage Generator

A Window Comparator

The extremely low power supply current demands of the OPx81 family make it ideal for use in long life battery powered applications such as a monitoring system. Figure 39 shows a circuit that uses the OP281 as a window comparator.

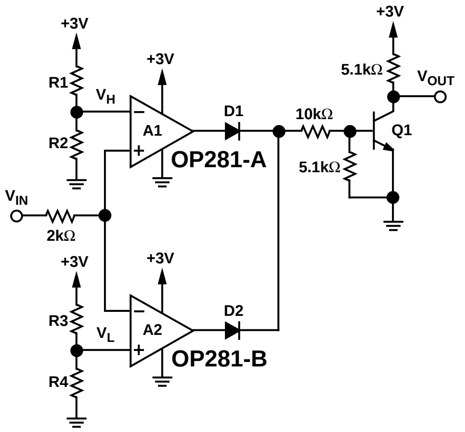


Figure 39. Using the OP281 as a Window Comparator

The threshold limits for the window are set by V_H and V_L, provided that $V_H > V_L$. The output of A1 will stay at the negative rail, in this case ground, as long as the input voltage is less than V_H. Similarly, the output of A2 will stay at ground as long the input voltage is higher than V_L. As long as V_{IN} remains between V_L and V_H, the outputs of both op amps will be 0 V. With no current flowing in either D1 or D2, the base of Q1 will stay at ground, putting the transistor in cutoff and forcing V_{OUT} to the positive supply rail. If the input voltage rises above V_H, the output of A2 stays at ground, but the output of A1 will go to the positive rail, and D1 will conduct current. This creates a base voltage that will turn on Q1 and drive V_{OUT} low. The same condition occurs if V_{IN} falls below V_L with A2's output going high, and D2 conducting current. Therefore, V_{OUT} will be high if the input voltage is between V_L and V_H, and V_{OUT} will be low if the input voltage moves outside of that range.

The R1 and R2 voltage divider sets the upper window voltage, and the R3 and R4 voltage divider sets the lower voltage for the window. For the window comparator to function properly, V_H must be a greater voltage than V_L.

$$V_H = \frac{R2}{R1 + R2}$$

$$V_L = \frac{R4}{R3 + R4}$$

The 2 kΩ resistor connects the input voltage to the input terminals to the op amps. This protects the OP281 from possible excess current flowing into the input stages of the devices. D1 and D2 are small-signal switching diodes (1N4446 or equivalent), and Q1 is a 2N2222 or equivalent NPN transistor.

A Low-Side Current Monitor

In the design of power supply control circuits, a great deal of design effort is focused on ensuring a pass transistor's long-term reliability over a wide range of load current conditions. As a result, monitoring and limiting device power dissipation is of prime importance in these designs. Figure 40 shows an example of a +5 V, single-supply current monitor that can be incorporated into the design of a voltage regulator with fold-back current limiting or a high current power supply with crowbar protection. The design capitalizes on the OP181's common-mode range that extends to ground. Current is monitored in the power supply return path where a 0.1 Ω shunt resistor, R_{SENSE}, creates a very small voltage drop. The voltage at the inverting terminal becomes equal to the voltage at the noninverting terminal through the feedback of Q1, which is a 2N2222 or equivalent NPN transistor. This makes the voltage drop across R1 equal to the voltage drop across R_{SENSE}. Therefore, the current through Q1 becomes directly proportional to the current through R_{SENSE}, and the output voltage is given by:

$$V_{OUT} = V_{EE} - \left(\frac{R2}{R1} \times R_{SENSE} \times I_L \right)$$

The voltage drop across R2 increases with I_L increasing, so V_{OUT} decreases with higher supply current being sensed. For the element values shown, the V_{OUT} transfer characteristic is –2.5 V/A, decreasing from V_{EE}.

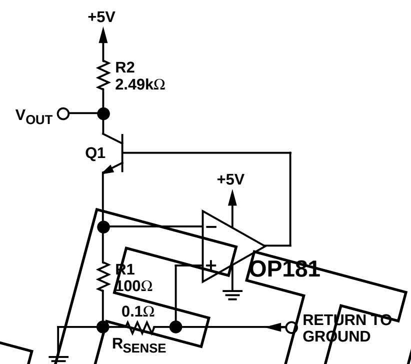


Figure 40. A Low-Side Load Current Monitor

Low Voltage Half-Wave and Full-Wave Rectifiers

Because of its quick overdrive recovery time, an OP281 can be configured as a full-wave rectifier for low frequency (<500 Hz) applications. Figure 41 shows the schematic.

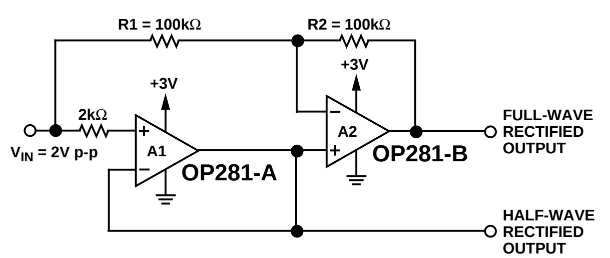


Figure 41. Single Supply Full- and Half-Wave Rectifiers Using an OP281

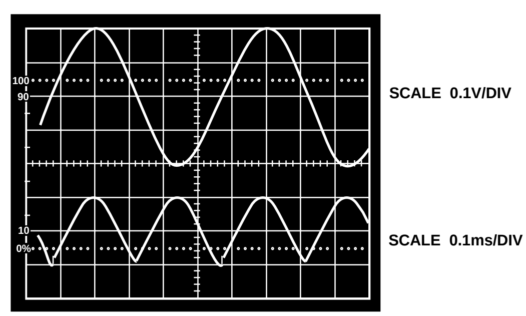


Figure 42. Full-Wave Rectified Signal

Amplifier A1 is used as a voltage follower that will only track the input voltage when it is greater than 0 V. This provides a half-wave rectification of the input signal to the noninverting terminal of amplifier A2. When A1's output is following the input, the inverting terminal of A2 will also follow the input from the virtual ground between the inverting and noninverting terminals of A2. With no potential difference across R1, no current flows through either R1 or R2, therefore the output of A2 will also follow the input. Now, when the input voltage goes below 0 V, the noninverting terminal of A2 becomes 0 V. This makes A2 work as an inverting amplifier with a gain of 1 and provides a full-wave rectified version of the input signal. A 2 kΩ resistor in series with A1's noninverting input protects the device when the input signal becomes less than ground.

A Battery Powered Telephone Headset Amplifier

Figure 43 shows how the OP281 can be used as a two-way amplifier in a telephone headset. One side of the OP281 can be used as an amplifier for the microphone, while the other side can be used to drive the speaker. A typical telephone headset uses a 600 Ω speaker and an electret microphone that requires a supply voltage and a biasing resistor.

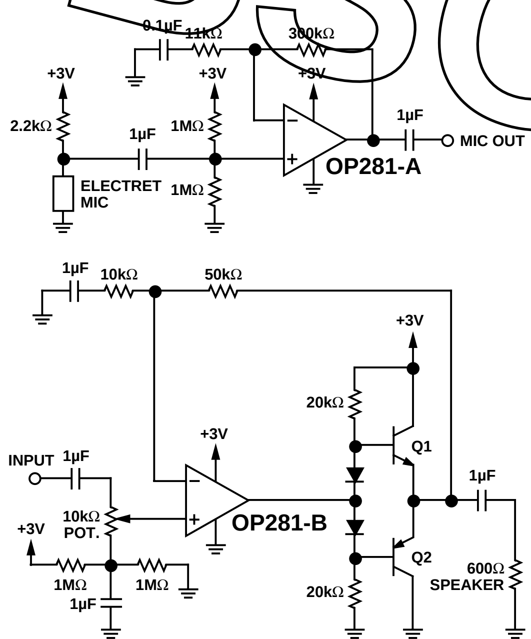


Figure 43. A Battery Powered Telephone Headset Two-Way Amplifier

The OP281-A op amp provides about 29 dB of gain for audio signals coming from the microphone. The gain is set by the 300 kΩ and 11 kΩ resistors. The gain bandwidth product of the amplifier is 95 kHz, which, for the set gain of 28, yields a –3 dB rolloff at 3.4 kHz. This is acceptable since telephone audio is band limited for 300 kHz to 3 kHz signals. If higher gain is required for the microphone, an additional gain stage should be used, as adding any more gain to the OP281 would limit the audio bandwidth. A 2.2 kΩ resistor is used to bias the electret microphone. This resistor value may vary depending on the specifications on the microphone being used. The output of the microphone is ac coupled to the noninverting terminal of the op amp. Two 1 MΩ resistors are used to provide the dc offset for single supply use.

The OP281-B amplifier can provide up to 15 dB of gain for the headset speaker. Incoming audio signals are ac coupled to a 10 kΩ potentiometer that is used to adjust the volume. Again, two 1 MΩ resistors provide the dc offset with a 1 µF capacitor establishing an ac ground for the volume control potentiometer. Because the OP281 is a rail-to-rail output amplifier, it would have difficulty driving a 600 Ω speaker directly. Here, a class AB buffer is used to isolate the load from the amplifier and also provide the necessary current drive to the speaker. By placing the buffer in the feedback loop of the op amp, crossover distortion can be minimized. Q1 and Q2 should have minimum betas of 100. The 600 Ω speaker is ac coupled to the emitters to prevent any quiescent current from flowing in the speaker. The 1 µF coupling capacitor makes an equivalent high pass filter cutoff at 265 Hz with a 600 Ω load attached. Again, this does not pose a problem, as it is outside the frequency range for telephone audio signals.

The circuit in Figure 43 draws around 250 µA of current. The class AB buffer has a quiescent current of 140 µA while roughly 100 µA is drawn by the microphone itself. A CR2032 3 V lithium battery has a life expectancy of 160 mA hours, which means this circuit could run continuously for 640 hours on a single battery.

SPICE Macro-Model

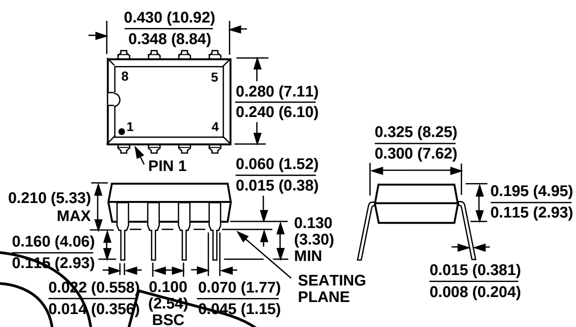
```
* OP181 SPICE Macro-model
* 9/96, Ver. 1
*
* Copyright 1996 by Analog Devices
*
* Refer to "README.DOC" file for License Statement. Use of this
* model indicates your acceptance of the terms and provisions in
* the License Statement.
*
* Node Assignments
*                 noninverting input
*                 |    inverting input
*                 |    |    positive supply
*                 |    |    |    negative supply
*                 |    |    |    |    output
*                 |    |    |    |    |
*                 |    |    |    |    |
.SUBCKT OP181     1    2    99   50   45
*
* INPUT STAGE
*
Q1    4    1    3    PIX
Q2    6    7    5    PIX
I1    99   8    1.28E-6
EOS   7    2    POLY(1)  (12, 98)  80E-6  1
IOS   1    2    1E-10
RC1   4    50   500E3
RC2   6    50   500E3
RE1   3    8    108
RE2   5    8    108
V1    99   13   DC  .9
V2    99   14   DC  .9
D1    3    13   DX
D2    5    14   DX
*
* CMRR 76dB,  ZERO AT 1kHz
*
```

```
ECM1  11  98   POLY(2)   (1, 98)   (2, 98)  0   .5   .5
R1    11  12   1.59E6
C1    11  12   100E-12
R2    12  98   283
*
* POLE AT 900kHz
*
EREF  98   0   (90, 0)     1
G1    98  20   (4, 6)      1E-6
R3    20  98   1E6
C2    20  98   177E-15
*
* POLE AT 500kHz
*
E2    21  98   (20, 98)    1
R4    21  22   1E6
C3    22  98   320E-15
*
* GAIN STAGE
*
CF    45   40   8. 5E-12
R5    40   98   65. 65E6
G3    98   40   (22, 98)    4.08E-7
D3    40   41   DX
D4    42   40   DX
V3    99   41   DC  0.5
V4    42   50   DC  0.5
*
* OUTPUT STAGE
*
ISY   99   50   1.375E-6
RS1   99   90   10E6
RS2   90   50   10E6
M1    45   46   99   99    POX L=1.5u    W=300u
M2    45   47   50   50    NOX L=1.5u    W=300u
EG1   99   46   POLY(1)    (98, 40)   0.77   1
EG2   47   50   POLY(1)    (40, 98)   0.77   1
*
* MODELS
*
.MODEL  POX  PMOS  (LEVEL=2, KP=25E-6, VTO=-0.75, LAMBDA=0.01)
.MODEL  NOX  NMOS  (LEVEL=2, KP=25E-6, VTO=0.75,  LAMBDA=0.01)
.MODEL  PIX  PNP   (BF=200)
.MODEL  DX   D(IS=1E-14)
.ENDS
```

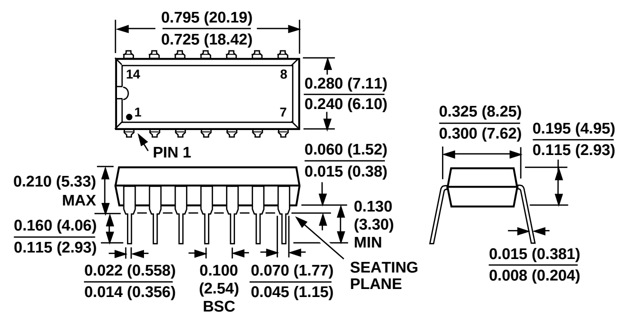
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

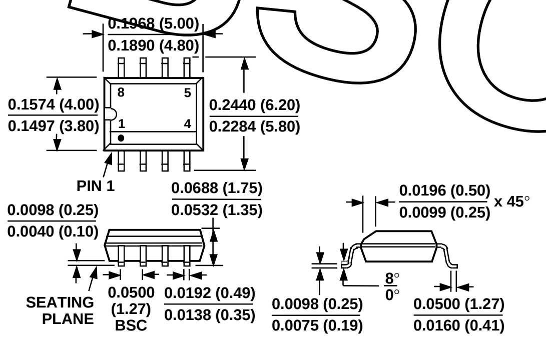
8-Lead Plastic DIP (N-8)



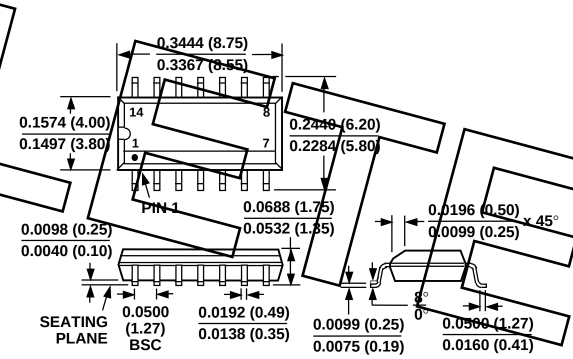
14-Lead Plastic DIP (N-14)



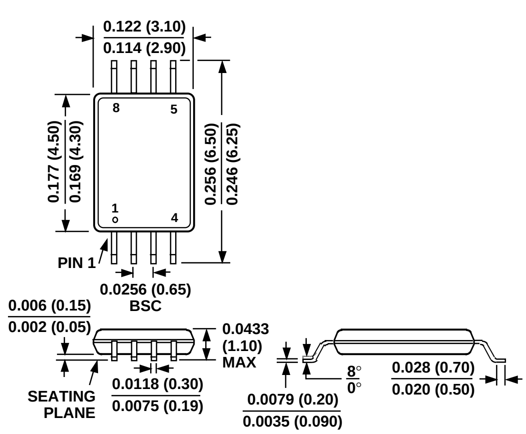
8-Lead SOIC (SO-8)



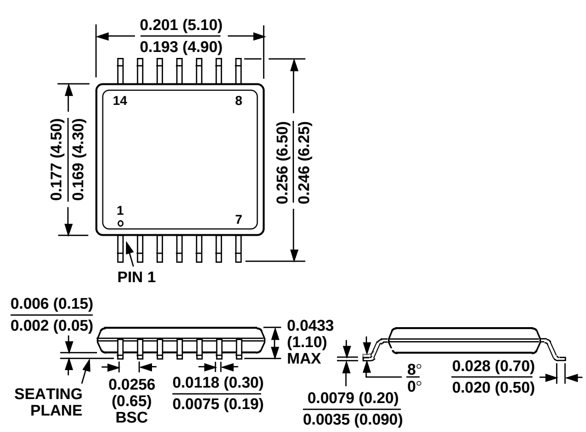
14-Lead Narrow Body SOIC (SO-14)



8-Lead TSSOP (RU-8)



14-Lead TSSOP (RU-14)



C2195-12-10/96

PRINTED IN U.S.A.