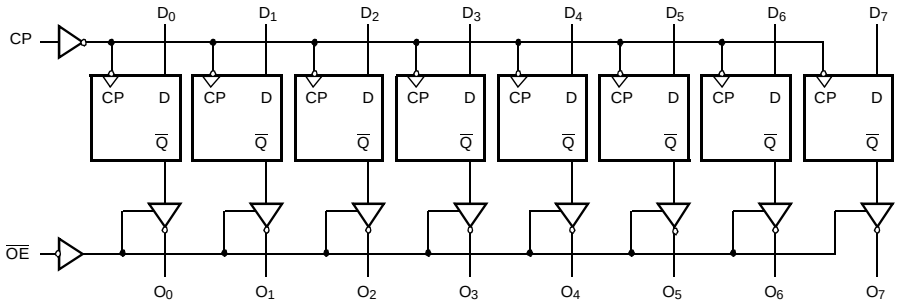
CY54/74FCT374T
CY54/74FCT574T

8-Bit Registers

Features

- **Function, pinout, and drive compatible with FCT and F logic**
- **FCT-C speed at 5.2 ns max. (Com'l)**
  FCT-A speed at 6.5 ns max. (Com'l)
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **ESD > 2000V**
- **Extended commercial range of –40°C to +85°C**
- **Sink Current 64 mA (Com'l), 32 mA (Mil)**
  Source Current 32 mA (Com'l), 12 mA (Mil)
- **Edge-triggered D-type inputs**
- **250 MHz typical toggle rate**

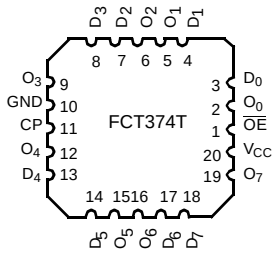
Logic Block Diagram



FCT374T–6

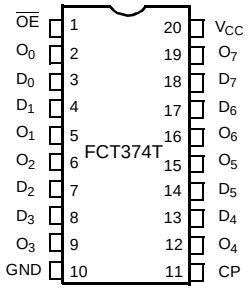
Pin Configurations

LCC
Top View



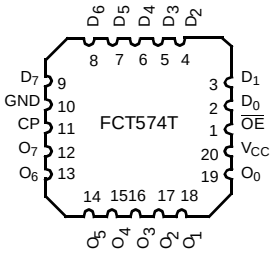
FCT374T–1

DIP/SOIC/QSOP
Top View



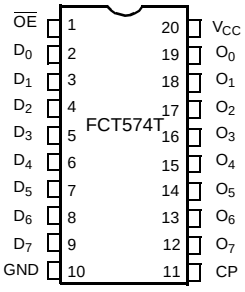
FCT374T–2

LCC
Top View



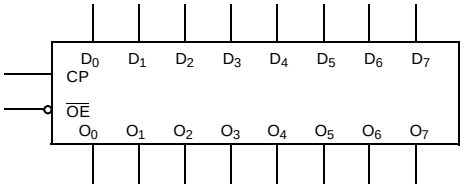
FCT374T–3

DIP/SOIC/QSOP
Top View



FCT374T–4

Logic Symbol



FCT374T–5

Functional Description

The FCT374T and FCT574T are high-speed low-power octal D-type flip-flops featuring separate D-type inputs for each flip-flop. Both devices have three-state outputs for bus oriented applications. A buffered clock (CP) and output enable ($\overline{OE}$) are common to all flip-flops. The FCT574T is identical to FCT374T except for flow-through pinout to simplify board design. The eight flip-flops contained in the FCT374T and FCT574T will store the state of their individual D inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (CP) transition. When $\overline{OE}$ is LOW, the contents of the eight flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs will be in the high-impedance state. The state of output enable does not affect the state of the flip-flops.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

Function Table[1]

Inputs			Outputs
D	**CP**	**OE**	**O**
H	⌐	L	H
L	⌐	L	L
X	X	H	Z

Maximum Ratings[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied ..... –65°C to +135°C

Supply Voltage to Ground Potential .....–0.5V to +7.0V

DC Input Voltage .....–0.5V to +7.0V

DC Output Voltage .....–0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) ..... 120 mA

Power Dissipation..... 0.5W

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V_{CC}
Commercial	DT	0°C to +70°C	5V ± 5%
Commercial	T, AT, CT	–40°C to +85°C	5V ± 5%
Military[4]	All	–55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=–32 mA	Com'l	2.0			V
		V_{CC}=Min., I_{OH}=–15 mA	Com'l	2.4	3.3		V
		V_{CC}=Min., I_{OH}=–12 mA	Mil	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA	Com'l		0.3	0.55	V
		V_{CC}=Min., I_{OL}=32 mA	Mil		0.3	0.55	V
V_{IH}	Input HIGH Voltage			2.0			V
V_{IL}	Input LOW Voltage					0.8	V
V_H	Hysteresis[6]	All inputs			0.2		V
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=–18 mA			–0.7	–1.2	V
I_I	Input HIGH Current	V_{CC}=Max., V_{IN}=V_{CC}				5	µA
I_{IH}	Input HIGH Current	V_{CC}=Max., V_{IN}=2.7V				±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_{IN}=0.5V				±1	µA
I_{OZH}	Off State HIGH-Level Output Current	V_{CC} = Max., V_{OUT} = 2.7V				10	µA
I_{OZL}	Off State LOW-Level Output Current	V_{CC} = Max., V_{OUT} = 0.5V				–10	µA
I_{OS}	Output Short Circuit Current[7]	V_{CC}=Max., V_{OUT}=0.0V		–60	–120	–225	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}=4.5V				±1	µA

Notes:

1. H = HIGH Voltage Level. L = LOW Voltage Level X = Don't Care Z = HIGH Impedance = LOW-to-HIGH clock transition
2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. T_A is the "instant on" case temperature.
5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
6. This parameter is guaranteed but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameters tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Capacitance[2]

Parameter	Description	Typ.[5]	Max.	Unit
C_{IN}	Input Capacitance	5	10	pF
C_{OUT}	Output Capacitance	9	12	pF

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max., $V_{IN}\leq$0.2V, $V_{IN}\geq V_{CC}$–0.2V	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max., V_{IN}=3.4V,[8] f_1=0, Outputs Open	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[9]	V_{CC}=Max., One Bit Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$=GND, $V_{IN}\leq$0.2V or $V_{IN}\geq V_{CC}$–0.2V	0.06	0.12	mA/MHz
I_C	Total Power Supply Current[10]	V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, $\overline{OE}$=GND, $V_{IN}\leq$0.2V or $V_{IN}\geq V_{CC}$–0.2V	0.7	1.4	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1=5 MHz, $\overline{OE}$=GND, V_{IN}=3.4V or V_{IN}=GND	1.2	3.4	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=2.5 MHz, $\overline{OE}$=GND, $V_{IN}\leq$0.2V or $V_{IN}\geq V_{CC}$–0.2V	1.6	3.2[11]	mA
		V_{CC}=Max., f_0=10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1=2.5 MHz, $\overline{OE}$=GND, V_{IN}=3.4V or V_{IN}=GND	3.9	12.2[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC}+\Delta I_{CC}D_HN_T+I_{CCD}(f_0/2 + f_1N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Switching Characteristics[12] Over the Operating Range

Parameter	Description	FCT374T/FCT574T				FCT374AT/FCT574AT				Unit	Fig. No.[13]
		Military		Commercial		Military		Commercial			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Clock to Output	2.0	11.0	2.0	10.0	2.0	7.2	2.0	6.5	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time	1.5	14.0	1.5	12.5	1.5	7.5	1.5	6.5	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	8.0	1.5	8.0	1.5	6.5	1.5	5.5	ns	1, 7, 8
t_S	Set–Up Time HIGH or LOW D to CP	2.0		2.0		2.0		2.0		ns	4
t_H	Hold Time HIGH or LOW D to CP	1.5		1.5		1.5		1.5		ns	4
t_W	Clock Pulse Width[14] HIGH or LOW	7.0		7.0		6.0		5.0		ns	5

Parameter	Description	FCT374CT/FCT574CT				FCT374DT/ FCT574DT		Unit	Fig. No.[13]
		Military		Commercial		Commercial			
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Clock to Output	2.0	6.2	2.0	5.2	2.0	4.2	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time	1.5	6.2	1.5	5.5	1.5	4.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	5.7	1.5	5.0	1.5	4.0	ns	1, 7, 8
t_S	Set-Up Time, HIGH or LOW D to CP	2.0		2.0		2.0		ns	4
t_H	Hold Time, HIGH or LOW D to CP	1.5		1.5		1.5		ns	4
t_W	Clock Pulse Width[14] HIGH or LOW	6.0		5.0		3.0		ns	5

Shaded areas contain preliminary information.

Notes:

12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. See “Parameter Measurement Information” in the General Information section.
14. With one data channel toggling, $t_W(L)=t_W(H)=4.0$ ns and $t_r=t_f=1.0$ ns.

Ordering Information—FCT374T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.2	CY74FCT374DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT374DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.2	CY74FCT374CTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT374CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
6.2	CY54FCT374CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT374CTLMB	L61	20-Pin Square Leadless Chip Carrier	
6.5	CY74FCT374ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT374ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT374ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
7.2	CY54FCT374ATLMB	L61	20-Pin Square Leadless Chip Carrier	Military
10.0	CY74FCT374TQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT374TSOC	S5	20-Lead (300-Mil) Molded SOIC	
11.0	CY54FCT374TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT374TLMB	L61	20-Pin Square Leadless Chip Carrier-	

Ordering Information—FCT574T

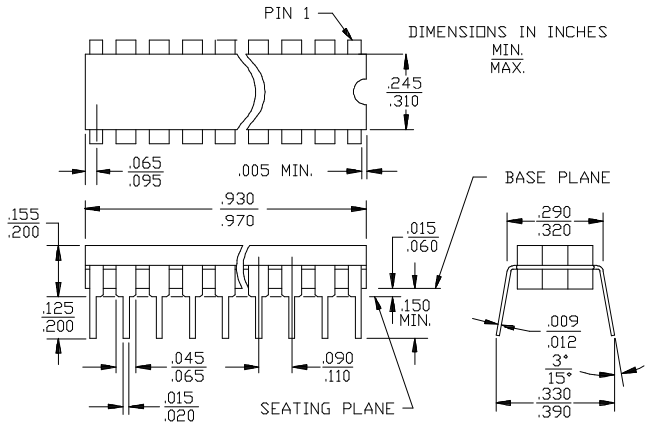
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.2	CY74FCT574DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT574DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.2	CY74FCT574CTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT574CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
6.2	CY54FCT574CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
6.5	CY74FCT574ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT574ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT574ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
7.2	CY54FCT574ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
10.0	CY74FCT574TQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT574TSOC	S5	20-Lead (300-Mil) Molded SOIC	
11.0	CY54FCT574TDMB	D6	20-Lead (300-Mil) CerDIP	Military

Shaded areas contain preliminary information.

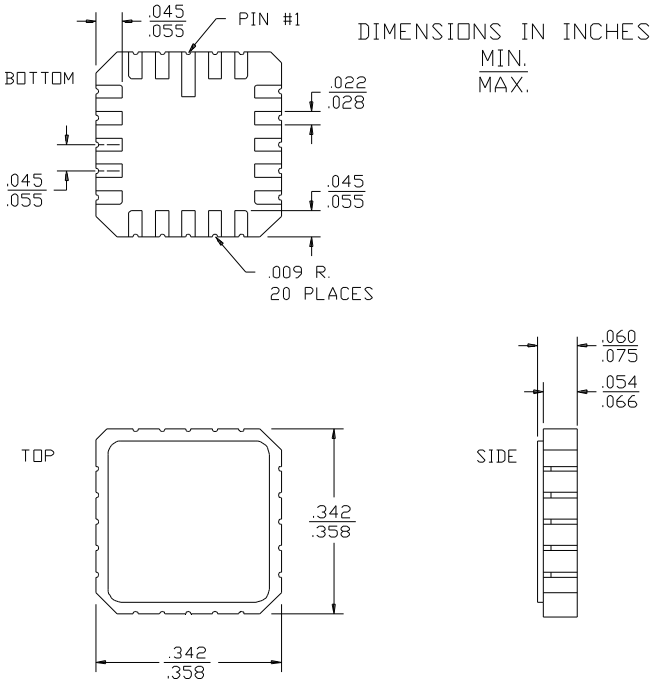
Document #: 38-00278-B

Package Diagrams

20-Lead (300-Mil) CerDIP D6
MIL-STD-1835 D- 8Config.A

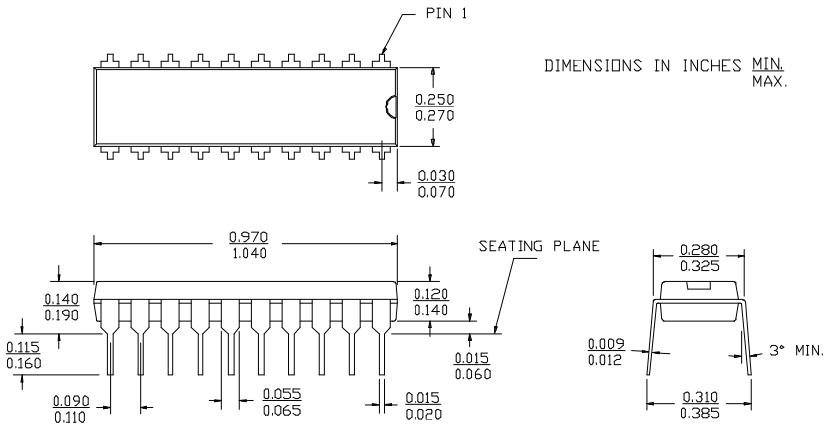


20-Pin Square Leadless Chip Carrier L61
MIL-STD-1835 C-2A

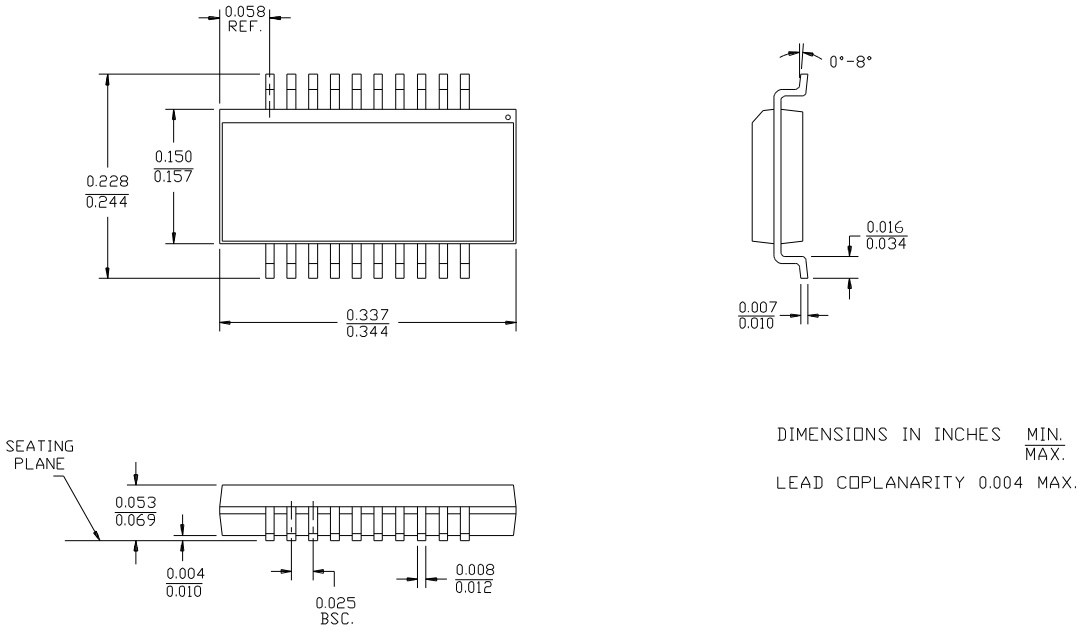


Package Diagrams (continued)

20-Lead (300-Mil) Molded DIP P5



20-Lead Quarter Size Outline Q5



Package Diagrams (continued)

20-Lead (300-Mil) Molded SOIC S5