DS90CP22 800 Mbps 2x2 LVDS Crosspoint Switch

Check for Samples: DS90CP22

FEATURES

- **DC - 800 Mbps Low Jitter, Low Skew Operation**
- **65 ps (typ) of Pk-Pk Jitter with PRBS = $2^{23}-1$ Data Pattern at 800 Mbps**
- **Single +3.3 V Supply**
- **Less than 330 mW (typ) Total Power Dissipation**
- **Non-Blocking "'Switch Architecture"'**
- **Balanced Output Impedance**
- **Output Channel-to-Channel Skew is 35 ps (typ)**
- **Configurable as 2:1 mux, 1:2 demux, Repeater or 1:2 Signal Splitter**
- **LVDS Receiver Inputs Accept LVPECL Signals**
- **Fast Switch Time of 1.2ns (typ)**
- **Fast Propagation Delay of 1.3ns (typ)**
- **Receiver Input Threshold < ±100 mV**
- **Available in 16 Lead TSSOP and SOIC Packages**
- **Conforms to ANSI/TIA/EIA-644-1995 LVDS Standard**
- **Operating Temperature: −40°C to +85°C**

DESCRIPTION

DS90CP22 is a 2x2 crosspoint switch utilizing LVDS (Low Voltage Differential Signaling) technology for low power, high speed operation. Data paths are fully differential from input to output for low noise generation and low pulse width distortion. The non-blocking design allows connection of any input to any output or outputs. LVDS I/O enable high speed data transmission for point-to-point interconnects. This device can be used as a high speed differential crosspoint, 2:1 mux, 1:2 demux, repeater or 1:2 signal splitter. The mux and demux functions are useful for switching between primary and backup circuits in fault tolerant systems. The 1:2 signal splitter and 2:1 mux functions are useful for distribution of serial bus across several rack-mounted backplanes.

The DS90CP22 accepts LVDS signal levels, LVPECL levels directly or PECL with attenuation networks.

The individual LVDS outputs can be put into TRI-STATE by use of the enable pins.

For more details, please refer to the Application Information section of this datasheet.

Connection Diagram

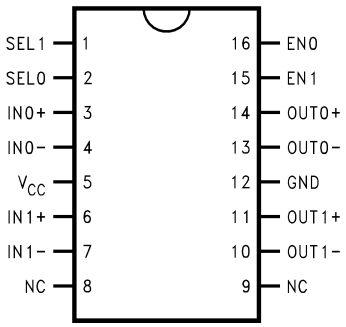


Figure 1. SOIC-16 Package or TSSOP-16 Package

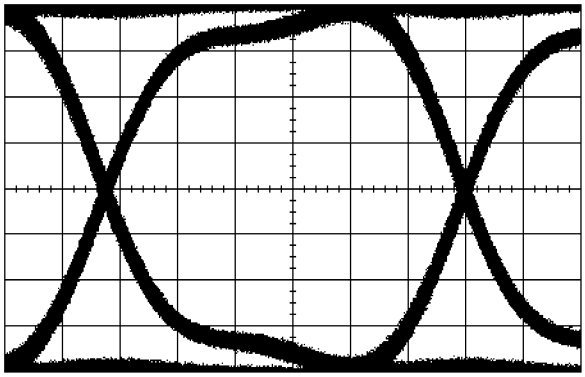


Figure 2. Diff. Output Eye-Pattern in 1:2 split mode @ 800 Mbps
Conditions: 3.3 V, PRBS = 2^{23}−1 data pattern,
V_{ID} = 300mV, V_{CM} = +1.2 V, 200 ps/div, 100 mV/div

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Supply Voltage (V_{CC})		−0.3V to +4V
CMOS/TTL Input Voltage (EN0, EN1, SEL0, SEL1)		−0.3V to (V_{CC} + 0.3V)
LVDS Receiver Input Voltage (IN+, IN−)		−0.3V to +4V
LVDS Driver Output Voltage (OUT+, OUT−)		−0.3V to +4V
LVDS Output Short Circuit Current		Continuous
Junction Temperature		+150°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)		+260°C
Maximum Package Power Dissipation at 25°C	16L SOIC	1.435 W
	16L SOIC Package Derating	11.48 mW/°C above +25°C
	16L TSSOP	0.866 W
	16L TSSOP Package Derating	9.6 mW/°C above +25°C
ESD Rating	(HBM, 1.5kΩ, 100pF)	> 5 kV
	(EIAJ, 0Ω, 200pF)	> 250 V

(1) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(2) "Absolute Maximum Ratings" are these beyond which the safety of the device cannot be verified. They are not meant to imply that the device should be operated at these limits. "Electrical Characteristics" provides conditions for actual device operation.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Receiver Input Voltage	0		V_{CC}	V
Operating Free Air Temperature	-40	+25	+85	°C

Electrical Characteristics[1]

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS/TTL DC SPECIFICATIONS (EN0,EN1,SEL0,SEL1)						
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
I_{IH}	High Level Input Current	V_{IN} = 3.6V or 2.0V; V_{CC} = 3.6V		+7	+20	µA
I_{IL}	Low Level Input Current	V_{IN} = 0V or 0.8V; V_{CC} = 3.6V		±1	±10	µA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA		−0.8	−1.5	V
LVDS OUTPUT DC SPECIFICATIONS (OUT0,OUT1)						
V_{OD}	Differential Output Voltage	R_L = 75Ω	270	365	475	mV
		R_L = 75Ω, V_{CC} = 3.3V, T_A = 25°C	285	365	440	mV
ΔV_{OD}	Change in V_{OD} between Complimentary Output States				35	mV
V_{OS}	Offset Voltage[2]		1.0	1.2	1.45	V
ΔV_{OS}	Change in V_{OS} between Complimentary Output States				35	mV
I_{OZ}	Output TRI-STATE Current	TRI-STATE Output,		±1	±10	µA
		V_{OUT} = V_{CC} or GND				
I_{OFF}	Power-Off Leakage Current	V_{CC} = 0V; V_{OUT} = 3.6V or GND		±1	±10	µA
I_{OS}	Output Short Circuit Current	V_{OUT+} OR V_{OUT-} = 0V		−15	−25	mA
I_{OSB}	Both Outputs Short Circuit Current	V_{OUT+} AND V_{OUT-} = 0V		−30	−50	mA
LVDS RECEIVER DC SPECIFICATIONS (IN0,IN1)						
V_{TH}	Differential Input High Threshold	V_{CM} = +0.05V or +1.2V or +3.25V,		0	+100	mV
V_{TL}	Differential Input Low Threshold	Vcc = 3.3V	−100	0		mV
V_{CMR}	Common Mode Voltage Range	V_{ID} = 100mV, Vcc = 3.3V	0.05		3.25	V
I_{IN}	Input Current	V_{IN} = +3.0V, V_{CC} = 3.6V or 0V		±1	±10	µA
		V_{IN} = 0V, V_{CC} = 3.6V or 0V		±1	±10	µA
SUPPLY CURRENT						
I_{CCD}	Total Supply Current	R_L = 75Ω, C_L = 5 pF, EN0 = EN1 = High		98	125	mA
I_{CCZ}	TRI-STATE Supply Current	EN0 = EN1 = Low		43	55	mA

(1) All typical are given for V_{CC} = +3.3V and T_A = +25°C, unless otherwise stated.
(2) V_{OS} is defined and measured on the ATE as (V_{OH} + V_{OL}) / 2.

AC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{SET}	Input to SEL Setup Time[2], (Figure 3 and Figure 4)		0.7	0.5		ns
T_{HOLD}	Input to SEL Setup Time[2], (Figure 3 and Figure 4)		1.0	0.5		ns
T_{SWITCH}	SEL to Switched Output, (Figure 3 and Figure 4)		0.9	1.2	1.7	ns
T_{PHZ}	Disable Time (Active to TRI-STATE) High to Z, Figure 5			2.1	4.0	ns
T_{PLZ}	Disable Time (Active to TRI-STATE) Low to Z, Figure 5			3.0	4.5	ns
T_{PZH}	Enable Time (TRI-STATE to Active) Z to High, Figure 5			25.5	55.0	ns
T_{PZL}	Enable Time (TRI-STATE to Active) Z to Low, Figure 5			25.5	55.0	ns
T_{LHT}	Output Low-to-High Transition Time, 20% to 80%, Figure 7		290	400	580	ps
T_{HLT}	Output High-to-Low Transition Time, 80% to 20%, Figure 7		290	400	580	ps

(1) The parameters are specified by design. The limits are based on statistical analysis of the device performance over PVT (process, voltage and temperature) range.
(2) T_{SET} and T_{HOLD} time specify that data must be in a stable state before and after the SEL transition.

AC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{JIT}	LVDS Data Path Peak to Peak Jitter(3)	V_{ID} = 300mV; 50% Duty Cycle; V_{CM} = 1.2V at 800Mbps		40	90	ps
		V_{ID} = 300mV; PRBS=2^{23}-1 data pattern; V_{CM} = 1.2V at 800Mbps		65	120	ps
T_{PLHD}	Propagation Low to High Delay, Figure 8		0.9	1.3	1.6	ns
	Propagation Low to High Delay, Figure 8	V_{CC} = 3.3V, T_A = 25°C	1.0	1.3	1.5	ns
T_{PHLD}	Propagation High to Low Delay, Figure 8		0.9	1.3	1.6	ns
	Propagation High to Low Delay, Figure 8	V_{CC} = 3.3V, T_A = 25°C	1.0	1.3	1.5	ns
T_{SKEW}	Pulse Skew $\|T_{PLHD} - T_{PHLD}\|$			0	225	ps
T_{CCS}	Output Channel-to-Channel Skew, Figure 9			35	80	ps

(3) The parameters are specified by design. The limits are based on statistical analysis of the device performance over PVT range with the following equipment test setup: HP70004A (display mainframe) with HP70841B (pattern generator), 5 feet of RG-142 cable with DUT test board and HP83480A (digital scope mainframe) with HP83483A (20GHz scope module).

AC Timing Diagrams

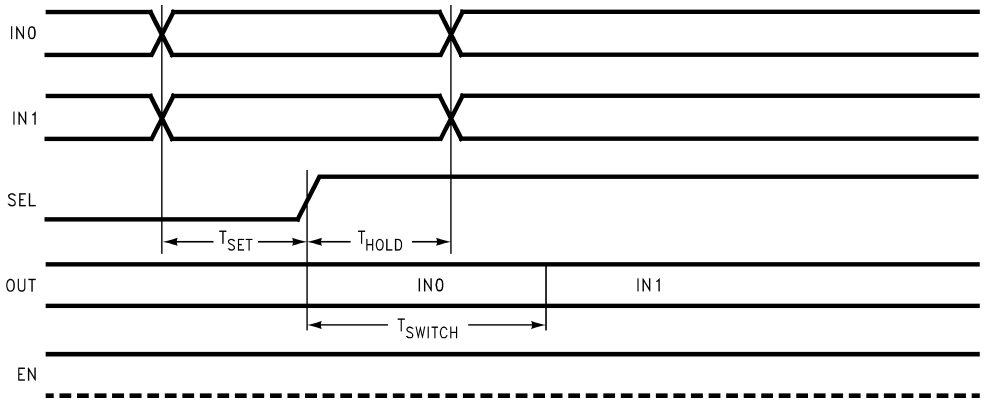


Figure 3. Input-to-Select rising edge setup and hold times and mux switch time

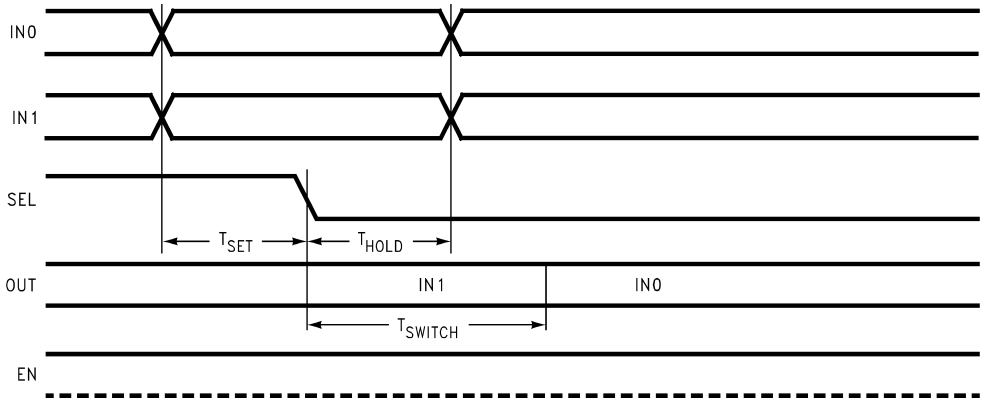


Figure 4. Input-to-Select falling edge setup and hold times and mux switch time

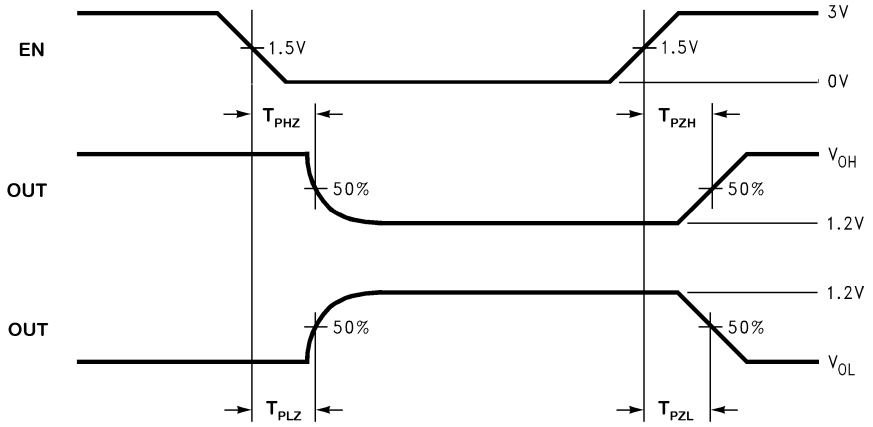


Figure 5. Output active to TRI-STATE and TRI-STATE to active output time

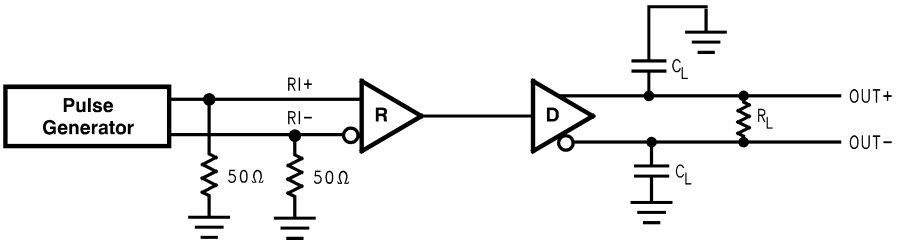


Figure 6. LVDS Output Load

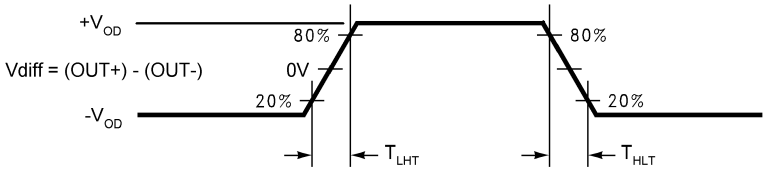


Figure 7. LVDS Output Transition Time

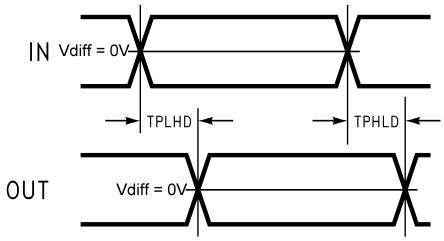


Figure 8. Propagation Delay Low-to-High and High-to-Low

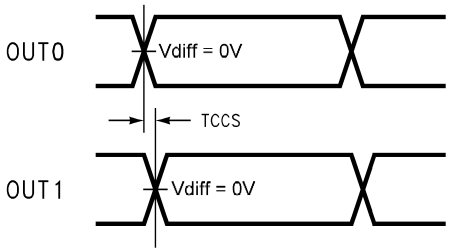


Figure 9. Output Channel-to-Channel Skew in 1:2 splitter mode

PIN DESCRIPTIONS

Pin Name	# of Pin	Input/Output	Description
IN+	2	I	Non-inverting LVDS input
IN -	2	I	Inverting LVDS input
OUT+	2	O	Non-inverting LVDS Output
OUT -	2	O	Inverting LVDS Output
EN	2	I	A logic low on the Enable puts the LVDS output into TRI-STATE and reduces the supply current
SEL	2	I	2:1 mux input select
GND	1	P	Ground
V_{CC}	1	P	Power Supply
NC	2		No Connect

APPLICATION INFORMATION

MODES OF OPERATION

The DS90CP22 provides three modes of operation. In the 1:2 splitter mode, the two outputs are copies of the same single input. This is useful for distribution / fan-out applications. In the repeater mode, the device operates as a 2 channel LVDS buffer. Repeating the signal restores the LVDS amplitude, allowing it to drive another media segment. This allows for isolation of segments or long distance applications. The switch mode provides a crosspoint function. This can be used in a system when primary and redundant paths are supported in fault tolerant applications.

INPUT FAIL-SAFE

The receiver inputs of the DS90CP22 do not have internal fail-safe biasing. For point-to-point and multidrop applications with a single source, fail-safe biasing may not be required. When the driver is off, the link is in-active. If fail-safe biasing is required, this can be accomplished with external high value resistors. The IN+ should be pull to Vcc with 10kΩ and the IN− should be pull to Gnd with 10kΩ. This provides a slight positive differential bias, and sets a known HIGH state on the link with a minimum amount of distortion.

UNUSED LVDS INPUTS

Unused LVDS Receiver inputs should be tied off to prevent the high-speed sensitive input stage from picking up noise signals. The open input to IN+ should be pull to Vcc with 10kΩ and the open input to IN− should be pull to Gnd with 10kΩ.

UNUSED CONTROL INPUTS

The SEL and EN control input pins have internal pull down devices. Unused pins may be tied off or left as no-connect (if a LOW state is desired).

EXPANDING THE NUMBER OF OUTPUT PORTS

To expand the number of output ports, more than one DS90CP22 can be used. Total propagation delay through the devices should be considered to determine the maximum expansion. For example, if 2 X 4 is desired, than three of the DS90CP22 are required. A minimum of two device propagation delays (2 x 1.3ns = 2.6ns (typ)) can be achieved. For a 2 X 8, a total of 7 devices must be used with propagation delay of 3 x 1.3ns = 3.9ns (typ). The power consumption will increase proportional to the number of devices used.

PCB LAYOUT AND POWER SYSTEM BYPASS

Circuit board layout and stack-up for the DS90CP22 should be designed to provide noise-free power to the device. Good layout practice also will separate high frequency or high level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (4 to 10 mils) for power/ground sandwiches. This increases the intrinsic capacitance of the PCB power system which improves power supply filtering, especially at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range 0.01 µF to 0.1 µF. It is recommended practice to use two vias at each power pin of the DS90CP22 as well as all RF bypass capacitor terminals. Dual vias reduce the interconnect inductance by up to half, thereby reducing interconnect inductance and extending the effective frequency range of the bypass components.

The outer layers of the PCB may be flooded with additional ground plane. These planes will improve shielding and isolation as well as increase the intrinsic capacitance of the power supply plane system. Naturally, to be effective, these planes must be tied to the ground supply plane at frequent intervals with vias. Frequent via placement also improves signal integrity on signal transmission lines by providing short paths for image currents which reduces signal distortion.

There are more common practices which should be followed when designing PCBs for LVDS signaling.

COMPATIBILITY WITH LVDS STANDARD

The DS90CP22 is compatible with LVDS and Bus LVDS Interface devices. It is enhanced over standard LVDS drivers in that it is able to driver lower impedance loads with standard LVDS levels. Standard LVDS drivers provide 330mV differential output with a 100Ω load. The DS90CP22 provides 365mV with a 75Ω load or 400mV with 100Ω loads. This extra drive capability is useful in certain multidrop applications.

In backplane multidrop configurations, with closely spaced loads, the effective differential impedance of the line is reduced. If the mainline has been designed for 100Ω differential impedance, the loading effects may reduce this to the 70Ω range depending upon spacing and capacitance load. Terminating the line with a 75Ω load is a better match than with 100Ω and reflections are reduced.

BLOCK DIAGRAM

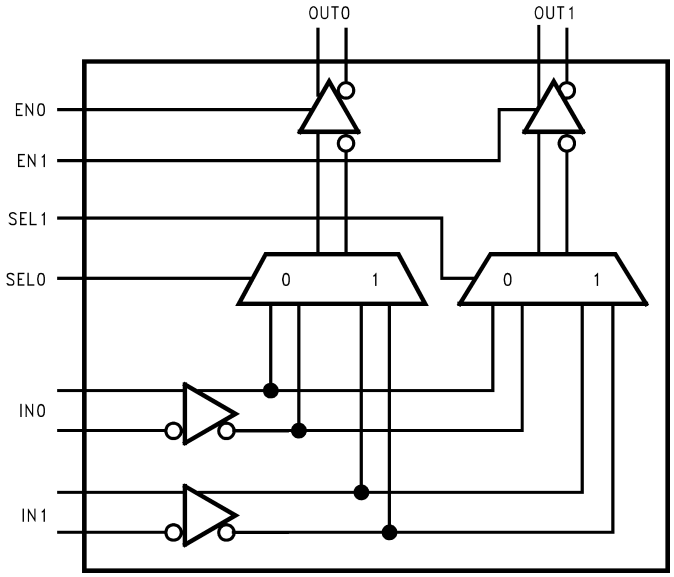


Table 1. Function Table

SEL0	SEL1	OUT0	OUT1	Mode
0	0	IN0	IN0	1:2 splitter
0	1	IN0	IN1	repeater
1	0	IN1	IN0	switch
1	1	IN1	IN1	1:2 splitter

Typical Performance Characteristics

Diff. Output Voltage (V_{OD}) vs. Resistive Load (R_T)

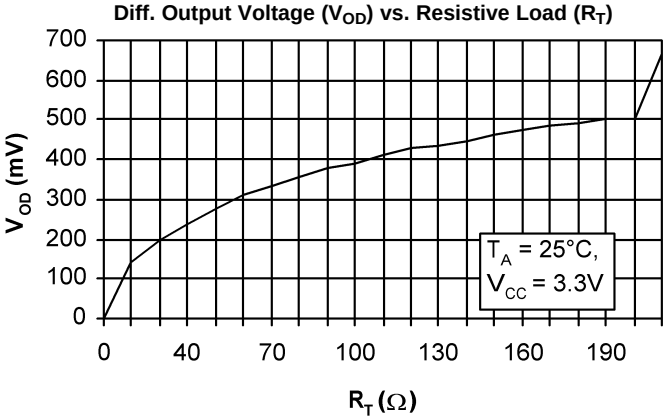


Figure 10.

Peak-to-Peak Output Jitter at V_{CM} = +0.4V vs. VID

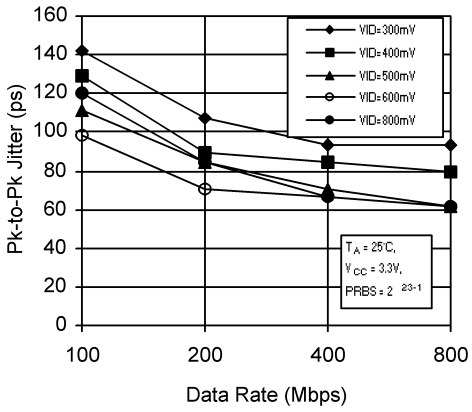


Figure 11.

Peak-to-Peak Output Jitter at V_{CM} = +1.2V vs. VID

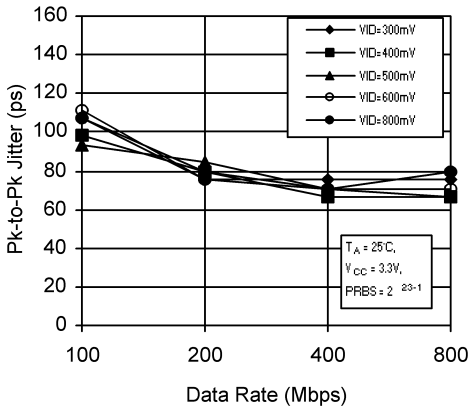


Figure 12.

Peak-to-Peak Output Jitter at V_{CM} = +1.6V vs. VID

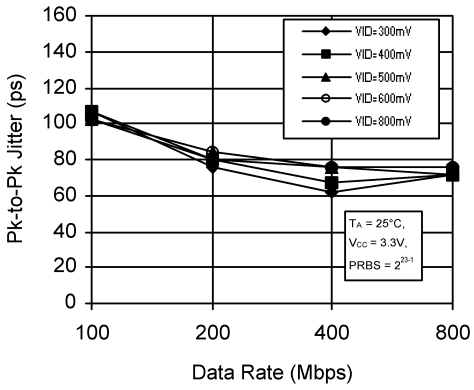


Figure 13.

REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	9

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90CP22M-8	NRND	SOIC	D	16	48	TBD	Call TI	Call TI	-40 to 85	DS90CP22M -8	
DS90CP22M-8/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	DS90CP22M -8	Samples
DS90CP22MT	NRND	TSSOP	PW	16	92	TBD	Call TI	Call TI	-40 to 85	DS90CP 22MT	
DS90CP22MT/NOPB	ACTIVE	TSSOP	PW	16	92	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	DS90CP 22MT	Samples
DS90CP22MTX/NOPB	ACTIVE	TSSOP	PW	16	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	DS90CP 22MT	Samples
DS90CP22MX-8/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 85	DS90CP22M -8	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

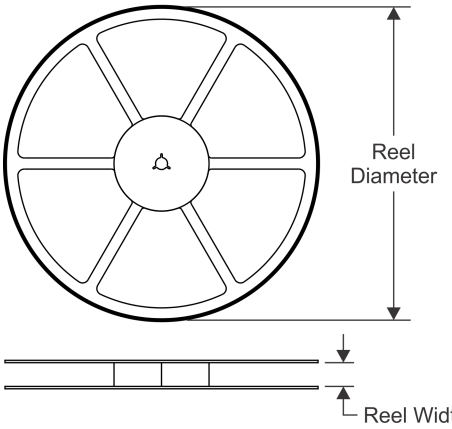
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

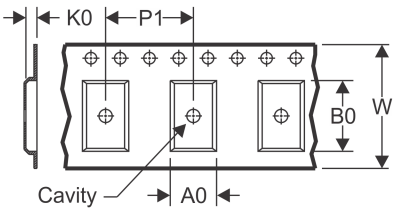
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

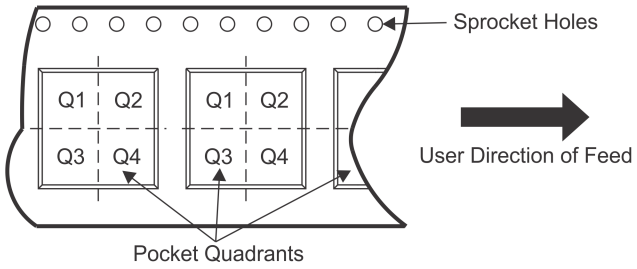


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

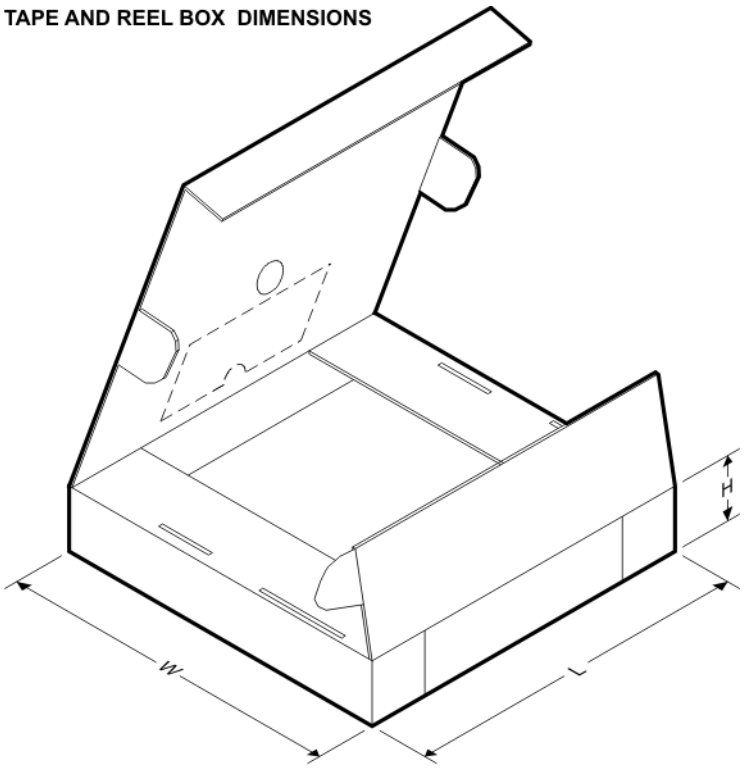
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90CP22MTX/NOPB	TSSOP	PW	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
DS90CP22MX-8/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

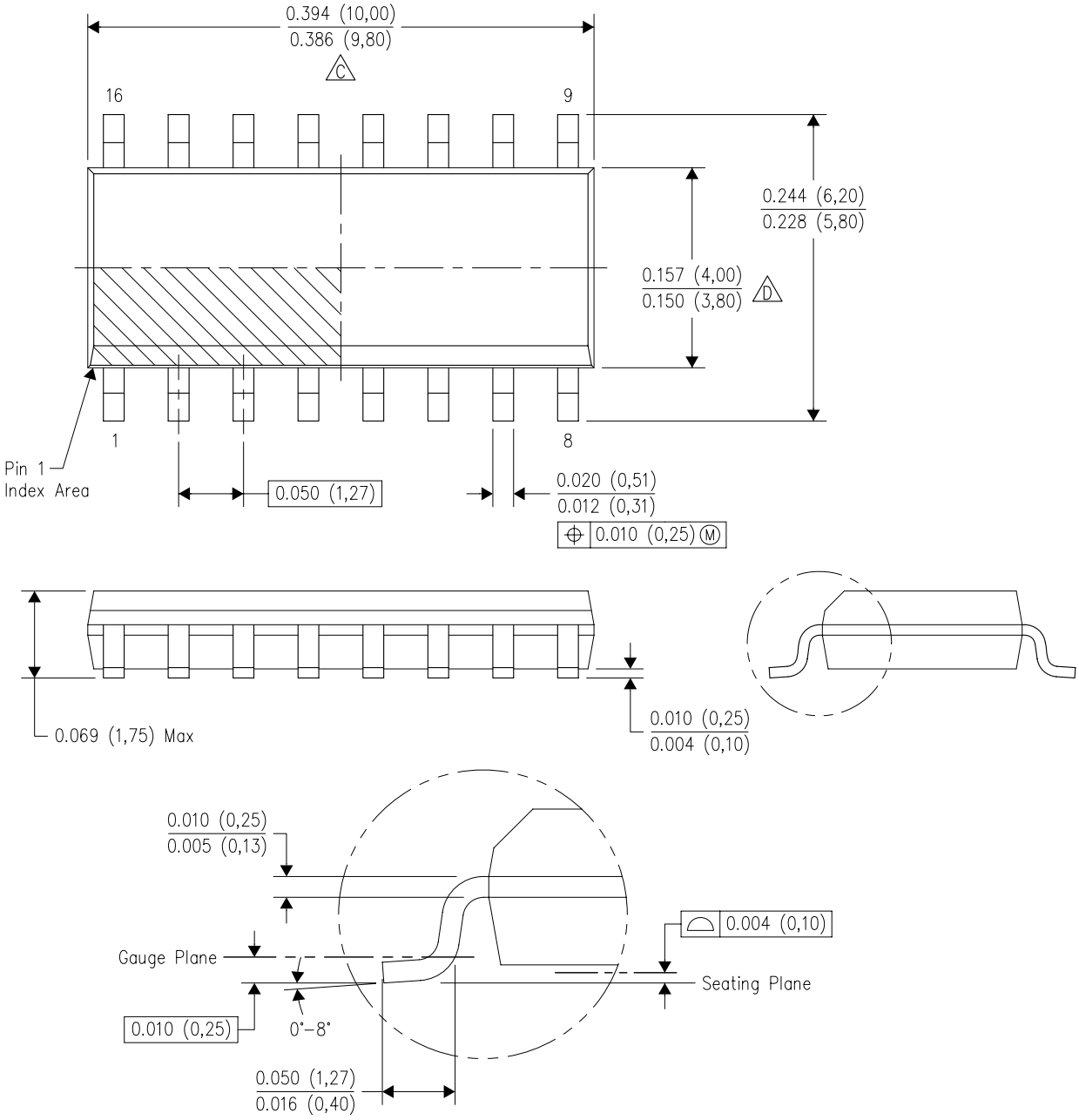
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90CP22MTX/NOPB	TSSOP	PW	16	2500	367.0	367.0	35.0
DS90CP22MX-8/NOPB	SOIC	D	16	2500	367.0	367.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



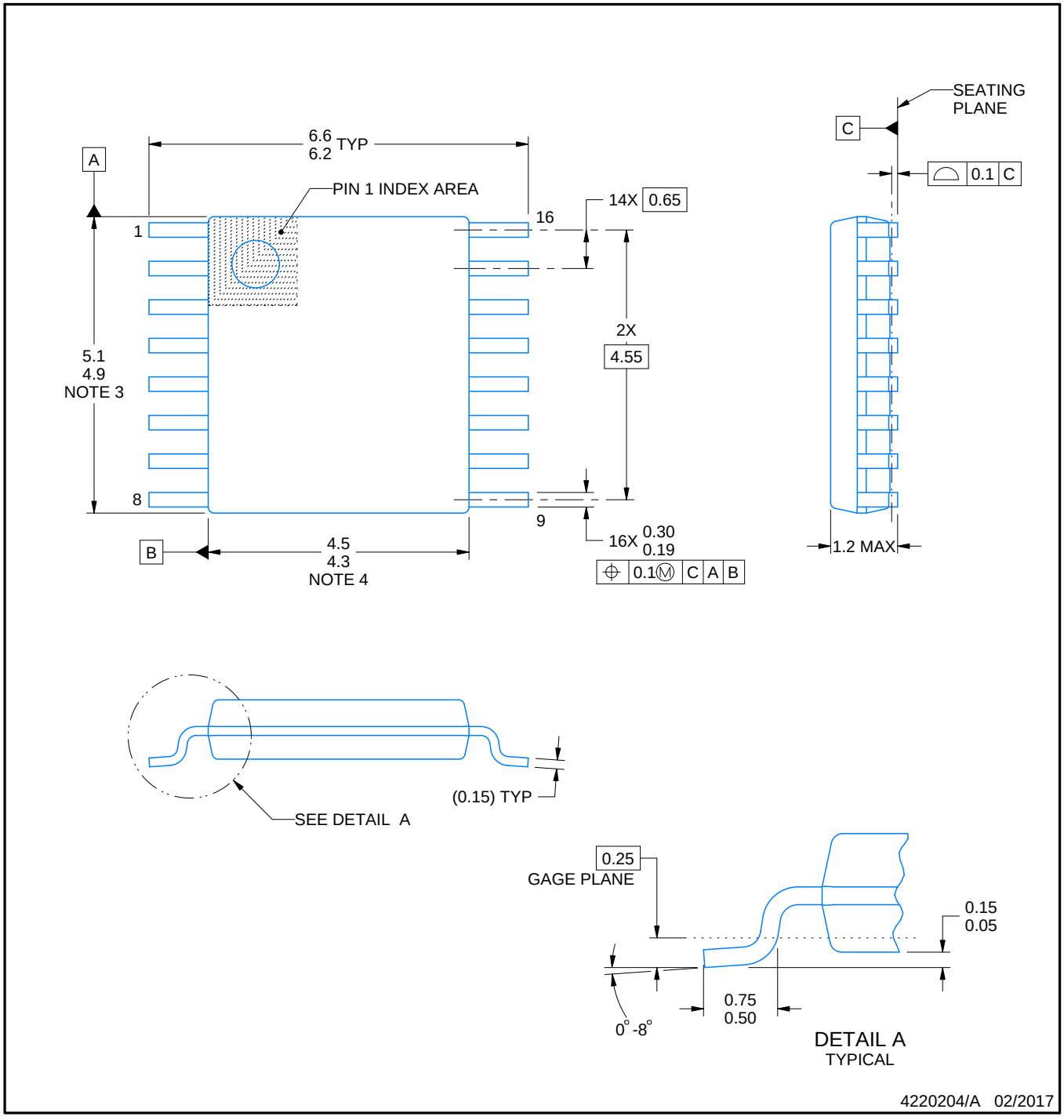
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

PW0016A

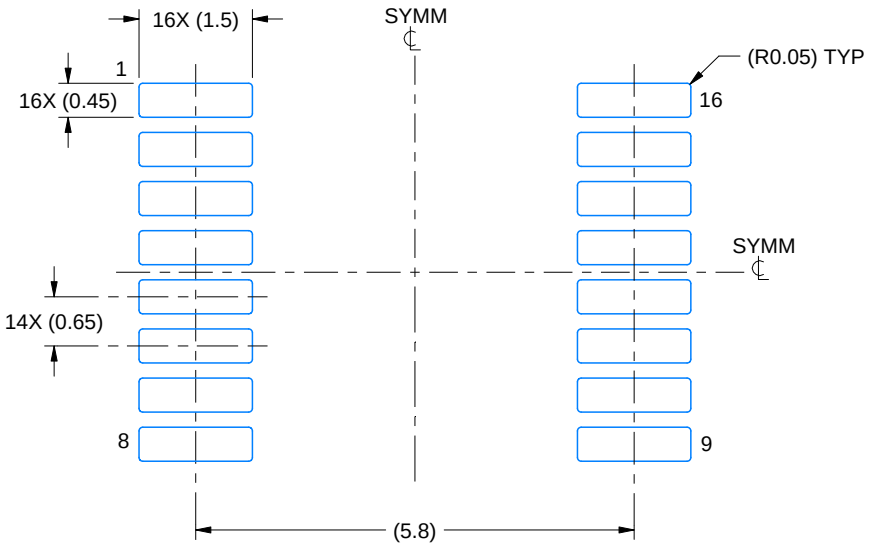
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

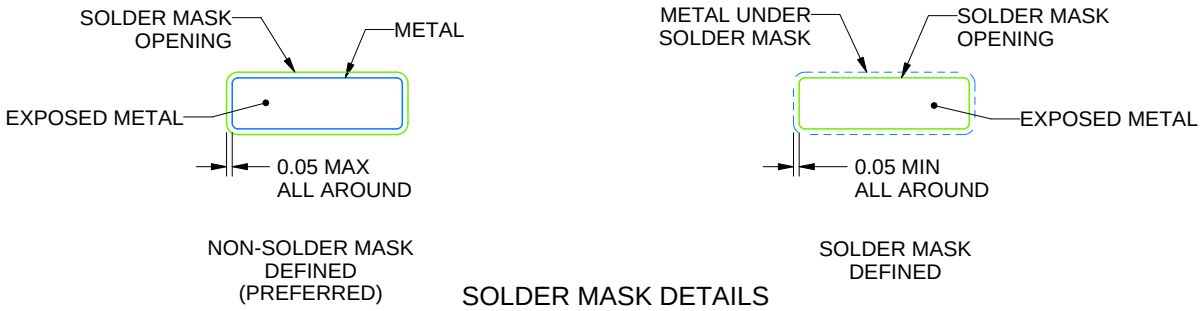


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

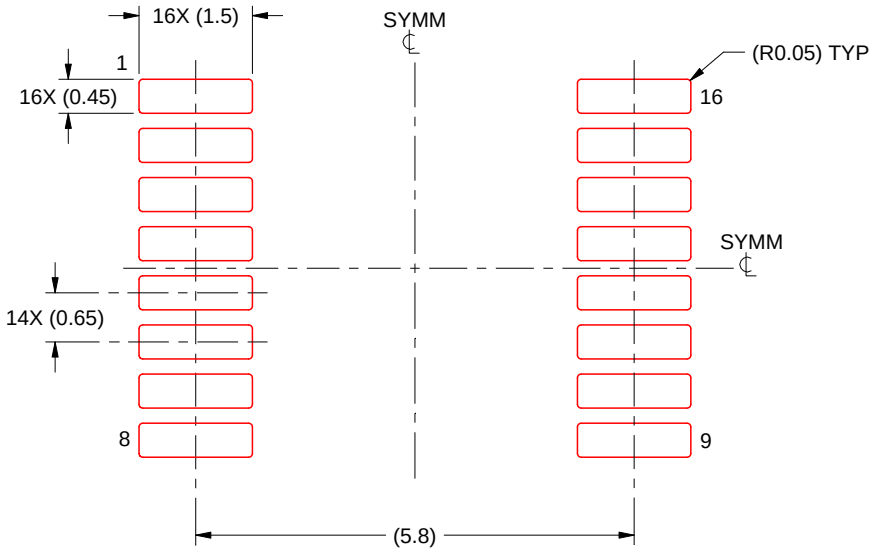


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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