- Very Low Dropout Voltage, Less Than 0.6 V at 750 mA
- Low Quiescent Current
- TTL- and CMOS-Compatible Enable on TL751M Series
- 60-V Load-Dump Protection
- Overvoltage Protection
- Internal Thermal Overload Protection
- Internal Overcurrent Limiting Circuitry

description

The TL750M and TL751M series are low-dropout positive voltage regulators specifically designed for battery-powered systems. The TL750M and TL751M incorporate on-board overvoltage and current-limit protection circuitry to protect the TL75xM devices and the regulated system. Both series are fully protected against 60-V load-dump and reverse battery conditions. Extremely low quiescent current, even during full-load conditions, makes the TL750M and TL751M series ideal for standby power systems.

The TL750M series of fixed-output voltage regulators offers 5-V, 8-V, 10-V, and 12-V options available in 3-lead KC (TO-220AB) and KTE plastic packages.

The TL751M series of fixed-output voltage regulators also offers 5-V, 8-V, 10-V, and 12-V options with the addition of an enable input. The enable input gives the designer complete control over power up, allowing sequential power up or emergency shutdown. When taken high, the enable input places the regulator output in a high-impedance state. The enable input is completely TTL- and CMOS-compatible. The TL751M series is offered in 5-lead KTG plastic packages.

The TL750MxxC and TL751MxxC are characterized for operation from 0°C to 125°C virtual junction temperature, and the TL750MxxQ and TL751MxxQ series are characterized for operation from –40°C to 125°C virtual junction temperature. The TL751M05M and TL751M12M are characterized for operation over the full military temperature range of –55°C to 125°C.

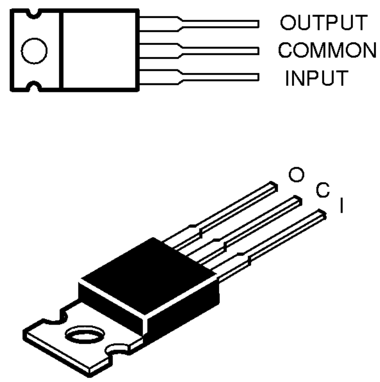
AVAILABLE OPTIONS

T_J	V_O TYP (V)	PACKAGED DEVICES						CHIP FORM (Y)
		CHIP CARRIER (FK)	CERAMIC DIP (JG)	HEAT-SINK MOUNTED (3-PIN) (KC)	PLASTIC FLANGE MOUNT (KTE)†	PLASTIC FLANGE MOUNT (KTG)†	PLASTIC FLANGE MOUNT (KTP)†	
0°C to 125°C	5	—	—	TL750M05CKC	TL750M05CKTE	TL751M05CKTG	TL750M05CKTP	TL750M05Y
	8	—	—	TL750M08CKC	TL750M08CKTE	TL751M08CKTG	TL750M08CKTP	TL750M08Y
	10	—	—	TL750M10CKC	TL750M10CKTE	TL751M10CKTG	TL750M10CKTP	TL750M10Y
	12	—	—	TL750M12CKC	TL750M12CKTE	TL751M12CKTG	TL750M12CKTP	TL750M12Y
–40°C to 125°C	5	—	—	TL750M05QKC	TL750M05QKTE	TL751M05QKTG	—	—
	8	—	—	TL750M08QKC	TL750M08QKTE	TL751M08QKTG	—	—
	10	—	—	TL750M10QKC	TL750M10QKTE	TL751M10QKTG	—	—
	12	—	—	TL750M12QKC	TL750M12QKTE	TL751M12QKTG	—	—
–55°C to 125°C	5	TL751M05MFK	TL751M05MJG	—	—	—	—	—
	12	TL751M12MFK	TL751M12MJG	—	—	—	—	—

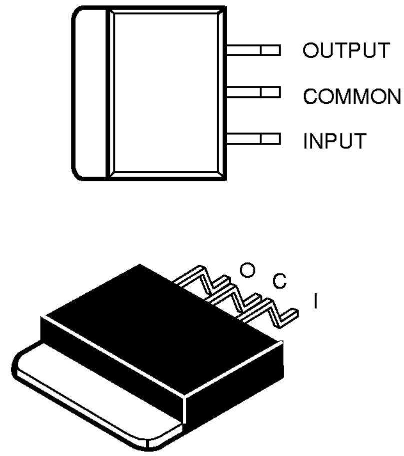
† The KTE and KTG packages also are available taped and reeled. The KTP is only available taped and reeled.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

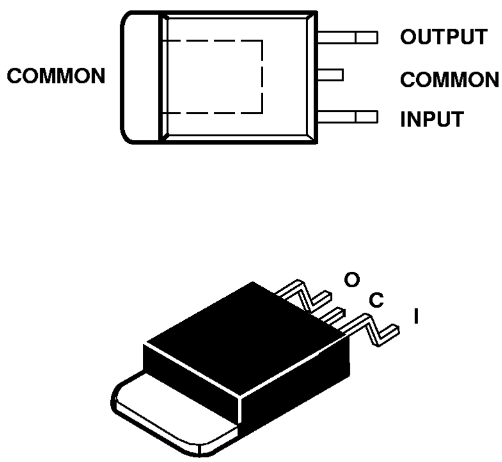
TL750M . . . 3-LEAD KC (TO-200AB) PACKAGE†
(TOP VIEW)



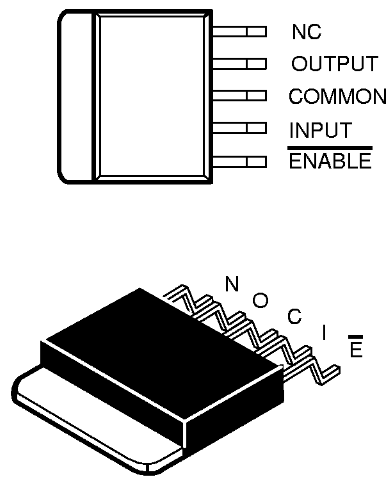
TL750M . . . 3-LEAD KTE PACKAGE†
(TOP VIEW)



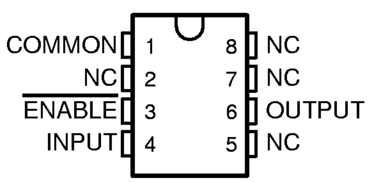
TL750M . . . KTP PACKAGE†
(TOP VIEW)



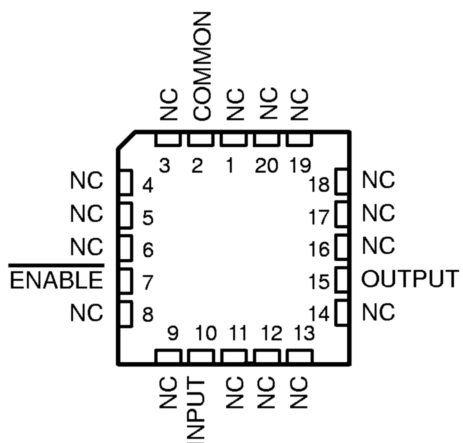
TL751M . . . 5-LEAD KTG PACKAGE†
(TOP VIEW)



TL751M . . . JG PACKAGE
(TOP VIEW)



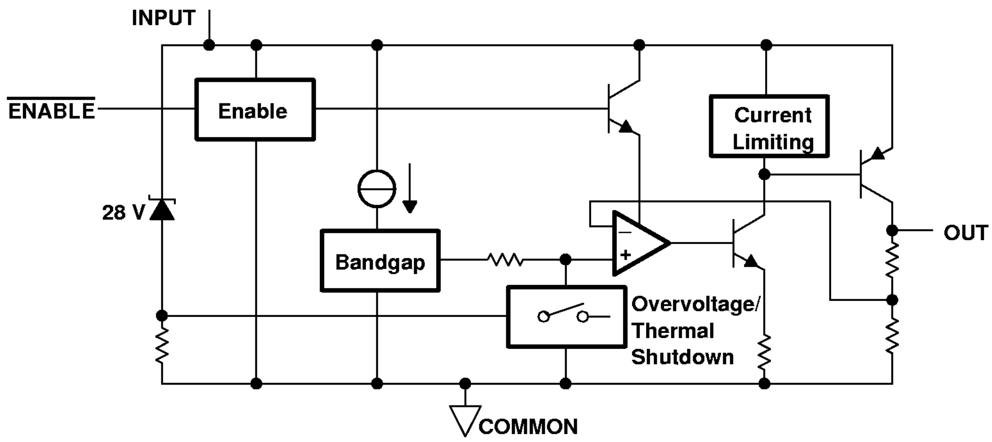
TL751M . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

† The common terminal is in electrical contact with the mounting base.

TL751Mxx functional block diagram

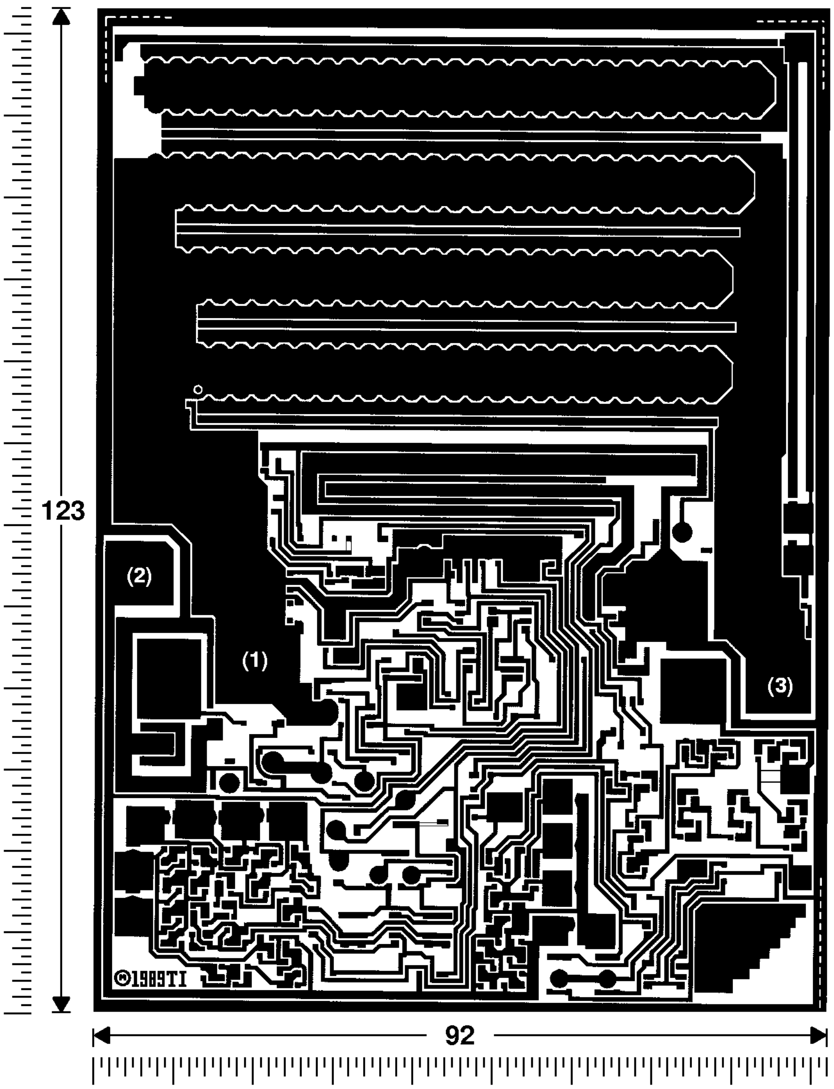


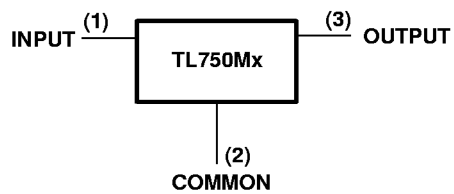
DEVICE COMPONENT COUNT	
Transistors	46
Diodes	14
Resistors	44
Capacitors	4
JFET	1
Tunnels (emitter R)	2

TL750MxxY chip information

This chip, when properly assembled, displays characteristics similar to the TL750MxxC. Thermal compression or ultrasonic bonding can be used on the doped-aluminum bonding pads. The chip can be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 11 MILS TYPICAL
BONDING PADS: 7 X 7 MILS MINIMUM
T_J(max) = 150°C
TOLERANCES ARE ±10%
ALL DIMENSIONS ARE IN MILS

absolute maximum ratings over virtual junction temperature range (unless otherwise noted)†

Continuous input voltage . . . . . 26 V
Transient input voltage (see Figure 5) . . . . . 60 V
Continuous reverse input voltage . . . . . –15 V
Transient reverse input voltage: t = 100 ms . . . . . –50 V
Continuous total power dissipation at (or below) T_A = 25°C . . . . . See Dissipation Rating Tables
Continuous total power dissipation at (or below) T_C = 40°C:
FK Package . . . . . 5.5 W
JG Package . . . . . 3.9 W
All other packages (see Note 1) . . . See Dissipation Rating Tables
Operating free-air (T_A) case (T_C) or virtual-junction (T_J) temperature range . . . . . –40°C to 150°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: For operation above T_A = 25°C and T_C = 40°C, refer to Figures 1 and 2. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variation in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

DISSIPATION RATING TABLE — FREE-AIR TEMPERATURE

PACKAGE	$T_A \leq$ 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 105°C POWER RATING	T_A = 125°C POWER RATING
FK	1920 mW	15.4 mW/°C	1227 mW	688 mW	380 mW
JG	1050 mW	8.4 mW/°C	672 mW	378 mW	210 mW
KC	2000 mW	16 mW/°C	1280 mW	720 mW	400 mW
KTE/KTG	1900 mW	15.2 mW/°C	1216 mW	684 mW	380 mW
KTP	1800 mW	14.5 mW/°C	1147 mW	653 mW	363 mW

DISSIPATION RATING TABLE — CASE TEMPERATURE

PACKAGE	$T_C \leq$ 90°C POWER RATING	DERATING FACTOR ABOVE T_C = 90°C	T_C = 125°C POWER RATING
KC	15000 mW	250 mW/°C	6250 mW
KTE/KTG	14300 mW	238 mW/°C	5970 mW
KTP	13000 mW	217 mW/°C	5417 mW

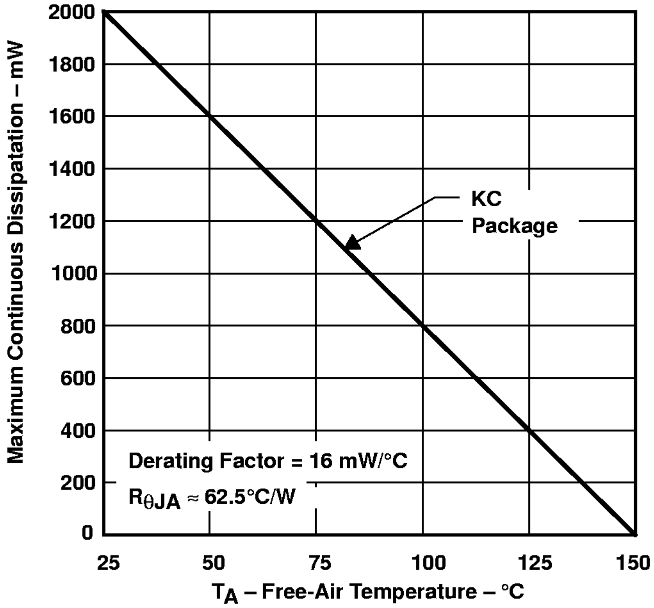


Figure 1

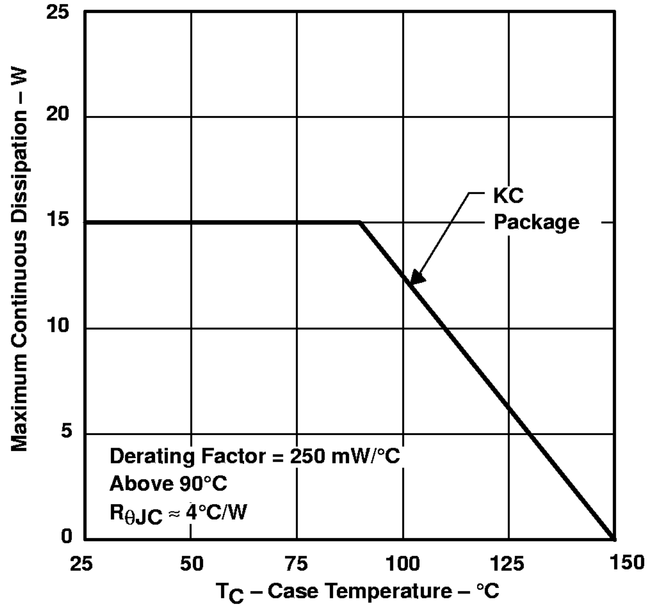


Figure 2

recommended operating conditions over recommended virtual junction temperature range

		MIN	MAX	UNIT
Input voltage range, V_I	TL75xM05	6	26	V
	TL75xM08	9	26	
	TL75xM10	11	26	
	TL75xM12	13	26	
High-level $\overline{\text{ENABLE}}$ input voltage, V_{IH}	TL751Mxx	2	15	V
Low-level $\overline{\text{ENABLE}}$ input voltage, V_{IL}	TL751Mxx	0	0.8	
Output current range, I_O	TL75xMxxC, TL75xMxxQ		750	mA
	TL751MxxM		480	mA
Operating virtual junction temperature range, T_J	TL75xMxxC	0	125	°C
	TL75xMxxQ	–40	125	
	TL75xMxxM	–55	125	

electrical characteristics, V_I = 14 V, I_O = 300 mA, T_J = 25°C

PARAMETER	TL751Mxxx MIN	TL751Mxxx TYP	TL751Mxxx MAX	UNIT
Response time, $\overline{\text{ENABLE}}$ to output		50		µs

electrical characteristics, V_I = 14 V, I_O = 300 mA, $\overline{ENABLE}$ at 0 V for TL751M05, T_J = 25°C (unless otherwise noted) (see Note 2)

PARAMETER	TEST CONDITIONS	TL750M05C, TL751M05C TL750M05Q, TL751M05Q			UNIT
		MIN	TYP	MAX	
Output voltage	T_J = 25°C	4.95	5	5.05	V
	T_J = MIN to MAX†	4.9		5.1	
Input voltage regulation	V_I = 9 V to 16 V, I_O = 250 mA		10	25	mV
	V_I = 6 V to 26 V, I_O = 250 mA		12	50	
Ripple rejection	V_I = 8 V to 18 V, f = 120 Hz	50	55		dB
Output voltage regulation	I_O = 5 mA to 750 mA		20	50	mV
Dropout voltage	I_O = 500 mA			0.5	V
	I_O = 750 mA			0.6	
Output noise voltage	f = 10 Hz to 100 kHz		500		µV
Bias current	I_O = 750 mA		60	75	mA
	I_O = 10 mA			5	
Bias current (TL751M05C and TL751M05Q only)	$\overline{ENABLE}$ $V_{IH} \geq 2$ V			200	µA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF tantalum capacitor on the output with equivalent series resistance within the guidelines shown in Figure 3.

electrical characteristics, V_I = 14 V, I_O = 300 mA, $\overline{ENABLE}$ at 0 V for TL751M08, T_J = 25°C (unless otherwise noted) (see Note 2)

PARAMETER	TEST CONDITIONS	TL750M08x, TL751M08x			UNIT
		MIN	TYP	MAX	
Output voltage	T_J = 25°C	7.92	8	8.08	V
	T_J = MIN to MAX†	7.84		8.16	
Input voltage regulation	V_I = 10 V to 17 V, I_O = 250 mA		12	40	mV
	V_I = 9 V to 26 V, I_O = 250 mA		15	68	
Ripple rejection	V_I = 11 V to 21 V, f = 120 Hz	50	55		dB
Output voltage regulation	I_O = 5 mA to 750 mA		24	80	mV
Dropout voltage	I_O = 500 mA			0.5	V
	I_O = 750 mA			0.6	
Output noise voltage	f = 10 Hz to 100 kHz		500		µV
Bias current	I_O = 750 mA		60	75	mA
	I_O = 10 mA			5	
Bias current (TL751Mxx only)	$\overline{ENABLE}$ $V_{IH} \geq 2$ V			200	µA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF tantalum capacitor on the output with equivalent series resistance within the guidelines shown in Figure 3.

electrical characteristics, V_I = 14 V, I_O = 300 mA, $\overline{\text{ENABLE}}$ at 0 V for TL751M10, T_J = 25°C (unless otherwise noted) (see Note 2)

PARAMETER	TEST CONDITIONS	TL750M10x, TL751M10x			UNIT
		MIN	TYP	MAX	
Output voltage	T_J = 25°C	9.9	10	10.1	V
	T_J = MIN to MAX†	9.8		10.2	
Input voltage regulation	V_I = 12 V to 18 V, I_O = 250 mA		15	43	mV
	V_I = 11 V to 26 V, I_O = 250 mA		20	75	
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz	50	55		dB
Output voltage regulation	I_O = 5 mA to 750 mA		30	100	mV
Dropout voltage	I_O = 500 mA			0.5	V
	I_O = 750 mA			0.6	
Output noise voltage	f = 10 Hz to 100 kHz		1000		µV
Bias current	I_O = 750 mA		60	75	mA
	I_O = 10 mA			5	
Bias current (TL751Mxx only)	$\overline{\text{ENABLE}}$ $V_{IH} \geq 2$ V			200	µA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF tantalum capacitor on the output with equivalent series resistance within the guidelines shown in Figure 3.

electrical characteristics, V_I = 14 V, I_O = 300 mA, $\overline{\text{ENABLE}}$ at 0 V for TL751M12, T_J = 25°C (unless otherwise noted) (see Note 2)

PARAMETER	TEST CONDITIONS	TL750M12C, TL751M12C TL750M12Q, TL751M12Q			UNIT
		MIN	TYP	MAX	
Output voltage	T_J = 25°C	11.88	12	12.12	V
	T_J = MIN to MAX†	11.76		12.24	
Input voltage regulation	V_I = 14 V to 19 V, I_O = 250 mA		15	43	mV
	V_I = 13 V to 26 V, I_O = 250 mA		20	78	
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz	50	55		dB
Output voltage regulation	I_O = 5 mA to 750 mA		30	120	mV
Dropout voltage	I_O = 500 mA			0.5	V
	I_O = 750 mA			0.6	
Output noise voltage	f = 10 Hz to 100 kHz		1000		µV
Bias current	I_O = 750 mA		60	75	mA
	I_O = 10 mA			5	
Bias current (TL751Mxx only)	$\overline{\text{ENABLE}}$ $V_{IH} \geq 2$ V			200	µA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF tantalum capacitor on the output with equivalent series resistance within the guidelines shown in Figure 3.

electrical characteristics, V_I = 14 V, I_O = 300 mA, $\overline{ENABLE}$ at 0 V, T_J = 25°C (unless otherwise noted) (see Note 2)

PARAMETER	TEST CONDITIONS			TL751M05M			UNIT
				MIN	TYP	MAX	
Output voltage	V_I = 6 V to 26 V,	I_O = 0 mA to 480 mA	T_J = 25°C	4.95	5	5.05	V
			T_J = −55°C to 125°C	4.9		5.1	
Input voltage regulation	V_I = 9 V to 16 V,	I_O = 250 mA			10	25	mV
	V_I = 6 V to 26 V,	I_O = 250 mA			12	50	
Ripple rejection	V_I = 8 V to 18 V,	f = 120 Hz		50*	55		dB
Output voltage regulation	I_O = 5 mA to 480 mA				20	50	mV
Dropout voltage	I_O = 480 mA					0.5	V
Output noise voltage	f = 10 Hz to 100 kHz				500		µV
Bias current	I_O = 480 mA				60	75	mA
	I_O = 10 mA					5	
	$\overline{ENABLE}$ V_{IH} ≥ 2 V					200	µA

* This parameter is not production tested.

NOTE 2: Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF tantalum capacitor on the output with equivalent series resistance within the guidelines shown in Figure 3.

electrical characteristics, V_I = 14 V, I_O = 300 mA, $\overline{ENABLE}$ at 0 V, T_J = 25°C (unless otherwise noted) (see Note 2)

PARAMETER	TEST CONDITIONS			TL751M12M			UNIT
				MIN	TYP	MAX	
Output voltage	V_I = 13 V to 26 V,	I_O = 0 mA to 480 mA	T_J = 25°C	11.88	12	12.12	V
			T_J = −55°C to 125°C	11.76		12.24	
Input voltage regulation	V_I = 14 V to 19 V,	I_O = 250 mA			15	43	mV
	V_I = 13 V to 26 V,	I_O = 250 mA			20	78	
Ripple rejection	V_I = 13 V to 23 V,	f = 120 Hz		50*	55		dB
Output voltage regulation	I_O = 5 mA to 480 mA				30	120	mV
Dropout voltage	I_O = 480 mA					0.5	V
Output noise voltage	f = 10 Hz to 100 kHz				1000		µV
Bias current	I_O = 480 mA				60	75	mA
	I_O = 10 mA					5	
	$\overline{ENABLE}$ V_{IH} ≥ 2 V					200	µA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF tantalum capacitor on the output with equivalent series resistance within the guidelines shown in Figure 3.

electrical characteristics, V_I = 14 V, I_O = 300 mA, $\overline{ENABLE}$ at 0 V, T_J = 25°C (unless otherwise noted) (see Note 2)

PARAMETER	TEST CONDITIONS		TL750M05Y			UNIT
			MIN	TYP	MAX	
Output voltage				5		V
Input voltage regulation	V_I = 9 V to 16 V,	I_O = 250 mA		10		mV
	V_I = 6 V to 26 V,	I_O = 250 mA		12		
Ripple rejection	V_I = 8 V to 18 V,	f = 120 Hz		55		dB
Output voltage regulation	I_O = 5 mA to 750 mA			20		mV
Output noise voltage	f = 10 Hz to 100 kHz			500		µV
Bias current	I_O = 750 mA			60		mA

NOTE 2: Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF tantalum capacitor on the output with equivalent series resistance within the guidelines shown in Figure 3.

electrical characteristics, V_I = 14 V, I_O = 300 mA, $\overline{ENABLE}$ at 0 V, T_J = 25°C (unless otherwise noted) (see Note 2)

PARAMETER	TEST CONDITIONS		TL750M08Y			UNIT
			MIN	TYP	MAX	
Output voltage				8		V
Input voltage regulation	V_I = 10 V to 17 V,	I_O = 250 mA		12		mV
	V_I = 9 V to 26 V,	I_O = 250 mA		15		
Ripple rejection	V_I = 11 V to 21 V,	f = 120 Hz		55		dB
Output voltage regulation	I_O = 5 mA to 750 mA			24		mV
Output noise voltage	f = 10 Hz to 100 kHz			500		µV
Bias current	I_O = 750 mA			60		mA

NOTE 2: Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF tantalum capacitor on the output with equivalent series resistance within the guidelines shown in Figure 3.

electrical characteristics, V_I = 14 V, I_O = 300 mA, $\overline{ENABLE}$ at 0 V, T_J = 25°C (unless otherwise noted) (see Note 2)

PARAMETER	TEST CONDITIONS		TL750M10Y			UNIT
			MIN	TYP	MAX	
Output voltage				10		V
Input voltage regulation	V_I = 12 V to 18 V,	I_O = 250 mA		15		mV
	V_I = 11 V to 26 V,	I_O = 250 mA		20		
Ripple rejection	V_I = 13 V to 23 V,	f = 120 Hz		55		dB
Output voltage regulation	I_O = 5 mA to 750 mA			30		mV
Output noise voltage	f = 10 Hz to 100 kHz			1000		µV
Bias current	I_O = 750 mA			60		mA

NOTE 2: Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF tantalum capacitor on the output with equivalent series resistance within the guidelines shown in Figure 3.

TL751M12Y electrical characteristics, V_I = 14 V, I_O = 300 mA, $\overline{\text{ENABLE}}$ at 0 V, T_J = 25°C (unless otherwise noted) (see Note 2)

PARAMETER	TEST CONDITIONS	TL750M12Y MIN	TL750M12Y TYP	TL750M12Y MAX	UNIT
Output voltage			12		V
Input voltage regulation	V_I = 14 V to 19 V, I_O = 250 mA		15		mV
	V_I = 13 V to 26 V, I_O = 250 mA		20		
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz		55		dB
Output voltage regulation	I_O = 5 mA to 750 mA		30		mV
Output noise voltage	f = 10 Hz to 100 kHz		1000		µV
Bias current	I_O = 750 mA		60		mA

NOTE 2: Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF tantalum capacitor on the output with equivalent series resistance within the guidelines shown in Figure 3.

PARAMETER MEASUREMENT INFORMATION

The TL751Mxx is a low-dropout regulator. This means that the capacitance loading is important to the performance of the regulator because it is a vital part of the control loop. The capacitor value and the equivalent series resistance (ESR) both affect the control loop and must be defined for the load range and the temperature range. Figures 3 and 4 can establish the capacitance value and ESR range for the best regulator performance.

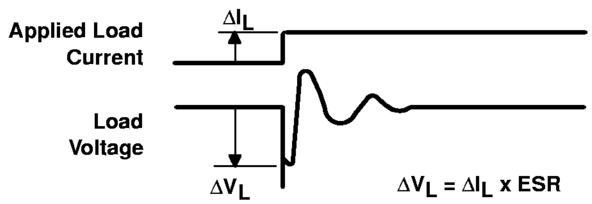
Figure 3 shows the recommended range of ESR for a given load with a 10-µF capacitor on the output. This figure also shows a maximum ESR limit of 2 Ω and a load-dependent minimum ESR limit.

For applications with varying loads, the lightest load condition should be chosen since it is the worst case. Figure 4 shows the relationship of the reciprocal of ESR to the square root of the capacitance with a minimum capacitance limit of 10 µF and a maximum ESR limit of 2 Ω. This figure establishes the amount that the minimum ESR limit shown in Figure 3 can be adjusted for different capacitor values. For example, where the minimum load needed is 200 mA, Figure 4 suggests an ESR range of 0.8 Ω to 2 Ω for 10 µF. Figure 4 shows that changing the capacitor from 10 µF to 400 µF can change the ESR minimum by greater than 3/0.5 (or 6). Therefore, the new minimum ESR value is 0.8/6 (or 0.13 Ω). This now allows an ESR range of 0.13 Ω to 2 Ω , achieving an expanded ESR range by using a larger capacitor at the output. For better stability in low-current applications, a small resistance placed in series with the capacitor (see Table 1) is recommended, so that ESRs better approximate those shown in Figures 3 and 4.

PARAMETER MEASUREMENT INFORMATION

Table 1. Compensation for Increased Stability at Low Currents

MANUFACTURER	CAPACITANCE	ESR TYP	PART NUMBER	ADDITIONAL RESISTANCE
AVX	15 µF	0.9 Ω	TAJB156M010S	1 Ω
KEMET	33 µF	0.6 Ω	T491D336M010AS	0.5 Ω



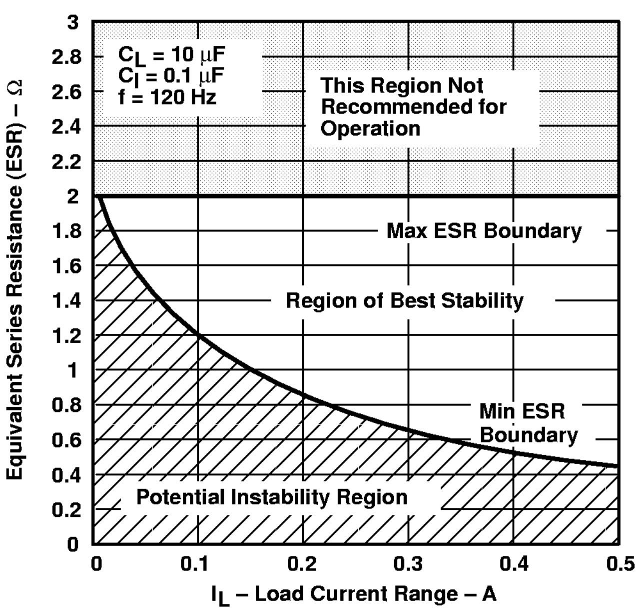


Figure 3

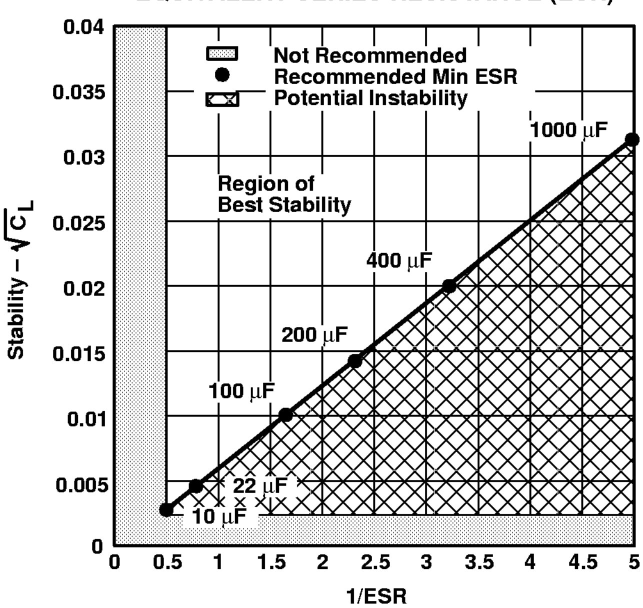


Figure 4

TYPICAL CHARACTERISTICS

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Load transient response		11
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TRANSIENT INPUT VOLTAGE vs TIME

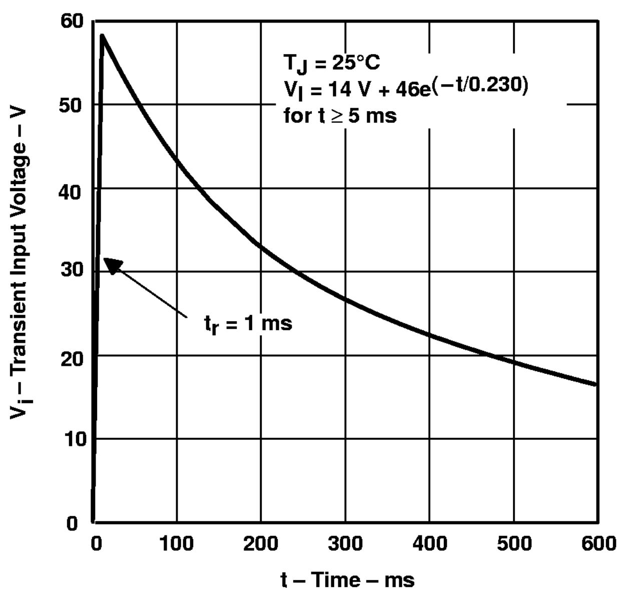

Figure 5

OUTPUT VOLTAGE vs INPUT VOLTAGE

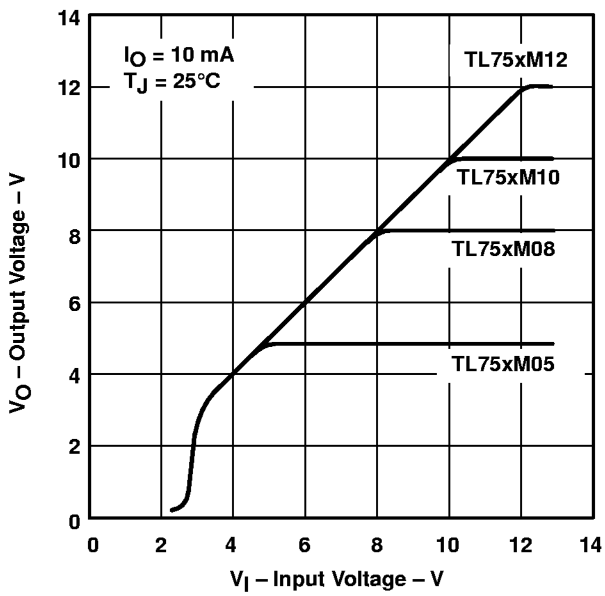

Figure 6

TYPICAL CHARACTERISTICS

INPUT CURRENT vs INPUT VOLTAGE

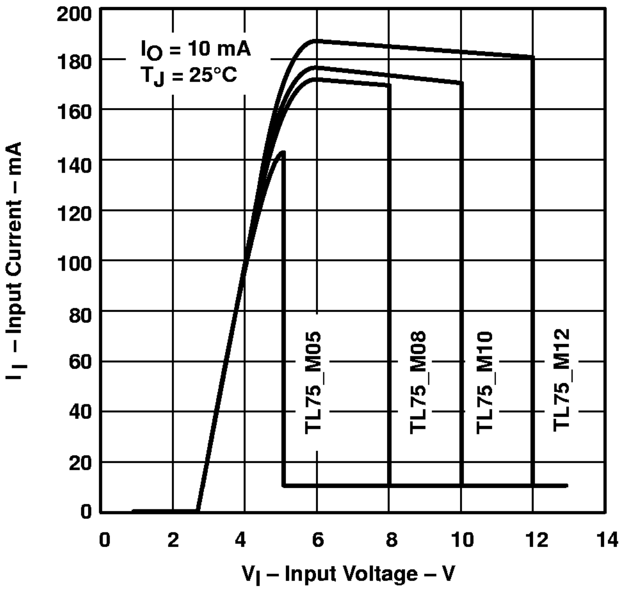

Figure 7

INPUT CURRENT vs INPUT VOLTAGE

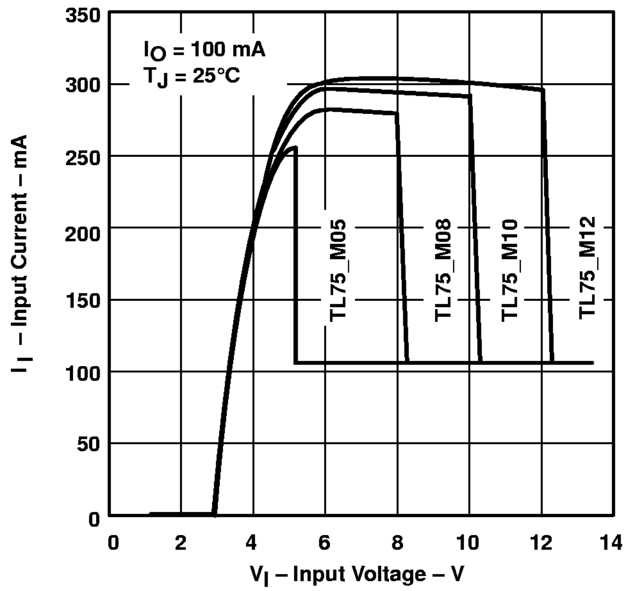

Figure 8

DROPOUT VOLTAGE vs OUTPUT CURRENT

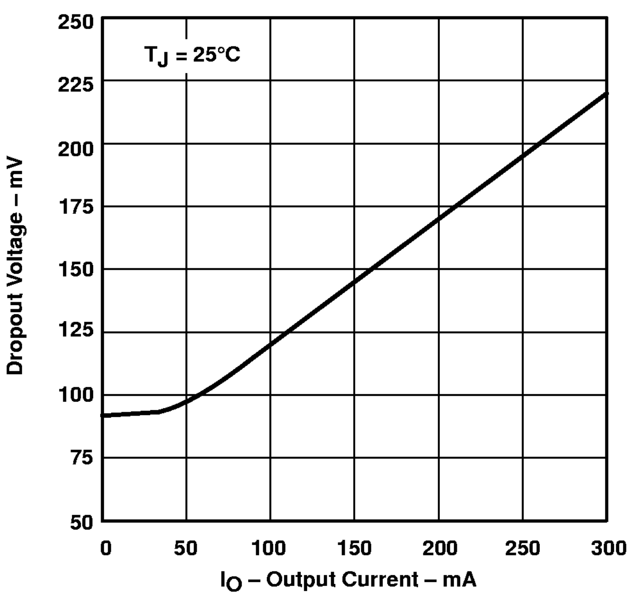

Figure 9

QUIESCENT CURRENT vs OUTPUT CURRENT

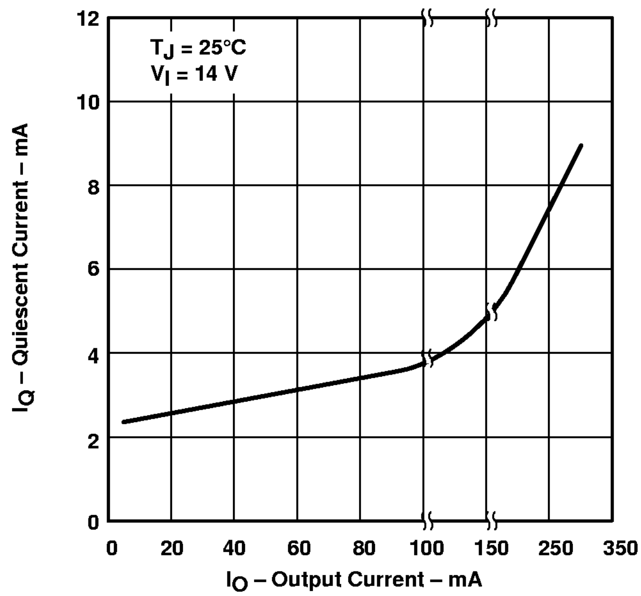

Figure 10

TYPICAL CHARACTERISTICS

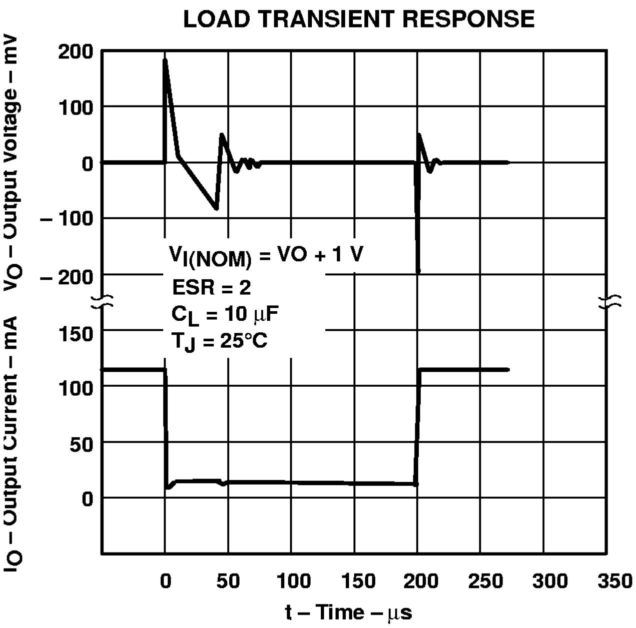

Figure 11

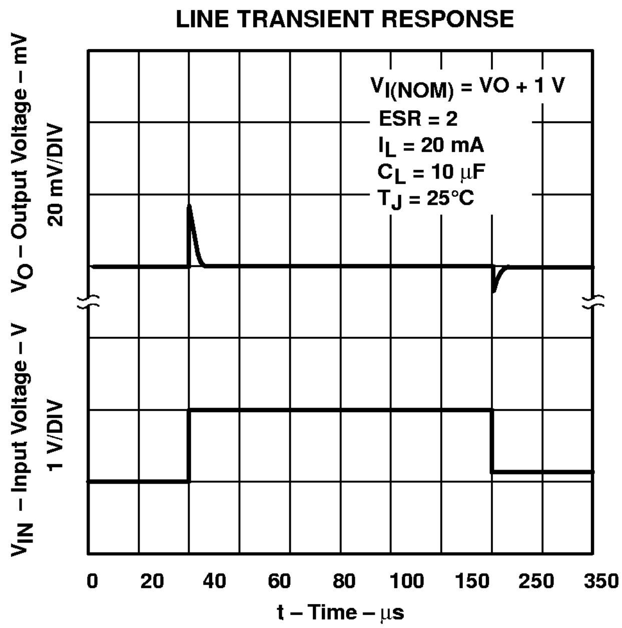

Figure 12