

TMS45165, TMS45165P

262144-WORD BY 16-BIT HIGH-SPEED DYNAMIC RANDOM-ACCESS MEMORIES

SMHS165C - OCTOBER 1992 - REVISED JUNE 1995

This data sheet is applicable to all TMS45165/Ps symbolized with Revision "B" and subsequent revisions as described on page 4-134.

- Organization . . . 262144 x 16
- Single 5-V Supply ($\pm 10\%$ Tolerance)
- Performance Ranges:

	ACCESS TIME	ACCESS TIME	ACCESS TIME	READ OR WRITE CYCLE MIN
	t _{RAC} MAX	t _{CAC} MAX	t _{AA} MAX	
'45165/P-70	70 ns	20 ns	35 ns	130 ns
'45165/P-80	80 ns	20 ns	40 ns	150 ns
'45165/P-10	100 ns	25 ns	45 ns	180 ns

- Enhanced Page Mode Operation With CAS-Before-RAS (CBR) Refresh
- Long Refresh Period
512-Cycle Refresh in 8 ms (Max)
64 ms for Low Power With Self-Refresh Version (TMS45165P)
- 3-State Unlatched Output
- Lower Power Dissipation
- Texas Instruments EPIC™ CMOS Process
- All Inputs, Outputs and Clocks are TTL Compatible
- High-Reliability Plastic 40-Lead 400-Mil-Wide Surface Mount (SOJ) Package, and 40/44-Lead Thin Small Outline Package (TSOP)
- Operating Free-Air Temperature Range 0°C to 70°C
- Low-Power With Self-Refresh
- Upper and Lower Byte Control During Write Operations

DZ PACKAGE (TOP VIEW)

VCC	1	40	VSS
DQ0	2	39	DQ15
DQ1	3	38	DQ14
DQ2	4	37	DQ13
DQ3	5	36	DQ12
VCC	6	35	VSS
DQ4	7	34	DQ11
DQ5	8	33	DQ10
DQ6	9	32	DQ9
DQ7	10	31	DQ8
NC	11	30	NC
LW	12	29	NC
UW	13	28	CAS
RAS	14	27	OE
NC	15	26	A8
A0	16	25	A7
A1	17	24	A6
A2	18	23	A5
A3	19	22	A4
VCC	20	21	VSS

DGE PACKAGE (TOP VIEW)

VCC	1	44	VSS
DQ0	2	43	DQ15
DQ1	3	42	DQ14
DQ2	4	41	DQ13
DQ3	5	40	DQ12
VCC	6	39	VSS
DQ4	7	38	DQ11
DQ5	8	37	DQ10
DQ6	9	36	DQ9
DQ7	10	35	DQ8
NC	13	32	NC
LW	14	31	NC
UW	15	30	CAS
RAS	16	29	OE
NC	17	28	A8
A0	18	27	A7
A1	19	26	A6
A2	20	25	A5
A3	21	24	A4
VCC	22	23	VSS

PIN NOMENCLATURE

A0-A8	Address Inputs
CAS	Column Address Strobe
DQ0-DQ15	Data In/Data Out
LW	Lower Write Enable
NC	No Internal Connection
OE	Output Enable
RAS	Row Address Strobe
UW	Upper Write Enable
VCC	5-V Supply
VSS	Ground

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description

The TMS45165 series are high-speed, 4194304-bit dynamic random access memories organized as 262144 words of sixteen bits each.

The TMS45165P series are high-speed, low-power with self-refresh, 4194304-bit dynamic random-access memories organized as 262144 words by sixteen bits each.

They employ state-of-the-art enhanced performance implanted CMOS (EPIC™) technology for high performance, reliability, and low power at low cost. These devices feature maximum RAS access times of 70 ns, 80 ns, and 100 ns. Maximum power dissipation is as low as 660 mW operating and 11 mW standby on 100 ns devices.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

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262 144-WORD BY 16-BIT HIGH-SPEED
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description (continued)

The TMS45165 and TMS45165P are each offered in a 40-lead plastic surface mount SOJ (DZ suffix) package, and a 40/44-lead plastic surface mount TSOP (DGE suffix). These packages are characterized for operation from 0°C to 70°C.

operation

enhanced page mode

Page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that can be accessed is determined by the maximum $\overline{\text{RAS}}$ low time and the $\overline{\text{CAS}}$ page-mode cycle time used. With minimum $\overline{\text{CAS}}$ page cycle time, all 512 columns specified by column addresses A0 through A8 can be accessed without intervening $\overline{\text{RAS}}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in these devices are activated on the falling edge of $\overline{\text{RAS}}$. The buffers act as transparent or flow-through latches while $\overline{\text{CAS}}$ is high. The falling edge of $\overline{\text{CAS}}$ latches the column addresses. This feature allows the TMS45165 and TMS45165P to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{\text{CAS}}$ transitions low. This performance improvement is referred to as enhanced page mode. Valid column address can be presented immediately after t_{RAH} (row address hold time) has been satisfied, usually well in advance of the falling edge of $\overline{\text{CAS}}$. In this case, data is obtained after $t_{\text{CAC max}}$ (access time from $\overline{\text{CAS}}$ low) if $t_{\text{AA max}}$ (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{\text{CAS}}$ goes high, access time for the next cycle is determined by the later occurrence of t_{CAC} or t_{CPA} (access time from rising edge of the last $\overline{\text{CAS}}$).

address (A0-A8)

Eighteen address bits are required to decode 1 of 262 144 storage cell locations. Nine row-address bits are set up on pins A0 through A8 and latched onto the chip by the row-address strobe ($\overline{\text{RAS}}$). Then nine column-address bits are set up on pins A0 through A8 and latched onto the chip by the column-address strobe ($\overline{\text{CAS}}$). All addresses must be stable on or before the falling edge of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$. $\overline{\text{RAS}}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. In the TMS45165 and TMS45165P $\overline{\text{CAS}}$ is used as a chip select activating the output buffer, as well as latching the address bits into the column-address buffers.

write enable ($\overline{\text{UW}}$, $\overline{\text{LW}}$)

The read or write mode is selected through the upper or lower write-enable ($\overline{\text{UW}}$, $\overline{\text{LW}}$) input. $\overline{\text{LW}}$ controls DQ0-DQ7, and $\overline{\text{UW}}$ controls DQ8-DQ15. A logic high on the $\overline{\text{UW}}$ and $\overline{\text{LW}}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from the standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{\text{UW}}$ or $\overline{\text{LW}}$ goes low prior to $\overline{\text{CAS}}$ (early write), data out remains in the high-impedance state for the entire cycle permitting a write operation with $\overline{\text{OE}}$ grounded.

NOTE: Either $\overline{\text{UW}}$ or $\overline{\text{LW}}$ can be brought low in a given write cycle and only eight data bits are written into. The user can bring both $\overline{\text{UW}}$ and $\overline{\text{LW}}$ low at the same time and all 16 data bits are written into.

data In (DQ0-DQ15)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{\text{CAS}}$, $\overline{\text{UW}}$, or $\overline{\text{LW}}$ strobes data into the on-chip data latch. In an early write cycle, $\overline{\text{UW}}$ or $\overline{\text{LW}}$ is brought low prior to $\overline{\text{CAS}}$ and the data is strobed in by $\overline{\text{CAS}}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{\text{CAS}}$ is already low, the data is strobed in by $\overline{\text{UW}}$ or $\overline{\text{LW}}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{\text{OE}}$ must be high to bring the output buffers to high-impedance prior to impressing data on the I/O lines. The $\overline{\text{LW}}$ pin controls DQ0-DQ7. The $\overline{\text{UW}}$ pin controls DQ8-DQ15.

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data out (DQ0-DQ15)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{\text{CAS}}$ and $\overline{\text{OE}}$ are brought low. In a read cycle the output becomes valid after the access time interval t_{CAC} that begins with the negative transition of $\overline{\text{CAS}}$ as long as t_{RAC} and t_{AA} are satisfied.

output enable ($\overline{\text{OE}}$)

$\overline{\text{OE}}$ controls the impedance of the output buffers. When $\overline{\text{OE}}$ is high, the buffers remain in the high-impedance state. Bringing $\overline{\text{OE}}$ low during a normal cycle activates the output buffers, putting them in the low-impedance state. It is necessary for both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ to be brought low for the output buffers to go into the low-impedance state, they remain in the low-impedance state until either $\overline{\text{OE}}$ or $\overline{\text{CAS}}$ is brought high.

$\overline{\text{RAS}}$ -only refresh

A refresh operation must be performed at least once every eight milliseconds (64 ms for TMS45165P) to retain data. This can be achieved by strobing each of the 512 rows (A0-A8). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{\text{RAS}}$ -only operation can be used by holding $\overline{\text{CAS}}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{\text{RAS}}$ -only refresh.

hidden refresh

Hidden refresh can be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{\text{CAS}}$ at V_{IL} after a read operation and cycling $\overline{\text{RAS}}$ after a specified precharge period, similar to a $\overline{\text{RAS}}$ -only refresh cycle.

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh (CBR)

CBR refresh is utilized by bringing $\overline{\text{CAS}}$ low earlier than $\overline{\text{RAS}}$ (see parameter t_{CSR}) and holding it low after $\overline{\text{RAS}}$ falls (see parameter t_{CHR}). For successive CBR refresh cycles, $\overline{\text{CAS}}$ can remain low while cycling $\overline{\text{RAS}}$. The external address is ignored and the refresh address is generated internally.

A low-power battery-backup refresh mode that requires less than 300 μA refresh current is available on the TMS45165P. Data integrity is maintained using CBR refresh with a period of 125 μs holding $\overline{\text{RAS}}$ low for less than 1 μs . To minimize current consumption, all input levels must be at CMOS levels ($V_{\text{IL}} \leq 0.2 \text{ V}$, $V_{\text{IH}} \geq V_{\text{CC}} - 0.2 \text{ V}$).

self-refresh (TMS45165P)

The self-refresh mode is entered by dropping $\overline{\text{CAS}}$ low prior to $\overline{\text{RAS}}$ going low. Then $\overline{\text{CAS}}$ and $\overline{\text{RAS}}$ are both held low for a minimum of 100 μs . The chip is then refreshed internally by an on-board oscillator. No external address is required since the CBR counter is used to keep track of the address. To exit the self-refresh mode, both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are brought high to satisfy t_{CHS} .

power up

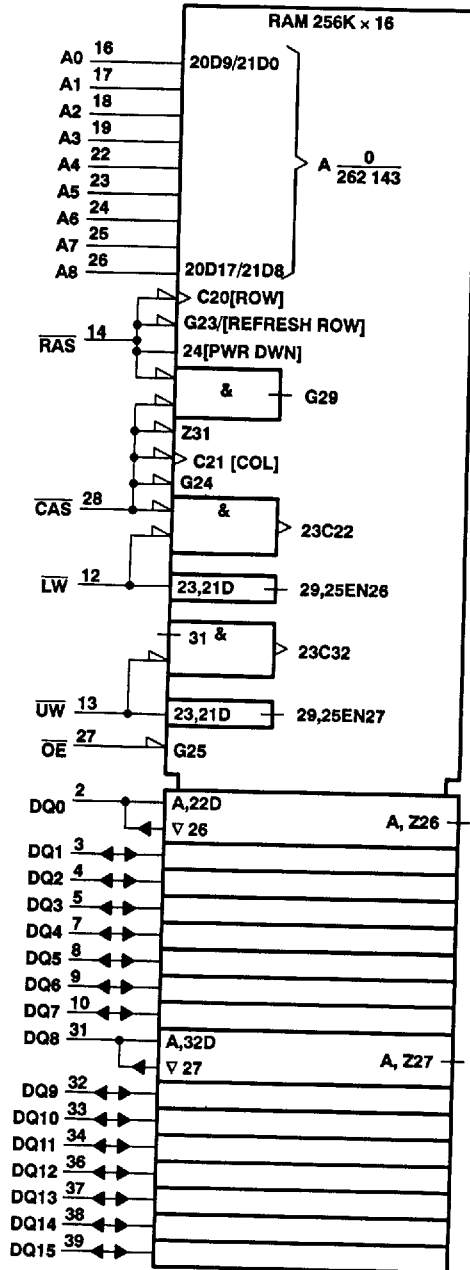
To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight $\overline{\text{RAS}}$ cycles is required after power-up to the full V_{CC} level.

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logic symbol†

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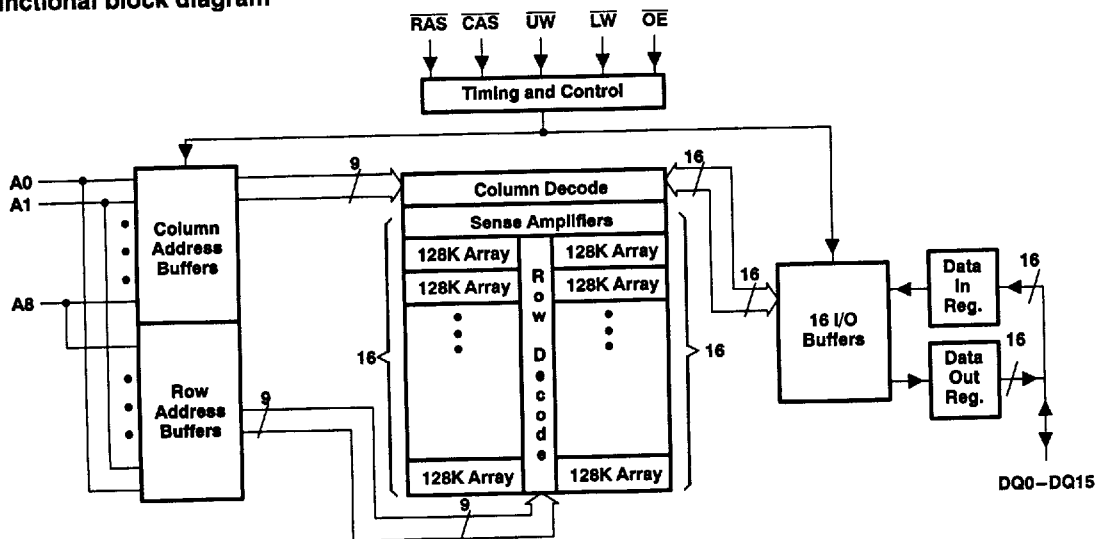


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown correspond to the DZ package.



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functional block diagram



- absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**
- Supply voltage range on any pin (see Note 1) - 1 V to 7 V
 - Supply voltage range on V_{CC} - 1 V to 7 V
 - Short-circuit output current 50 mA
 - Power dissipation 1 W
 - Operating free-air temperature range 0°C to 70°C
 - Storage temperature range, T_{stg} - 55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

	MIN	NOM	MAX	UNIT
V _{CC} Supply voltage	4.5	5	5.5	V
V _{SS} Supply voltage		0		V
V _{IH} High-level input voltage			6.5	V
V _{IL} Low-level input voltage (see Note 2)	-1		0.8	V
T _A Operating free-air temperature			70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

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PARAMETER	TEST CONDITIONS	'45165-70 '45165P-70		'45165-80 '45165P-80		'45165-10 '45165P-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
		V_{OH}	High-level output voltage	$I_{OH} = -5 \text{ mA}$		2.4		
V_{OL}	Low-level output voltage	$I_{OL} = 4.2 \text{ mA}$		0.4		0.4		V
I_I	Input current (leakage)	$V_{CC} = 5.5 \text{ V}$, $V_I = 0 \text{ V to } 6.5 \text{ V}$, All other pins = $0 \text{ V to } V_{CC}$		± 10		± 10		μA
I_O	Output current (leakage)	$V_{CC} = 5.5 \text{ V}$, $V_O = 0 \text{ V to } V_{CC}$, CAS high		± 10		± 10		μA
I_{CC1}^\dagger	Read or write cycle current (see Note 3)	$V_{CC} = 5.5 \text{ V}$, Minimum cycle		160		140		mA
I_{CC2}	Standby current	$V_{IH} = 2.4 \text{ V (TTL)}$ After 1 memory cycle, RAS and CAS high		2		2		mA
		$V_{IH} = V_{CC} - 0.2 \text{ V (CMOS)}$ After 1 memory cycle, RAS and CAS high	'45165	1		1		mA
			'45165P	200		200		μA
I_{CC3}	Average refresh current (RAS only or CBR) (see Note 3)	$V_{CC} = 5.5 \text{ V}$, Minimum cycle, (RAS only), RAS cycling, CAS high (CBR only) RAS low after CAS low		160		140		mA
I_{CC4}^\dagger	Average page current (see Note 4)	$V_{CC} = 5.5 \text{ V}$, $t_{PC} = \text{minimum}$, RAS low, CAS cycling		160		140		mA
I_{CC5}^\ddagger	Battery backup operating current (equivalent refresh time is 64 ms) (CBR only)	$t_{RC} = 125 \mu\text{s}$, $t_{RAS} \leq 1 \mu\text{s}$, $V_{CC} - 0.2 \text{ V} \leq V_{IH} \leq 6.5 \text{ V}$, $0 \text{ V} \leq V_{IL} \leq 0.2 \text{ V}$, \overline{UW} , \overline{LW} and $\overline{OE} = V_{IH}$, Address and data stable		300		300		μA
$I_{CC6}^{\dagger\ddagger}$	Self refresh current	CAS < 0.2 V, RAS < 0.2 V, Measured after t_{RASS} minimum		200		200		μA

† Measured with outputs open

‡ For TMS45165P only

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS} = V_{IL}$

4. Measured with a maximum of one address change while $\overline{CAS} = V_{IH}$

capacitance over recommended ranges of supply voltage and operating free-air temperature, $f = 1 \text{ MHz}$ (see Note 5)

PARAMETER	MIN	MAX	UNIT
$C_{i(A)}$ Input capacitance, A0-A8		5	pF
$C_{i(OE)}$ Input capacitance, \overline{OE}		7	pF
$C_{i(RC)}$ Input capacitance, CAS and RAS		7	pF
$C_{i(W)}$ Input capacitance, \overline{W}		7	pF
C_O Output capacitance		7	pF

NOTE 5: $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ and the bias on pins under test is 0 V.



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switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	'45165-70 '46165P-70		'45165-80 '46165P-80		'45165-10 '46165P-10		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
t _{CAC} Access time from $\overline{\text{CAS}}$ low		20		20		25	ns
t _{AA} Access time from column address		35		40		45	ns
t _{RAC} Access time from $\overline{\text{RAS}}$ low		70		80		100	ns
t _{OEA} Access time from $\overline{\text{OE}}$ low		20		20		25	ns
t _{CPA} Access time from column precharge		40		45		50	ns
t _{CLZ} $\overline{\text{CAS}}$ low to output in the low-impedance state	0		0		0		ns
t _{OFF} Output disable time after $\overline{\text{CAS}}$ high (see Note 6)	0	20	0	20	0	25	ns
t _{OEZ} Output disable time after $\overline{\text{OE}}$ high (see Note 6)	0	20	0	20	0	25	ns

NOTE 6: t_{OFF} and t_{OEZ} are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 7)

PARAMETER	'45165-70 '45165P-70		'45165-80 '45165P-80		'45165-10 '45165P-10		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
t _{RC} Cycle time, read (see Note 8)	130		150		180		ns
t _{WC} Cycle time, write	130		150		180		ns
t _{RWC} Cycle time, read-modify-write	185		205		245		ns
t _{PC} Cycle time, page-mode read or write (see Note 9)	45		50		55		ns
t _{PRWC} Cycle time, page-mode read-modify-write	90		105		120		ns
t _{RASP} Pulse duration, page mode, $\overline{\text{RAS}}$ low (see Note 11)	70	100 000	80	100 000	100	100 000	ns
t _{RAS} Pulse duration, nonpage mode, $\overline{\text{RAS}}$ low (see Note 11)	70	10 000	80	10 000	100	10 000	ns
t _{CAS} Pulse duration, $\overline{\text{CAS}}$ low (see Note 10)	20	10 000	20	10 000	25	10 000	ns
t _{CP} Pulse duration, $\overline{\text{CAS}}$ high	10		10		10		ns
t _{RP} Pulse duration, $\overline{\text{RAS}}$ high (precharge)	50		60		70		ns
t _{WP} Pulse duration, write	15		15		20		ns
t _{ASC} Setup time, column address before $\overline{\text{CAS}}$ low	0		0		0		ns
t _{ASR} Setup time, row address before $\overline{\text{RAS}}$ low	0		0		0		ns
t _{DS} Setup time, data before xW low (see Note 12)	0		0		0		ns
t _{RCS} Setup time, read before $\overline{\text{CAS}}$ low	0		0		0		ns
t _{CWL} Setup time, xW low before $\overline{\text{CAS}}$ high	20		20		25		ns
t _{RWL} Setup time, xW low before $\overline{\text{RAS}}$ high	20		20		25		ns
t _{WCS} Setup time, xW low before $\overline{\text{CAS}}$ low (early-write operation only)	0		0		0		ns

- NOTES: 7. Timing measurements are referenced to V_{IL} max and V_{IH} min.
 8. All cycle times assume t_r = 5 ns.
 9. t_{PC} > t_{CP} min + t_{CAS} min + 2t_r.
 10. In a read-modify-write cycle, t_{CWD} and t_{CWL} must be observed. Depending on the user's transition times, this can require additional $\overline{\text{CAS}}$ low time (t_{CAS}).
 11. In a read-modify-write cycle, t_{RWD} and t_{RWL} must be observed. Depending on the user's transition times, this can require additional $\overline{\text{RAS}}$ low time (t_{RAS}).
 12. Later of $\overline{\text{CAS}}$ or xW in write operations

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 7) (concluded)

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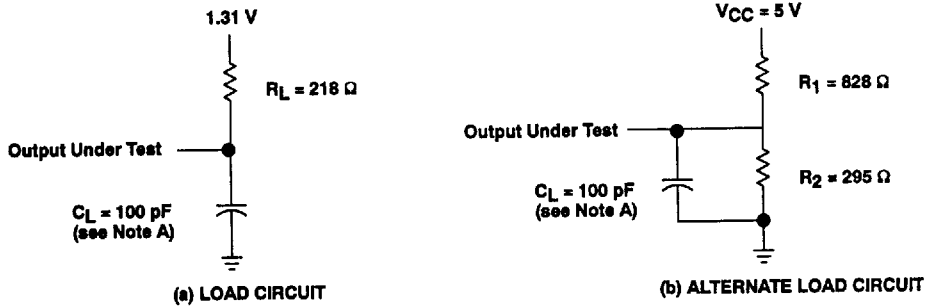
PARAMETER		'45165-70 '45165P-70		'45165-80 '45165P-80		'45165-10 '45165P-10		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _{CAH}	Hold time, column address after $\overline{\text{CAS}}$ low (see Note 12)	15		15		20		ns
t _{DHR}	Hold time, data after $\overline{\text{RAS}}$ low (see Note 13)	35		35		45		ns
t _{DH}	Hold time, data after $\overline{\text{CAS}}$ low (see Note 12)	15		15		20		ns
t _{AR}	Hold time, column address after $\overline{\text{RAS}}$ low (see Note 13)	35		35		45		ns
t _{RAH}	Hold time, row address after $\overline{\text{RAS}}$ low	10		10		15		ns
t _{RCH}	Hold time, read after $\overline{\text{CAS}}$ high (see Note 14)	0		0		0		ns
t _{RRH}	Hold time, read after $\overline{\text{RAS}}$ high (see Note 14)	0		0		0		ns
t _{WCH}	Hold time, write after $\overline{\text{CAS}}$ low (early-write operation only)	15		15		20		ns
t _{WCR}	Hold time, write after $\overline{\text{RAS}}$ low (see Note 13)	35		35		45		ns
t _{OEH}	Hold time, $\overline{\text{OE}}$ command	20		20		25		ns
t _{AWD}	Delay time, column address to $\overline{\text{xW}}$ low (see Note 15)	65		70		80		ns
t _{CHR}	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ high (CBR refresh only)	15		20		20		ns
t _{CRP}	Delay time, $\overline{\text{CAS}}$ high to $\overline{\text{RAS}}$ low	0		0		0		ns
t _{CSH}	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ high	70		80		100		ns
t _{CSR}	Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{RAS}}$ low (CBR refresh only)	10		10		10		ns
t _{CWD}	Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{xW}}$ low (see Note 16)	50		50		60		ns
t _{OED}	Delay time, $\overline{\text{OE}}$ high before data at DQ	20		20		25		ns
t _{ROH}	Delay time, $\overline{\text{OE}}$ low to $\overline{\text{RAS}}$ high	10		10		10		ns
t _{RAD}	Delay time, $\overline{\text{RAS}}$ low to column address (see Note 16)	15	35	15	40	20	55	ns
t _{RAL}	Delay time, column address to $\overline{\text{RAS}}$ high	35		40		45		ns
t _{CAL}	Delay time, column address to $\overline{\text{CAS}}$ high	35		40		45		ns
t _{RCD}	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ low (see Note 16)	20	50	20	60	25	75	ns
t _{RPC}	Delay time, $\overline{\text{RAS}}$ high to $\overline{\text{CAS}}$ low (CBR refresh only)	0		0		0		ns
t _{RSH}	Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{RAS}}$ high	20		20		25		ns
t _{RWD}	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{xW}}$ low (see Note 15)	100		110		135		ns
t _{CPR}	$\overline{\text{CAS}}$ precharge before self refresh	0		0		0		ns
t _{RPS}	$\overline{\text{RAS}}$ precharge after self refresh	130		150		180		ns
t _{RASS}	Self-refresh entry from $\overline{\text{RAS}}$ low	100		100		100		μs
t _{REF}	Refresh time interval (TMS45165 only)		8		8		8	ms
t _{REF}	Refresh time interval, low power (TMS45165P only)		64		64		64	ms
t _{CHS}	$\overline{\text{CAS}}$ low hold time after $\overline{\text{RAS}}$ high	-50		-50		-50		ns
t _T	Transition time	2	50	2	50	2	50	ns

- NOTES: 7. Timing measurements are referenced to V_{IL} max and V_{IH} min.
12. Later of $\overline{\text{CAS}}$ or $\overline{\text{xW}}$ in write operations
13. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. Read-modify-write operation only
16. Maximum value specified only to assure access time.



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PARAMETER MEASUREMENT INFORMATION



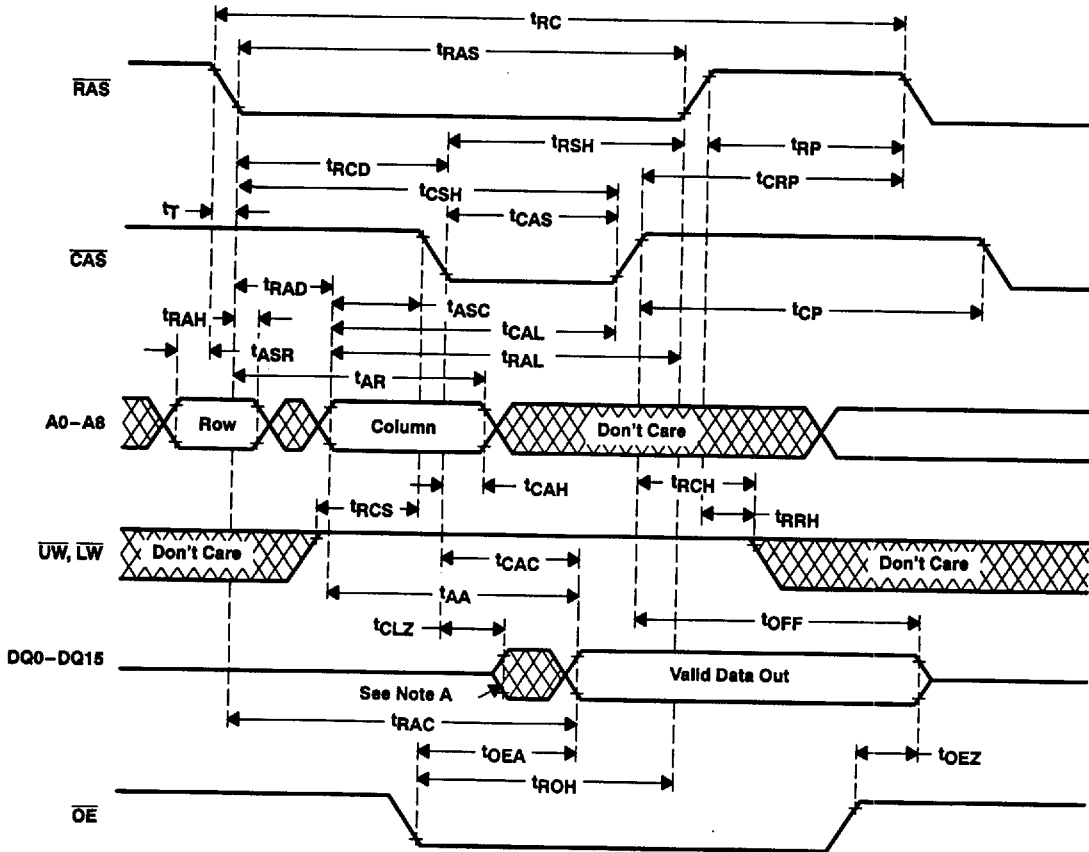
NOTE A: C_L includes probe and fixture capacitance.

Figure 1. Load Circuits for Timing Parameters

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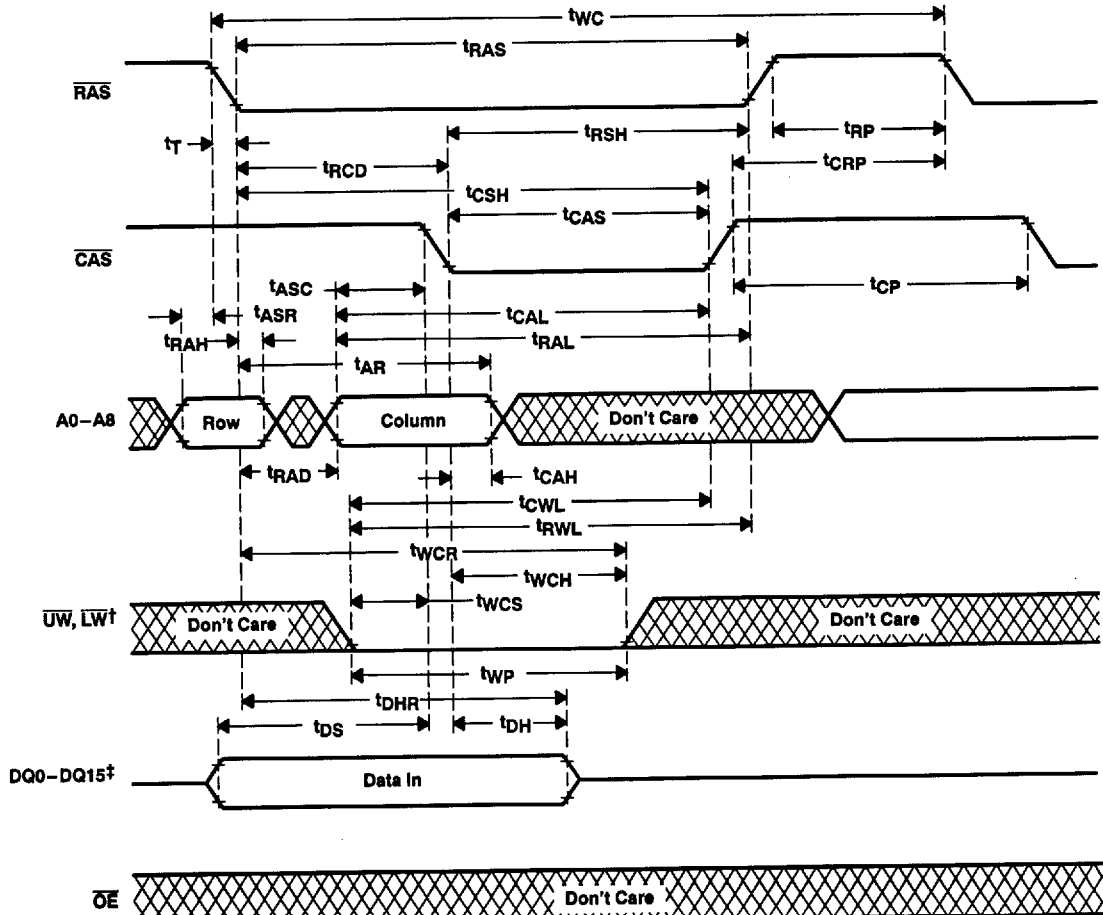
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NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 2. Read-Cycle Timing

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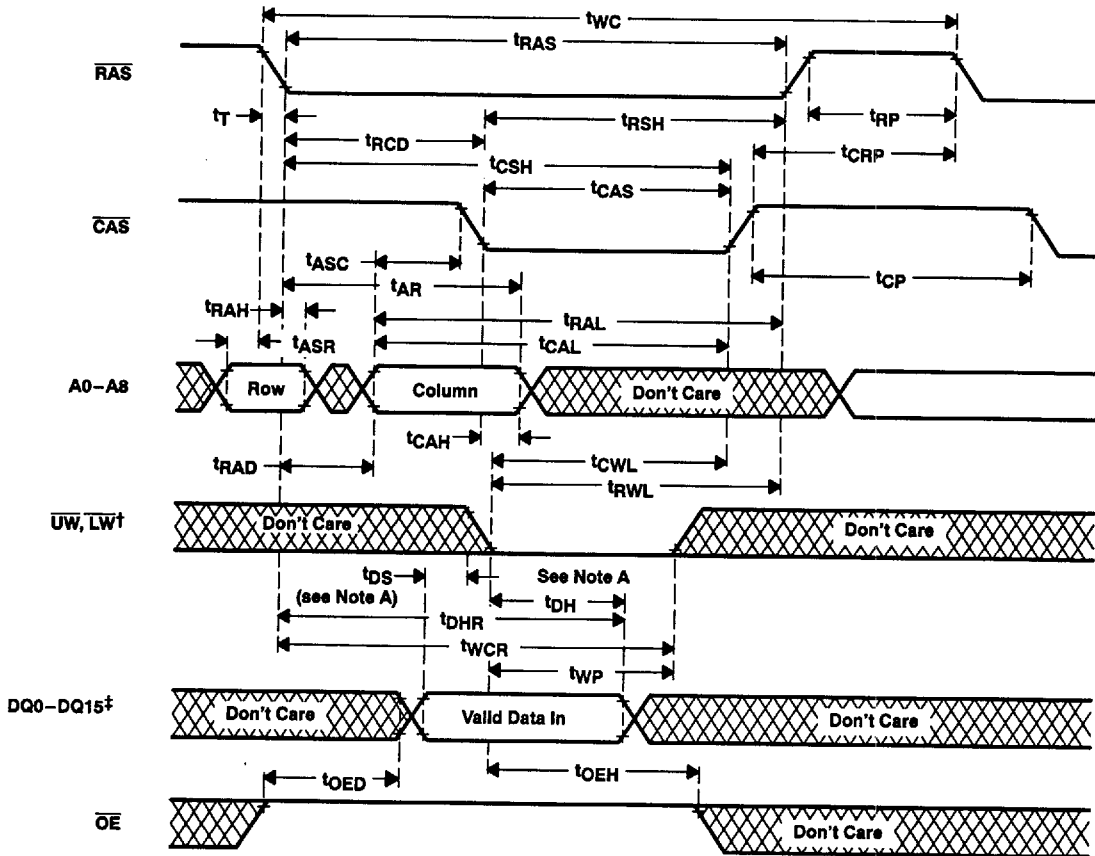
† Either \overline{UW} or \overline{LW} can be brought low and the user can write into eight DQ locations, or \overline{UW} and \overline{LW} can be brought low at the same time and all 16 DQ locations are written into.
 ‡ All DQ pins remain in the high-impedance state for an early-write cycle.

Figure 3. Early-Write-Cycle Timing



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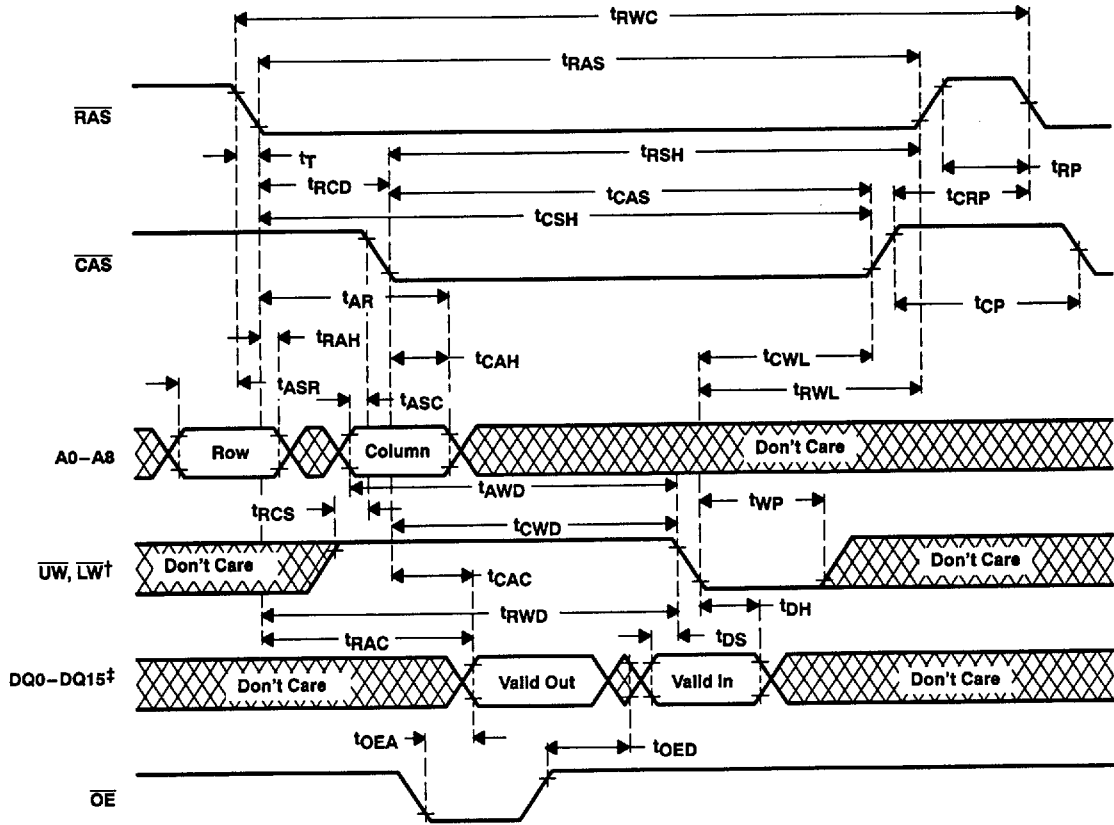
† Either \overline{UW} or \overline{LW} can be brought low and the user can write into eight DQ locations, or \overline{UW} and \overline{LW} can be brought low at the same time and all 16 DQ locations are written into.

‡ All DQ pins remain in the high-impedance state while \overline{OE} is high.

NOTE A: Later of \overline{CAS} or \overline{tW} in write operations.

Figure 4. Write-Cycle Timing

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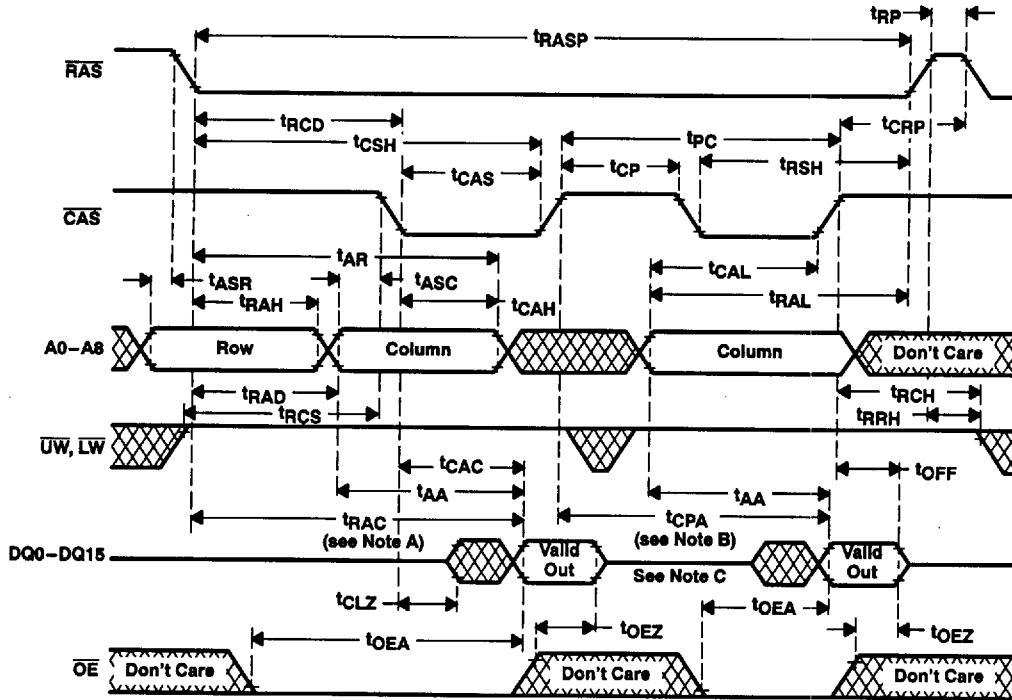
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† Either \overline{UW} or \overline{LW} can be brought low and the user can write into eight DQ locations, or \overline{UW} and \overline{LW} can be brought low at the same time and all 16 DQ locations are written into.

‡ All DQ pins remain in the high-impedance state for an early-write cycle.

Figure 5. Read-Modify-Write-Cycle Timing

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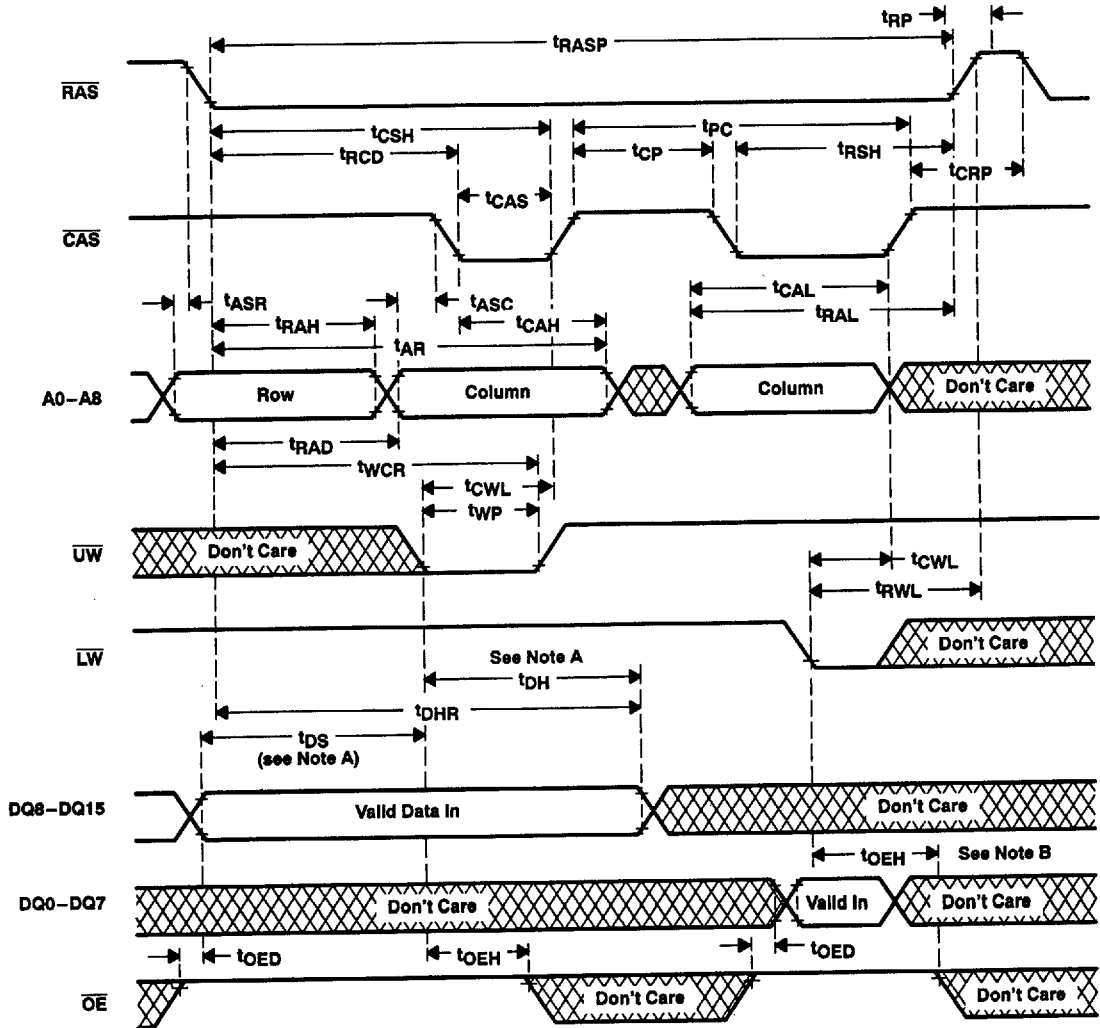
- NOTES: A. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
 B. Access time is t_{CPA} or t_{AA} dependent.
 C. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.

Figure 6. Enhanced Page-Mode Read-Cycle Timing

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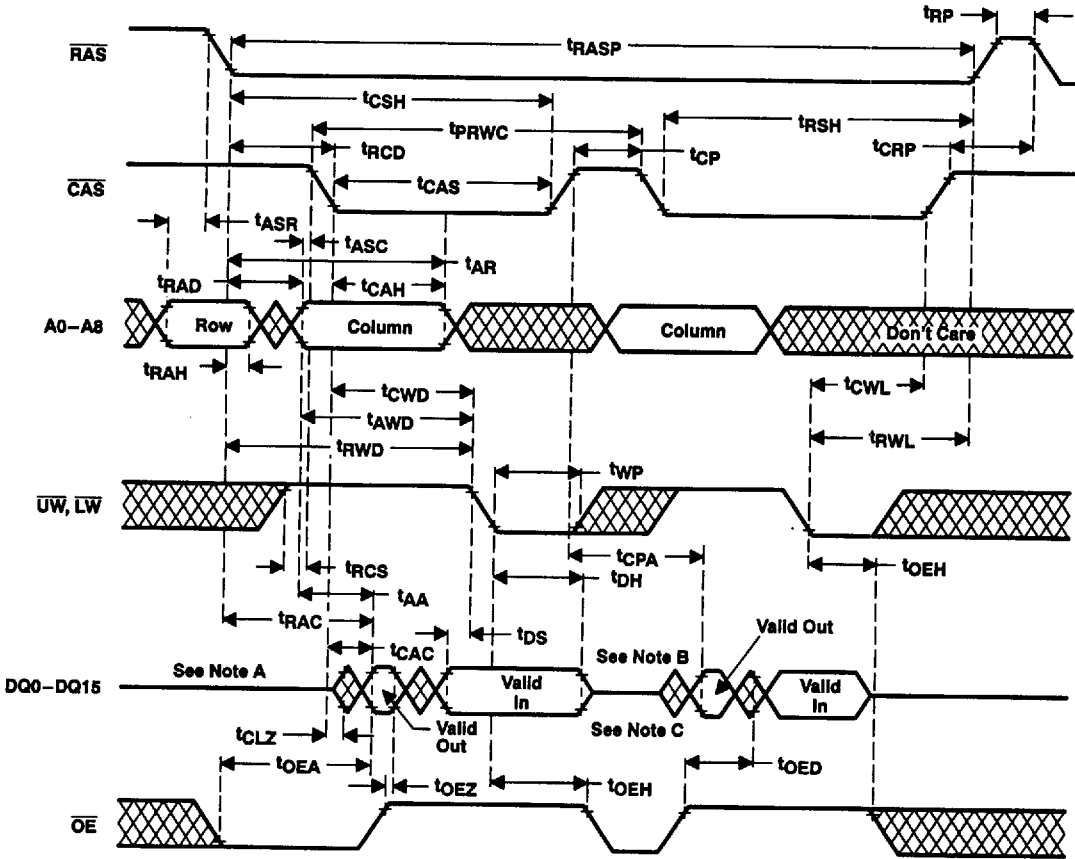
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- NOTES: A. Later of \overline{CAS} or \overline{xW} in write operations.
 B. A read-cycle or read-modify-write cycle can be mixed with the write cycles as long as the read and read-modify-write timing specifications are not violated.

Figure 7. Enhanced Page-Mode Write-Cycle Timing

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- NOTES: A. Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
 B. A read- or write cycle can be intermixed with read-modify-write cycles as long as the read and write cycle timing specifications are not violated.
 C. Access time is tCPA or tAA dependent.

Figure 8. Enhanced Page-Mode Read-Modify-Write-Cycle Timing



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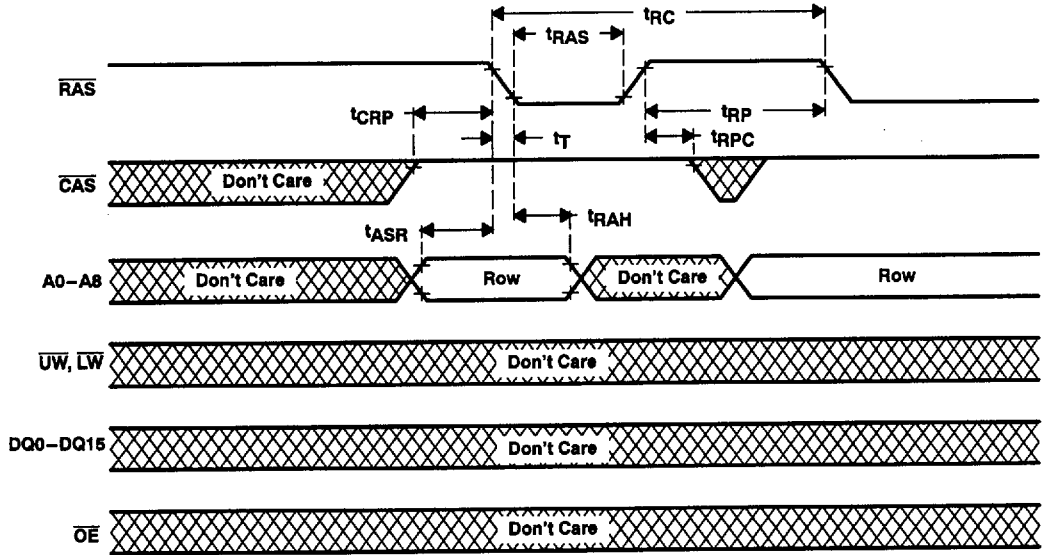


Figure 9. RAS-Only Refresh-Cycle Timing

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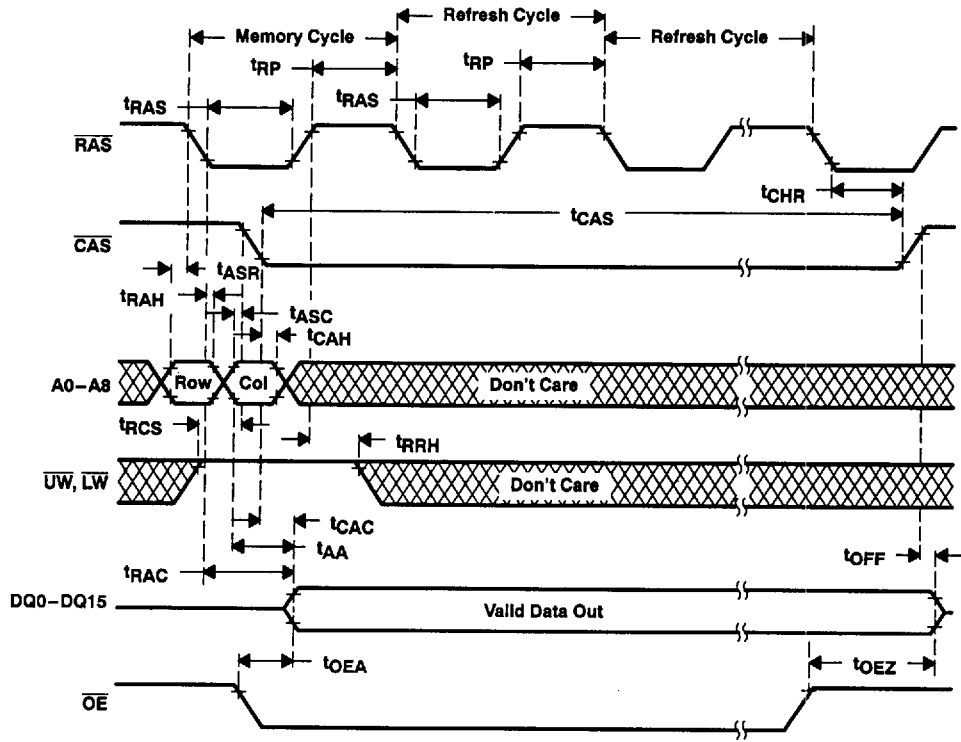
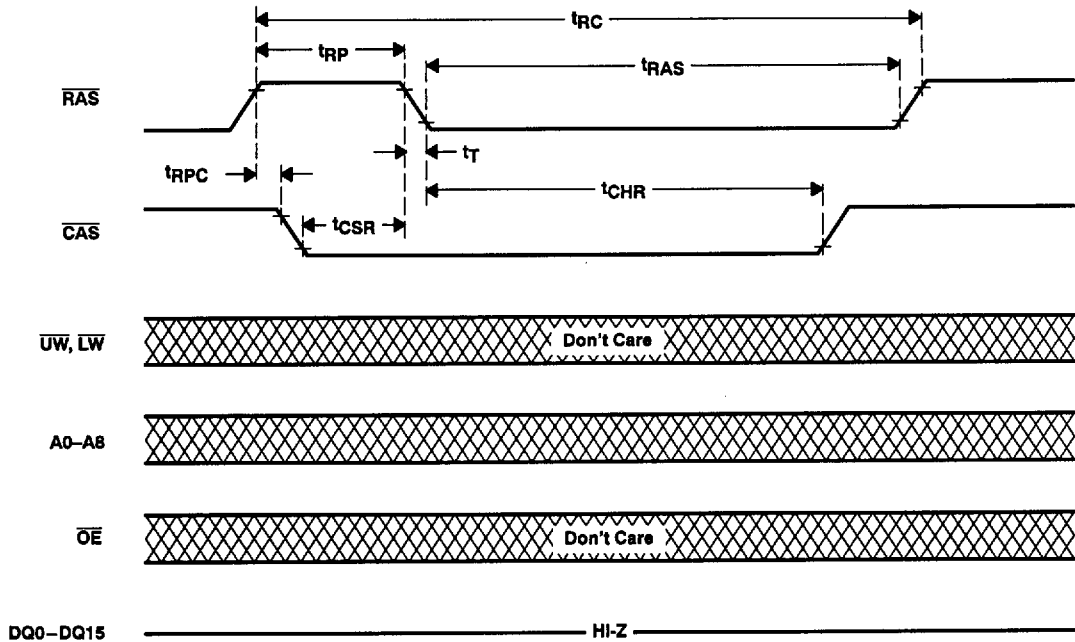


Figure 10. Hidden-Refresh-Cycle Timing

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NOTE A: 512 CBR cycles must be used for CBR counter test.

Figure 11. Automatic-CBR-Refresh-Cycle Timing

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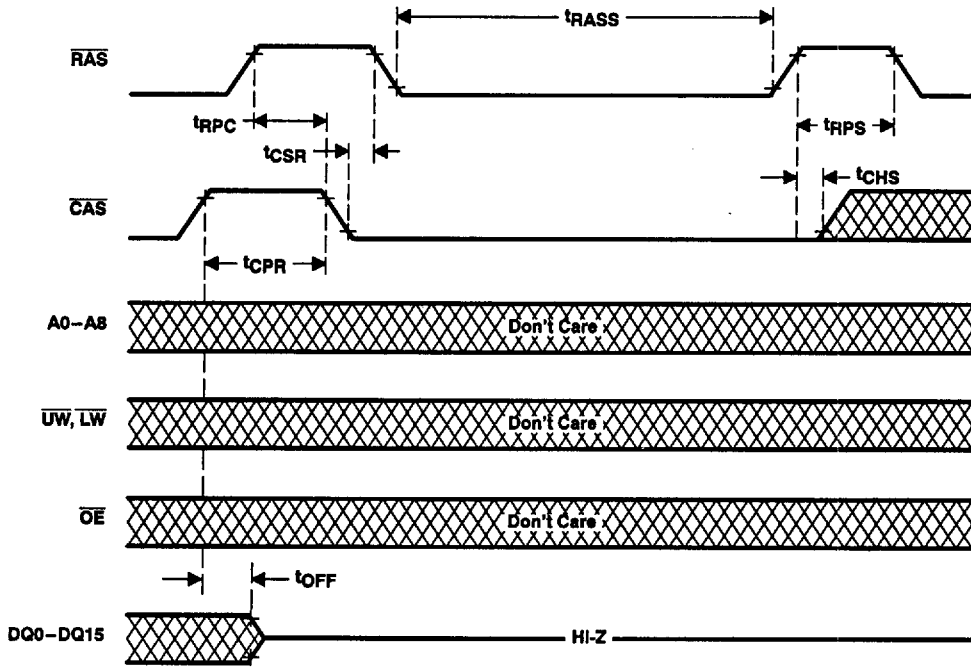


Figure 12. Self-Refresh-Cycle Timing

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device symbolization

