描述

MX5069HD 是一个 N_MOSFET 高边驱动器。MX5069HD 内部集成了 32uA 驱动能力的电荷泵。栅极输出电压在内部限制为大约 VIN+12V。MX5069HD 内部集成了过压和欠压保护，当发生欠压和过压时内部电路将关闭外部 FET。此外，MX5069HD 具有软起动功能。MX5069HD 采用 5V 至 85V 电源供电。

与 MX5069MS/MX5069D 相比，MX5069HD 的 VIN 可以耐-85V 负压； MX5069HD 没有内部反向关断功能。

特性

♦宽工作电压范围：5V 至 85V

♦VIN 最大反向电压：-85V

♦内部高侧电荷泵和栅极驱动器，用于外部 N 沟道 MOSFET

♦可调欠压锁定（UVLO）

♦可调过压锁定（OVP）

♦低电平有效漏极开路 POWER GOOD 输出

♦可自动重启

♦10 引脚 DFN3*3-10L 封装

应用

♦电动车

♦光伏

♦固态断路器

♦24V 和 48V 工业系统

基本信息

订购信息

型号	描述
MX5069HD	DFN3*3-10L
MPQ	3000pcs

封装耗散值

封装	RθJA（℃/W）
DFN3*3-10L	50

极限值

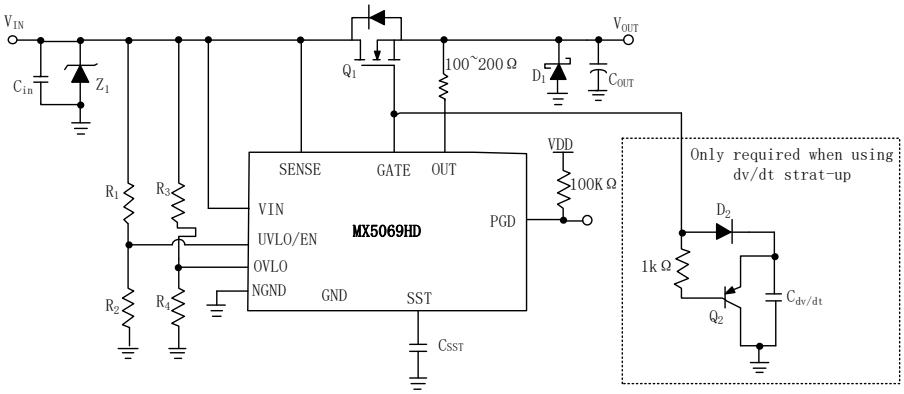
参数	值
VIN to GND	-0.3 to 90V
VIN to NGND	-90 to 90V
SENSE, OUT to GND	-0.3 to 90V
GATE to GND	-0.3 to 100V
OUT to GND (1ms transient)	-0.3 to 95V
UVLO to GND	-0.3 to 5.5V
OVP, PGD to GND	-0.3 to 7V
VIN to SENSE	-0.3 to 0.3V
最大结温, T_{JMAX}	150℃
存储温度, T_{stg}	-65 to 150℃

超出极限值中列出的范围可能会对设备造成永久性损坏。长时间工作在极限值条件下可能会影响可靠性。不建议设备在超出“推荐操作条件”部分中指示的任何条件下的功能运行。

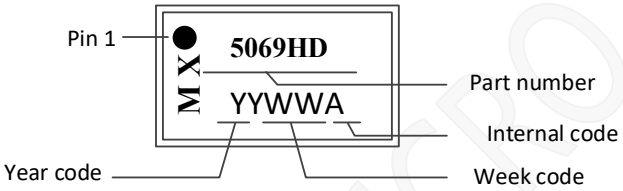
推荐工作条件

项目	范围
输入电压	5 to 85V
PGD, UVLO/EN 电压	0 to 5V
结温	-40 to 125℃

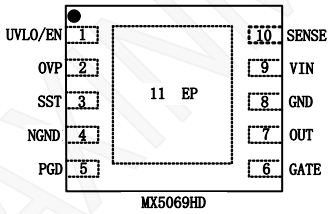
Typical application



Marking information

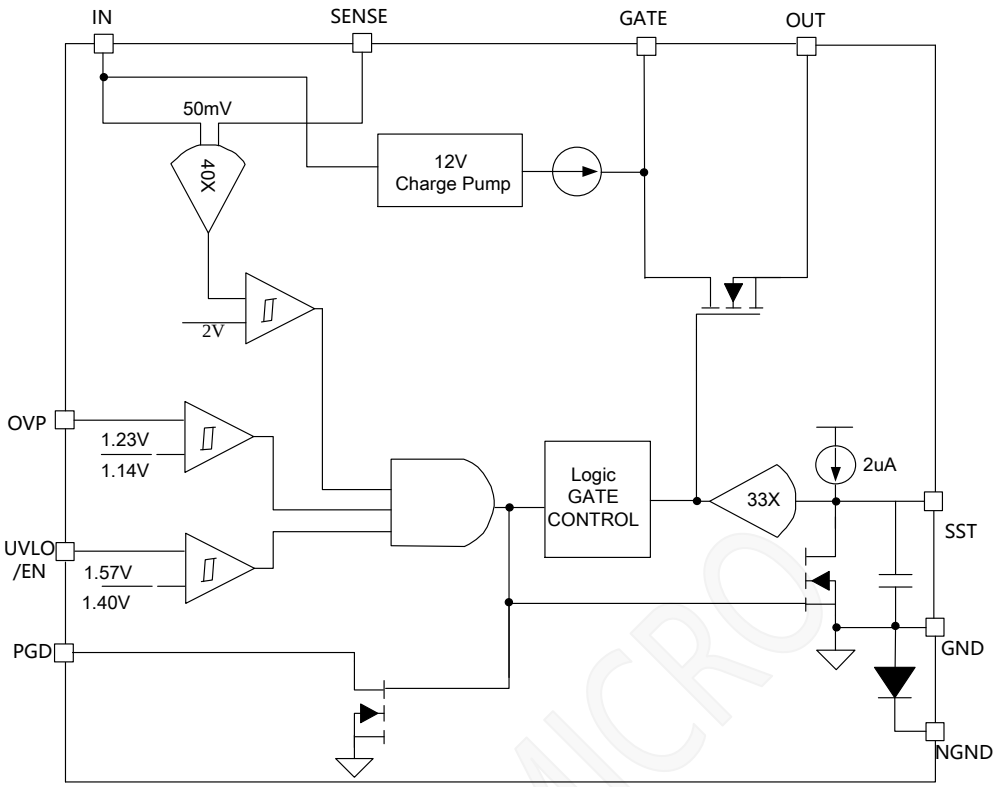


Terminal assignments



PIN NO.	PIN name	Description
1	UVLO/EN	This is a dual function control pin. When used as an ENABLE pin and pulled down, it shuts off the internal pass MOSFET. As an UVLO pin, it can be used to program different UVLO trip point via external resistor divider.
2	OVP	Overvoltage lockout: An external resistor divider from the system input voltage sets the overvoltage turnoff threshold. The disabled threshold at the pin is 1.23V.
3	SST	A capacitor from this pin to GND sets output voltage slew rate.
4	NGND	Using NGND instead of GND makes VIN resistant to -85V reverse voltage
5	PGD	Power Good indicator: An open drain output.
6	GATE	Gate drive output: Connect to the external MOSFET's gate. This pin's voltage is typically 12V above the OUT pin when enabled.
7	OUT	Output feedback: Connect to the output rail (external MOSFET source).
8	GND	Internal circuit ground. This GND is used when VIN does not require an inverting voltage drop.
9	VIN	Positive supply input: A small ceramic bypass capacitor close to this pin is recommended to suppress transients which occur when the load current is switched off.
10	SENSE	Connected this pin to VIN.
11	EP	Power Pad, Connect to GND or NGND as needed.

Block diagram



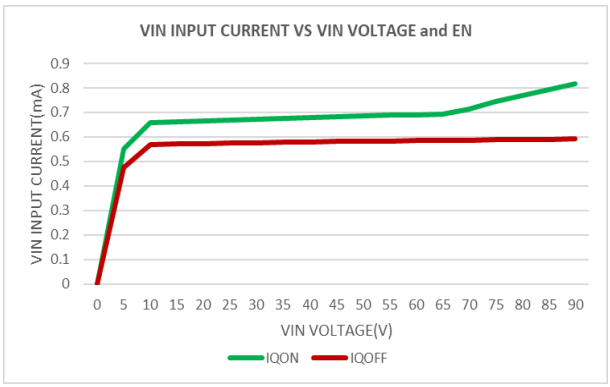
Electrical characteristics

VIN = 12V, UVLO=2V, OVP = NGND, T_J = 25°C, unless otherwise noted.

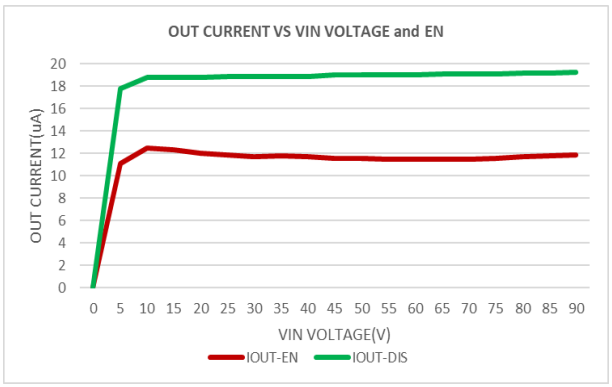
Symbol	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT (VIN PIN)						
VIN			5		85	V
I_{QON}	Supply current	Enabled: EN/UVLO = 2V	0.48	0.55	0.70	mA
I_{QOFF}		EN/UVLO = 0V	0.40	0.45	0.70	mA
EN/UVLO						
V_{UVLOR}	UVLO Threshold voltage	rising	1.47	1.57	1.70	V
V_{UVLOF}	UVLO Threshold voltage	falling	1.30	1.40	1.50	V
I_{UVLO}	UVLO leakage current	EN/UVLO = 0V	-3.5	-2.6	0	uA
t_{DUVLO}	UVLO delay	Delay to GATE high		840		us
		Delay to GATE low		3.4		us
OVP PINS						
V_{OVPR}	OVP Threshold voltage	Rising	1.10	1.23	1.35	V
V_{OVPF}	OVP Threshold voltage	Falling	1.0	1.14	1.3	V
t_{DOVP}	OVP delay	Delay to GATE high		13.8		µs
		Delay to GATE low		4.4		
I_{OVP}	OVP bias current		-1		2	µA
OUT PIN						
I_{OUT}	OUT bias current, disabled	Disabled, OUT = 0V	0	20	30	uA
GATE CONTROL (GATE PIN)						

I_{GATE}	Source current	Normal operation	1	32	40	μA
	Sink current	Disabled	-1	0.1	1	uA
		OVP>1.23V		2		A
V_{GATE}	Gate output voltage in normal operation	GATE-OUT voltage	8	10	14	V
SST (SST PIN)						
I_{SST}	SST Charging current	Normal operation	0	2	5	uA
R_{SST}	SST Discharging resistance		60	75	90	Ω
V_{SSTmax}	SST max capacitor voltage		4.4	5.2	5.5	V
$GAIN_{SST}$	SST to GATE gain			33		V/V
tSST	SST floating			230		us
PGD						
V_{PGD}	Output low voltage	I_{SINK} = 10mA	60	75	90	Ω
I_{PGD}	Off leakage current	V_{PGD} = 5V	-1	0.5	2	μA

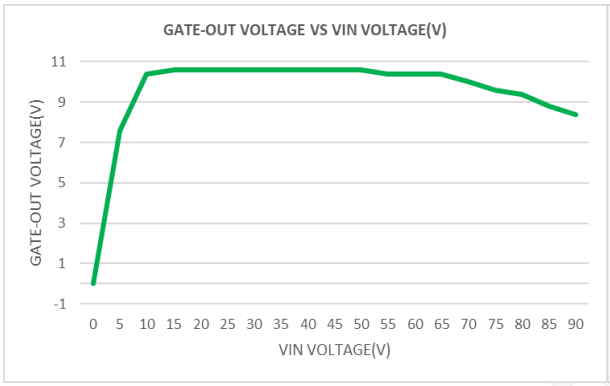
Characteristic plots



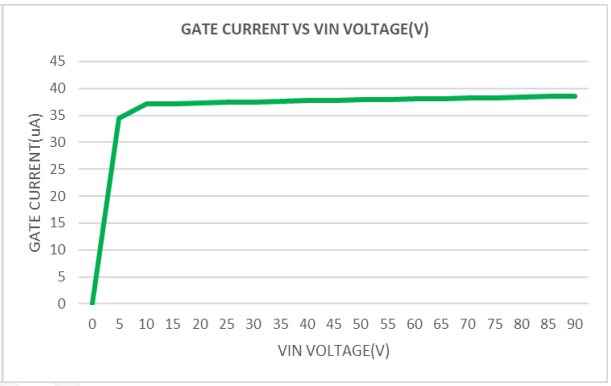
INPUT current vs VIN voltage



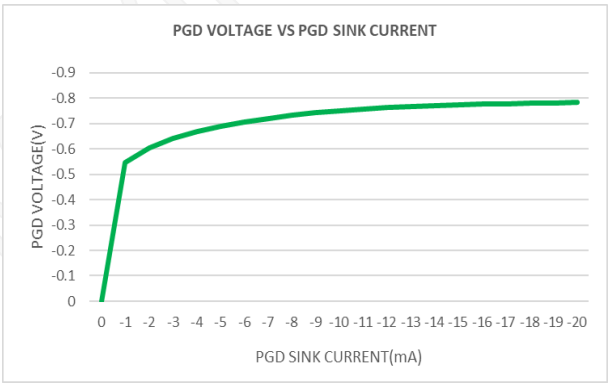
OUT current vs VIN voltage



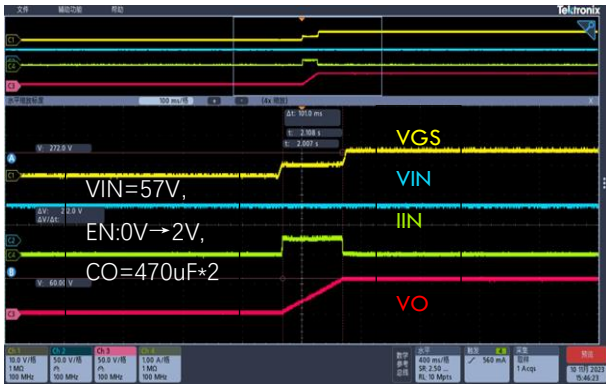
GATE-OUT voltage vs VIN voltage



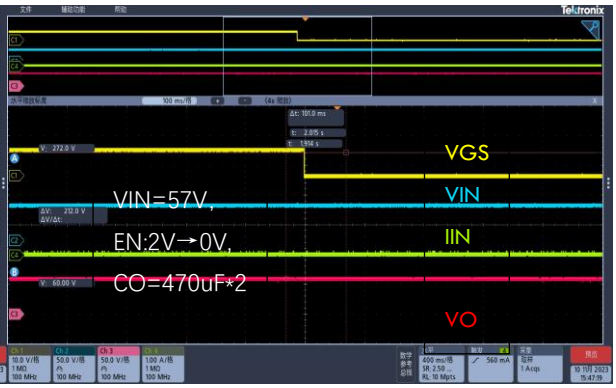
GATE current vs VIN voltage



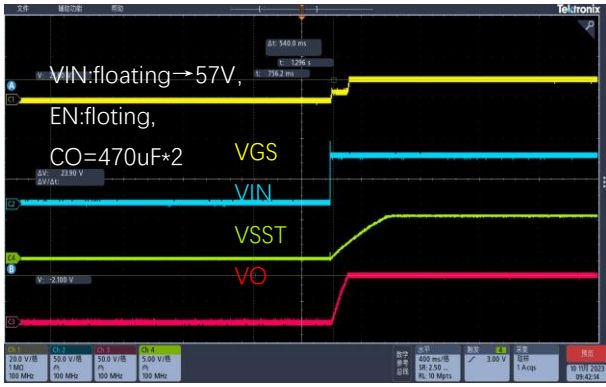
PGOOD voltage vs sink current



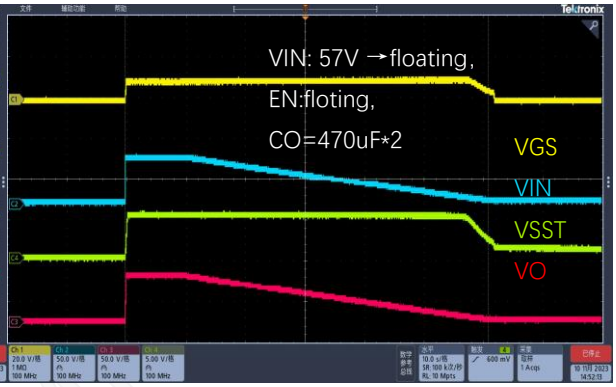
Start up with EN



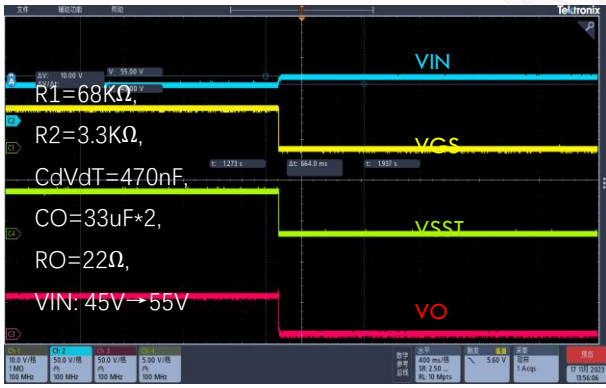
Shut down with EN



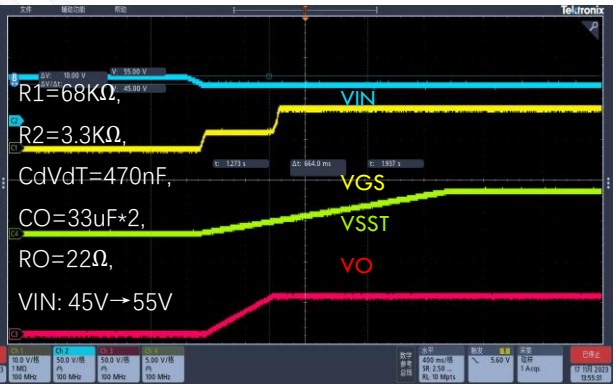
Start up with VIN (VIN added TVS)



Shut down VIN (VIN added TVS)



Enter over voltage protect



Exit over voltage protect

Detailed description

Overview

MX5069HD have undervoltage lockout (UVLO) and overvoltage lockout (OVP) circuits shut down the MX5069HD when the system input voltage is outside the desired operating range.

Undervoltage Lockout (UVLO)

As an input pin, it controls the ON/OFF state of the internal MOSFET. In its high state, the internal MOSFET is enabled. A low on this pin will turn off the internal MOSFET. High and Low levels are specified in the parametric table of the datasheet. The EN/UVLO pin is also used to clear a thermal shutdown latch by toggling this pin high to low.

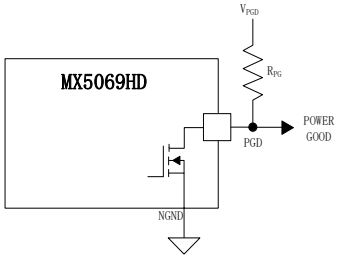
The internal de-glitch delay on EN/UVLO falling edge is intentionally kept low (1us typical) for quick detection of power failure. When used with a resistor divider connected between IN, UVLO, OVP and GND or NGND pins of the device, power-fail detection on EN/UVLO helps in quick turn-off of the FET driver, thereby stopping the flow of reverse current. For applications where a higher de-glitch delay on EN/UVLO is desired, or when the supply is particularly noisy, it is recommended to use an external bypass capacitor from EN/UVLO to GND.

Overvoltage Lockout (OVP)

The over voltage protection can be set by an external resistor divider. When the voltage of OVP pin exceed the internal reference voltage (1.23V typical), the internal MOSFET will be turned off quickly. When the voltage of this pin returns to the hysteresis voltage, the internal MOSFET will be reopened after the dVdT time.

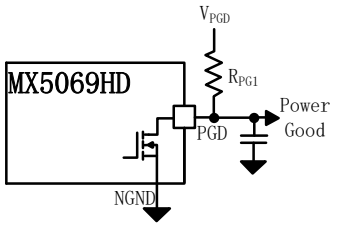
Power Good Pin

During turn-on, the Power Good pin (PGD) is high until the voltage at VIN increases above ≈ 5V. PGD then switches low, remaining low as the VIN voltage increases. When the voltage at OUT increases to within 1.25V of the SENSE pin (VDS <1.25V), PGD switches high. PGD switches low if the VDS of Q1 increases above 2.5V. A pullup resistor is required at PGD as shown in the following figure. The pullup voltage (VPGD) can be as high as 5V.

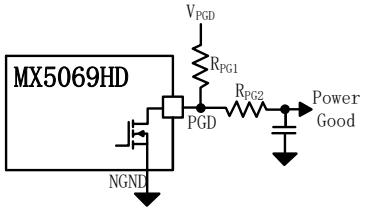


Power Good Output

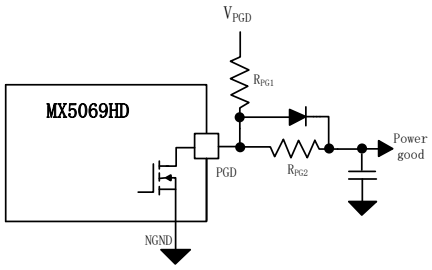
If a delay is required at PGD, suggested circuits are shown in the following figure. In figure a), capacitor C_{PG} adds delay to the rising edge, but not to the falling edge. In figure b), the rising edge is delayed by $R_{PG1} + R_{PG2}$ and C_{PG}, while the falling edge is delayed a lesser amount by R_{PG2} and C_{PG}. In figure c), adding a diode across R_{PG2} allows for equal delays at the two edges, or a short delay at the rising edge and a long delay at the falling edge.



a) Delay Rising Edge Only



b) Long delay at rising edge, short delay at falling edge



c) Short Delay at Rising Edge and Long Delay at Falling Edge or Equal Delays

Adding delay to the power good output pin

Gate control

A charge pump provides internal bias voltage above the output voltage (OUT pin) to enhance the N-Channel MOSFET's gate. The gate-to-source voltage is limited by an internal 12V Zener diode. During normal operating conditions the gate of Q1 is held charged by an internal 32μA current source to approximately 12V above OUT.

Application and Implementation

Design Requirements

When charging the output capacitor through the MOSFET, the FET's total energy dissipation equals the total energy stored in the output capacitor (½CV^2). Thus, both the input voltage and output capacitance determine the stress experienced by the MOSFET. The maximum load current drives the current limit and sense resistor selection. In addition, the maximum load current, maximum ambient temperature, and the thermal properties of the PCB ($R_{\theta CA}$) drive the selection of the MOSFET R_{DSON} and the number of MOSFETs used. $R_{\theta CA}$ is a strong function of the layout and the amount of copper that is connected to the drain of the MOSFET. Note that the drain is not electrically connected to the ground plane and thus the ground plane cannot be used to help with heat dissipation. It's a good practice to measure the $R_{\theta CA}$ of a given design after the physical PCBs are available.

Detailed Design Procedure

MOSFET Selection

The important MOSFET electrical parameters are the maximum continuous Drain current I_D, the maximum Source current (that is, body diode) I_S, the maximum drain-to-source voltage $V_{DS(MAX)}$, the gate-to-source threshold voltage $V_{GS(TH)}$, the drain-to-source reverse breakdown voltage $V_{(BR)DSS}$, and the drain-to-source on resistance $R_{DS(ON)}$.

The maximum continuous drain current, I_D, rating must exceed the maximum continuous load current. The rating for the maximum current through the body diode, I_S, is typically rated the same as, or slightly higher than the drain current, but body diode current only flows while the MOSFET gate is being charged to $V_{GS(TH)}$.

Gate Charge Time = Qg / $I_{GATE(ON)}$

1. The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest differential voltage seen in the application. This would include any anticipated fault conditions.
2. The drain-to-source reverse breakdown voltage, $V_{(BR)DSS}$, may provide some transient protection to the OUT pin in low voltage applications by allowing conduction back to the IN pin during positive transients at the OUT pin.
3. The gate-to-source threshold voltage, $V_{GS(TH)}$, should be compatible with the MX5069HD gate drive capabilities. Logic level MOSFETs, with $R_{DS(ON)}$ rated at $V_{GS(TH)}$ at 5V, are recommended, but sub-Logic level MOSFETs having $R_{DS(ON)}$ rated at $V_{GS(TH)}$ at 2.5V, can also be used.
4. The dominate MOSFET loss for the MX5069HD active OR-ing controller is conduction loss due to source - to - drain current to the output load, and the $R_{DS(ON)}$ of the MOSFET. This conduction loss could be reduced by using a MOSFET with the lowest possible $R_{DS(ON)}$. However, contrary to popular belief, arbitrarily selecting a MOSFET based solely on having low $R_{DS(ON)}$ may not always give desirable results for several reasons:

1. Reverse current leakage. In cases where multiple input supplies are closely matched it may be possible for some small current to flow continuously through the MOSFET drain to source (that is, reverse). Higher $R_{DS(ON)}$ will reduce this reverse current level.
2. Cost. Generally, as the $R_{DS(ON)}$ rating goes lower, the cost of the MOSFET goes higher.
3. The dominate MOSFET loss for the MX5069HD active

OR-ing controller is conduction loss due to source-to- drain current to the output load, and the $R_{DS(ON)}$ of the MOSFET. This conduction loss could be reduced by using a MOSFET with the lowest possible $R_{DS(ON)}$. However, contrary to popular belief, arbitrarily selecting a MOSFET based solely on having low $R_{DS(ON)}$ may not always give desirable results for several reasons:

a. It is suggested that $R_{DS(ON)}$ be selected to provide no more than 100mV, at the nominal load current.

$$R_{DS(ON)} \leq (100mV / I_D)$$

b. The thermal resistance of the MOSFET package should also be considered against the anticipated dissipation in the MOSFET to ensure that the junction temperature (T_J) is reasonably well controlled, because the $R_{DS(ON)}$ of the MOSFET increases as the junction temperature increases.

$$P_{DISS} = I_D^2 \times (R_{DS(ON)})$$

5. Operating with a maximum ambient temperature ($T_{A(MAX)}$) of 35°C, a load current of 10A, and an $R_{DS(ON)}$ of 10mΩ, and desiring to keep the junction temperature under 100°C, the maximum junction-to-ambient thermal resistance rating ($R\theta_{JA}$) must be:

a. $R_{\theta JA} \leq (T_{J(MAX)} - T_{A(MAX)}) / (I_D^2 \times R_{DS(ON)})$

b. $R_{\theta JA} \leq (100°C - 35°C) / (10A \times 10A \times 0.01\Omega)$

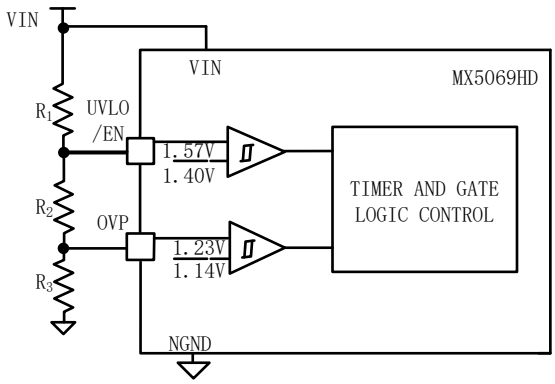
c. $R_{\theta JA} \leq 65°C/W$.

Set Undervoltage and Overvoltage Threshold

By programming the UVLO and OVP thresholds the MX5069HD enables the series pass device (Q1) when the input supply voltage (VIN) is within the desired operational range. If VIN is below the UVLO threshold, or above the OVP threshold, Q1 is switched off, denying power to the load. Hysteresis is provided for each threshold. The OVP function can be disabled by grounding the OVP pin.

Option A

The configuration shown in the following figure requires three resistors (R1 ~ R3) to set the thresholds.



The undervoltage lockout (UVLO) and overvoltage trip point are adjusted using an external voltage divider network of R1, R2 and R3 connected between IN, UVLO, OVP and GND pins of the device. The values required for setting the undervoltage and overvoltage are calculated by the following equation:

$$V_{UVLOF} = \frac{R_2 + R_3}{R_1 + R_2 + R_3} \cdot V_{UVP}$$

$$V_{OVPR} = \frac{R_3}{R_1 + R_2 + R_3} \cdot V_{OVP}$$

Where V_{UVLOF} = 1.40V and V_{OVPR} = 1.23V.

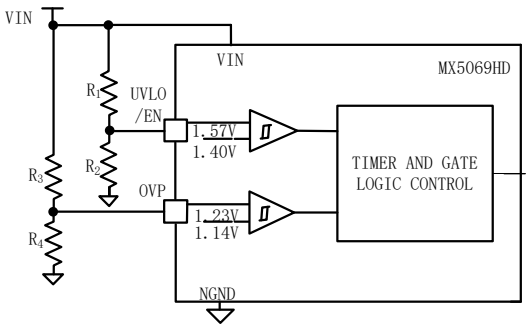
V_{UVP} is input under voltage protection and V_{OVP} is input over voltage protection.

Since R1, R2 and R3 will leak the current from input supply VIN, these resistors should be selected based on the acceptable leakage current from input power supply VIN. The current drawn by R1, R2 and R3 from the power supply {I_{R123} = VIN / (R1 + R2 + R3)}.

However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, I_{R123} must be chosen to be 20x greater than the leakage current of EN/UVLO and OVP pins.

Option B

If all four thresholds must be accurately defined, the configuration in the following figure can be used.



The four resistor values are calculated as follows:

$$R2 = \frac{1.40V \times R1}{(V_{UVP} - 1.40V)}$$

$$R4 = \frac{1.23V \times R3}{(V_{OVP} - 1.23V)}$$

Where the R1 ~ R4 resistor values are known, the threshold voltages and hysteresis are calculated by the following equations:

$$V_{UVP} = \frac{1.40V \times (R1 + R2)}{R2}$$

$$V_{OVP} = \frac{1.23V \times (R3 + R4)}{R4}$$

Setting Output Voltage Ramp Time

Connect a capacitor from this pin to GND to control the slew rate of the output voltage at power-on. This pin can be left floating to obtain a predetermined slew rate (minimum t_{SST}) on the output.

$$\frac{dV_O}{dt} = \frac{I_{SST} \times GAIN_{SST}}{C_{SST} + C_{INT}}$$

Where:

I_{SST} = 2uA (TYP)

$GAIN_{SST}$ = 33

C_{INT} = 60pF

$\frac{dV_O}{dt}$ = Desired output slew rate

The total ramp time (T_{SST}) for 0 to VIN can be calculated using the following equation:

$T_{SST} = 1.5 \times 10^4 \times VIN \times (C_{SST} + C_{INT})$

Input and Output Protection

Proper operation of the MX5069HD hot swap circuit requires a voltage clamping element present on the supply side of the connector into which the hot swap circuit is plugged in. A TVS is ideal, as depicted in Typical application. The TVS is necessary to absorb the voltage transient generated whenever the hot swap circuit shuts off the load current. This effect is the most severe during a hot-short when a large current is suddenly interrupted when the FET shuts off. The TVS must be chosen to have minimal leakage current at V_{INMAX} and to clamp the voltage to under 30V during hot-short events. A 100~200ohm resistor should be palced between OUT pin and Source of external MOSFET to prevent damage from surge voltage, as the R_{SOURCE} shown in the Typical application.

Power Supply Recommendations

In general, the MX5069HD behavior is more reliable if it is supplied from a very regulated power supply. However, high-frequency transients on a backplane are not uncommon due to adjacent card insertions or faults. If this is expected in the end system, Maxin recommends placing a 1μF ceramic capacitor to ground close to the drain of the MOSFET. Additional filtering may be necessary to avoid nuisance trips.

Layout Guidelines

The following guidelines must be followed when designing the PCB for the MX5069HD:

- Place the MX5069HD close to the board's input connector to minimize trace inductance from the connector to the FET.
- The high current path from the board's input to the load (via Q1), and the return path, must be parallel and close to each other to minimize loop inductance.
- The ground connection for the various components around the MX5069HD must be connected directly to each other, and to the MX5069HD's GND or NGND pin, and then connected to the system ground at one point. Do not connect

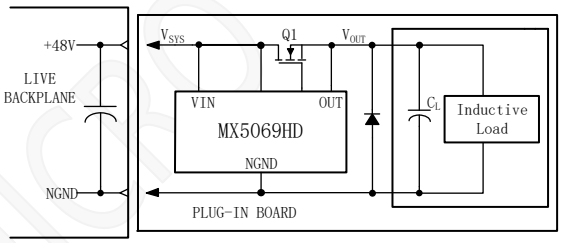
the various component grounds to each other through the high current ground line.

- Provide adequate heat sinking for the series pass device (Q1) to help reduce stresses during turnon and turnoff.
- The board's edge connector can be designed to shut off the MX5069HD as the board is removed, before the supply voltage is disconnected from the MX5069HD. When the board is inserted into the edge connector, the system voltage is applied to the MX5069HD's VIN pin before the UVLO voltage is taken high.

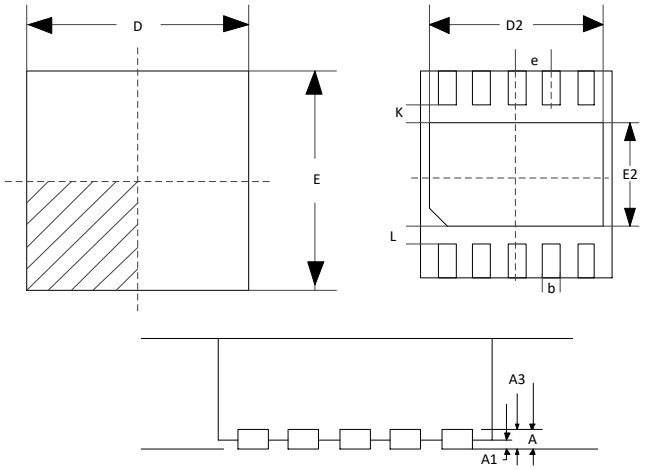
System Considerations

A) Continued proper operation of the MX5069HD hot swap circuit requires capacitance be present on the supply side of the connector into which the hot swap circuit is plugged in, as depicted in the following figure. The capacitor in the Live Backplane section is necessary to absorb the transient generated whenever the hot swap circuit shuts off the load current. If the capacitance is not present, inductance in the supply lines generate a voltage transient at shut-off which can exceed the absolute maximum rating of the MX5069HD, resulting in its destruction.

B) If the load powered via the MX5069HD hot swap circuit has inductive characteristics, a diode is required across the MX5069HD's output. The diode provides a recirculating path for the load's current when the MX5069HD shuts off that current. Adding the diode prevents possible damage to the MX5069HD as the OUT pin is taken below ground by the inductive load at shutoff.



Package information DFN3*3-10L



DFN3*3-10L for MX5069HD

SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.0275	0.0295	0.0315
A1	0.00	0.03	0.05	0.00	0.0012	0.0020
A3		0.20BSC			0.008BSC	
b	0.18	0.24	0.30	0.007	0.009	0.011
D		3.00BSC			0.12BSC	
D2	2.45	2.50	2.55	0.096	0.098	0.100
E		3.00BSC			0.12BSC	
E2	1.75	1.80	1.85	0.069	0.071	0.073
e		0.50BSC			0.02BSC	
K		0.19TYP			0.0075BSC	
θ	0.35	0.40	0.45	0.014	0.016	0.018

Restrictions on Product Use

◆ MAXIN micro is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing MAXIN products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such MAXIN products could cause loss of human life, bodily injury or damage to property.

◆ In developing your designs, please ensure that MAXIN products are used within specified operating ranges as set forth in the most recent MAXIN products specifications.

◆ The information contained herein is subject to change without notice.

Version update record:

V10 The original version （preliminary）