100V Dual High-Side MOSFET Gate Driver

FEATURES

- **Unique Symmetric Floating Gate Driver Architecture**
- **High Noise Immunity, Tolerates ±10V Ground Difference**
- **100V Maximum Input Voltage Independent of IC Supply Voltage V_{CC}**
- **5V to 14V V_{CC} Operating Voltage**
- **4V to 14V Gate Driver Voltage**
- **0.8Ω Pull-Down, 1.5Ω Pull-Up for Fast Turn-On/Off**
- TTL/CMOS Compatible Input
- V_{CC} UVLO/OVLO and Floating Supplies UVLO
- Drives Dual N-Channel MOSFETs
- Open-Drain Fault Indicator (V_{CC} UVLO/OVLO, Gate Driver UVLO and Thermal Shutdown)
- Available in Thermally Enhanced 12-Lead MSOP
- AEC-Q100 Automotive Qualification in Progress

APPLICATIONS

- Automotive and Industrial Power Systems
- Telecommunication Power Systems

DESCRIPTION

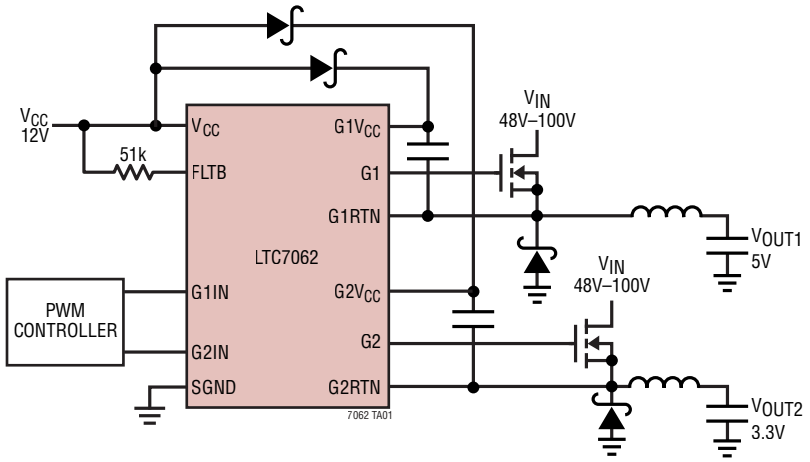
The LTC®7062 drives two high-side N-Channel MOSFETs with supply voltages up to 100V. Both drivers can operate with a different ground reference, providing excellent noise and transient immunity. The two drivers are symmetric and independent of each other, allowing complementary or non-complementary switching.

Its powerful 0.8Ω pull-down and 1.5Ω pull-up MOSFET drivers allows the use of large gate capacitance high voltage MOSFETs. Additional features include UVLO, TTL/CMOS compatible inputs and fault indicator.

See chart below for a similar driver in this product family.

PARAMETER	LTC7060	LTC7061	LTC7062	LTC7063
Input Signal	3-State PWM	CMOS/ TTL Logic	CMOS/ TTL Logic	3-State PWM
Shoot-Through Protection	Yes	Yes	No	Yes
Absolute Max Voltage	115V	115V	115V	155V
V_{CC} Falling UVLO	5.3V	4.3V	4.3V	5.3V

TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS

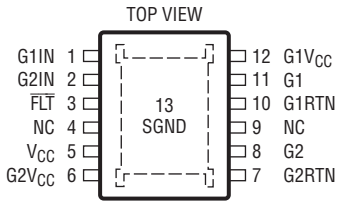
(All voltages are referred to SGND unless otherwise noted.)

(Note 1)

V_{CC} Supply Voltage .....–0.3V to 15V
G1 Gate Driver Voltage ($G1V_{CC}$) .....–0.3V to 115V
G2 Gate Driver Voltage ($G2V_{CC}$).....–0.3V to 115V
G1RTN, G2RTN .....–10V to 100V
($G1V_{CC}$ – G1RTN).....–0.3V to 15V
($G2V_{CC}$ – G2RTN) .....–0.3V to 15V
$\overline{FLT}$ ..... –0.3V to 15V
G1IN, G2IN ..... –0.3V to 6V
Output G1 (with Respect to G1RTN) .....–0.3V to 15V
Output G2 (with Respect to G2RTN).....–0.3V to 15V
Operating Junction Temperature
Range (Notes 2, 3)..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

Note: All voltage are referred to SGND unless otherwise noted.

PIN CONFIGURATION



MSE PACKAGE
12-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 40°C/W
EXPOSED PAD (PIN 13) IS SGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC7062EMSE#PBF	LTC7062EMSE#TRPBF	LTC7062	12-Lead Plastic MSOP	–40°C to 125°C
AUTOMOTIVE PRODUCTS**				
LTC7062IMSE#WPBF	LTC7062IMSE#WTRPBF	LTC7062	12-Lead Plastic MSOP	–40°C to 125°C
LTC7062JMSE#WPBF	LTC7062JMSE#WTRPBF	LTC7062	12-Lead Plastic MSOP	–40°C to 150°C
LTC7062HMSE#WPBF	LTC7062HMSE#WTRPBF	LTC7062	12-Lead Plastic MSOP	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{CC} = V_{G1VCC} = V_{G2VCC} =10V, V_{G1RTN} = V_{G2RTN} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply and V_{CC} Supply							
V_{IN}	Input Supply Operating Range					100	V
V_{CC}	IC Supply Operating Range			5		14	V
I_{VCC}	V_{CC} Supply Current	V_{G1IN} = V_{G2IN} = 0V			0.3		mA
V_{UVLO_VCC}	V_{CC} Undervoltage Lockout Threshold	V_{CC} Falling			4.3		V
		Hysteresis			0.2		V
V_{OVLO_VCC}	V_{CC} OVLO Threshold	V_{CC} Rising			14.6		V
		Hysteresis			0.8		V
G1 Gate Driver Supply (G1V_{CC} – G1RTN)							
$V_{G1VCC–G1RTN}$	G1 Driver Supply Voltage Range (With Respect to G1RTN)			4		14	V
I_{G1VCC}	Total G1VCC Current (Note 4)	G1 = L			8.9		µA
		G1 = H			146		µA
V_{UVLO_G1VCC}	Undervoltage Lockout Threshold	G1V_{CC} Falling, Respect to G1RTN			3.4		V
		Hysteresis			0.3		V
G2 Gate Driver Supply (G2V_{CC} – G2RTN)							
$V_{G2VCC–G2RTN}$	G2 Driver Supply Voltage Range (With Respect to G2RTN)			4		14	V
I_{G2VCC}	Total G2V_{CC} Current (Note 4)	G2 = L			8.9		µA
		G2 = H			146		µA
V_{VUVLO_G2VCC}	Undervoltage Lockout Threshold	G2V_{CC} Falling, Respect to G2RTN			3.4		V
		Hysteresis			0.3		V
Input Signal (G1IN, G2IN)							
$V_{IH(G1IN)}$	G1 Turn-On Input Threshold	G1IN Rising				1.75	V
$V_{IL(G1IN)}$	G1 Turn-Off Input Threshold	G1IN Falling		0.5			V
$V_{IH(G2IN)}$	G2 Turn-On Input Threshold	G2IN Rising				1.75	V
$V_{IL(G2IN)}$	G2 Turn-Off Input Threshold	G2IN Falling		0.5			V
R_{DOWN_G1IN}	G1IN Internal Pull-Down Resistor				1000		kΩ
R_{DOWN_G2IN}	G2IN Internal Pull-Down Resistor				1000		kΩ
FAULT ($\overline{FLT}$)							
R_{FLTb}	$\overline{FLT}$ Pin Pull-Down Resistor				60		Ω
t_{FLTb}	$\overline{FLT}$ Pin Delay	Low to High			100		µs
Gate Driver Output (G1)							
$V_{OH(G1)}$	G1 High Output Voltage	I_{G1} = –100mA, $V_{OH(G1)}$ = V_{G1VCC} – V_{G1}			150		mV
$V_{OL(G1)}$	G1 Low Output Voltage	I_{G1} = 100mA, $V_{OL(G1)}$ = V_{G1} – V_{G1RTN}			80		mV
R_{G1_UP}	G1 Pull-Up Resistance	$V_{G1VCC–G1RTN}$ =10V			1.5		Ω
R_{G1_DOWN}	G1 Pull-Down Resistance	$V_{G1VCC–G1RTN}$ =10V			0.8		Ω

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{CC} = V_{G1VCC} = V_{G2VCC} =10V, V_{G1RTN} = V_{G2RTN} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Gate Driver Output (G2)							
$V_{OH(G2)}$	G2 High Output Voltage	I_{G2} = –100mA, $V_{OH(G2)}$ = V_{G2Vcc} – V_{G2}			150		mV
$V_{OL(G2)}$	G2 Low Output Voltage	I_{G2} = 100mA, $V_{OL(G2)}$ = V_{G2} – V_{G2RTN}			80		mV
R_{G2_UP}	G2 Pull-Up Resistance	$V_{G2VCC–G2RTN}$ =10V			1.5		Ω
R_{G2_DOWN}	G2 Pull-Down Resistance	$V_{G2VCC–G2RTN}$ =10V			0.8		Ω
Switching Time							
$t_{PDLH(G1)}$	G1IN High to G1 High Propagation Delay				20		ns
$t_{PDHL(G1)}$	G1IN Low to G1 Low Propagation Delay				20		ns
$t_{PDLH(G2)}$	G2IN High to G2 High Propagation Delay				21		ns
$t_{PDHL(G2)}$	G2IN Low to G2 Low Propagation Delay				21		ns
$tr_{(G2)}$	G2 Output Rise Time	10% – 90%, C_{LOAD} = 3nF			18		ns
$tf_{(G2)}$	G2 Output Fall Time	10% – 90%, C_{LOAD} = 3nF			14		ns
$tr_{(G1)}$	G1 Output Rise Time	10% – 90%, C_{LOAD} = 3nF			18		ns
$tf_{(G1)}$	G1 Output Fall Time	10% – 90%, C_{LOAD} = 3nF			14		ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC7062E is guaranteed to meet performance specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC7062I is guaranteed over the –40°C to 125°C operation junction temperature range. The LTC7062J and LTC7062H are guaranteed over the –40°C to 150°C operation junction temperature range. High junction temperature degrades operation lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environment factors.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation PD according to the following formula.

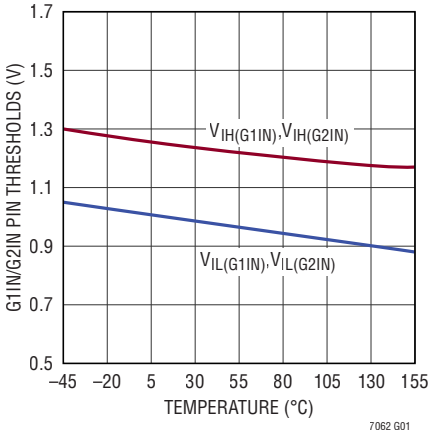
$$T_J = T_A + (P_D \bullet 40\ °C/W)$$

Note 4: The total current includes both the current from $G1V_{CC}$/$G2V_{CC}$ to G1RTN/G2RTN and the current to SGND. Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

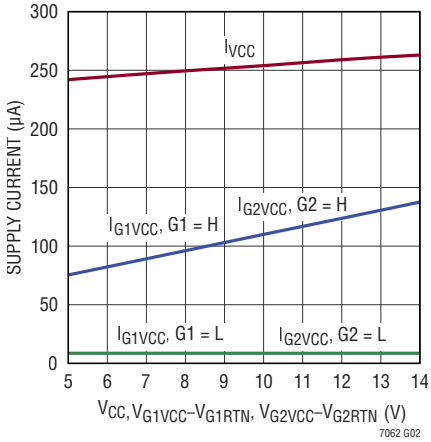
Note 5: Rise and fall times are measured using 10% and 90% levels.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

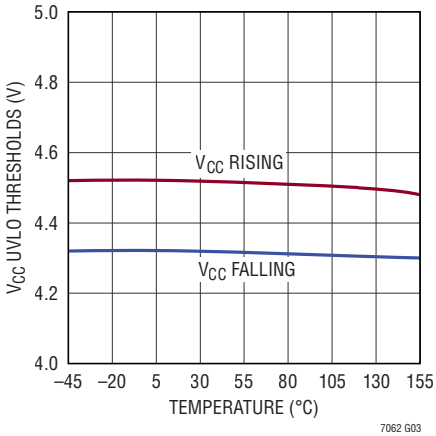
G1IN/G2IN Pin Thresholds vs Temperature



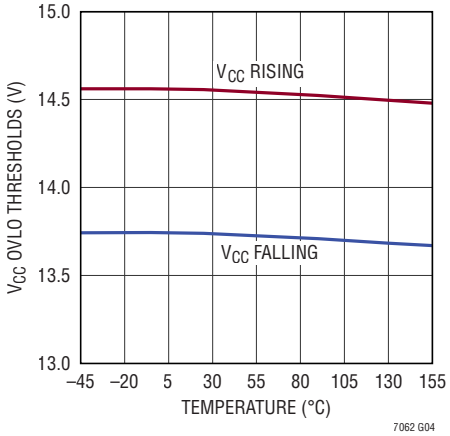
Quiescent Supply Current vs Supply Voltage



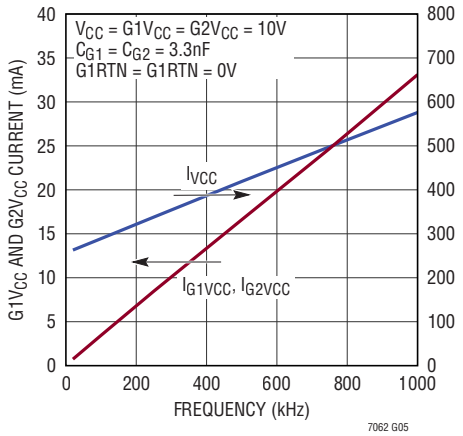
V_{CC} Undervoltage Lockout Thresholds vs Temperature



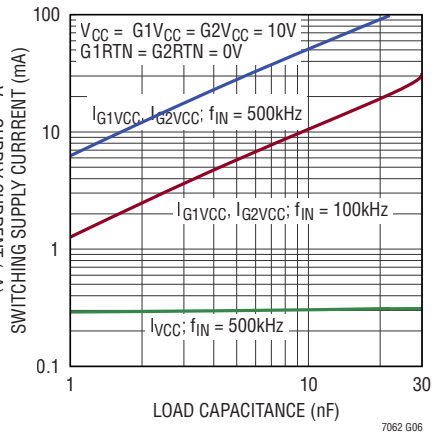
V_{CC} Overvoltage Lockout Thresholds vs Temperature



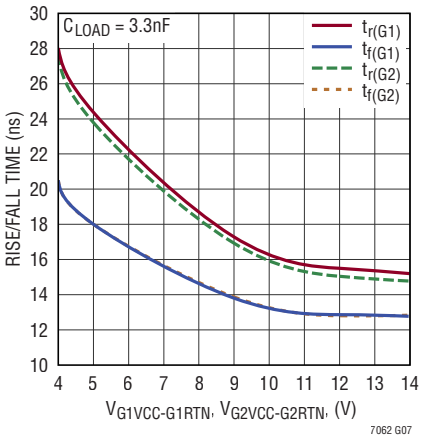
Supply Current vs Input Frequency



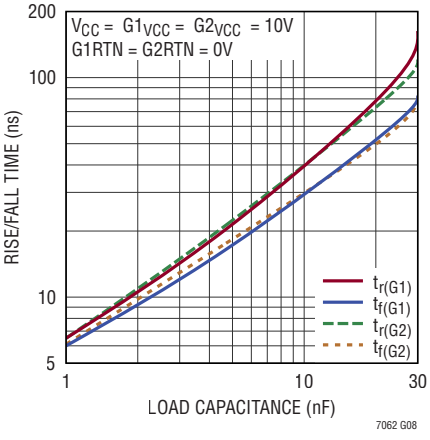
Switching Supply Current vs Load Capacitance



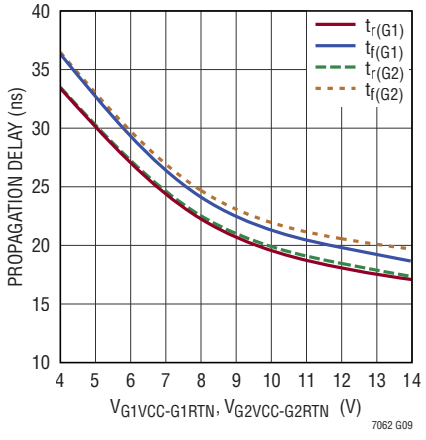
Rise and Fall Time vs Floating Supply Voltage



Rise and Fall Time vs Load Capacitance

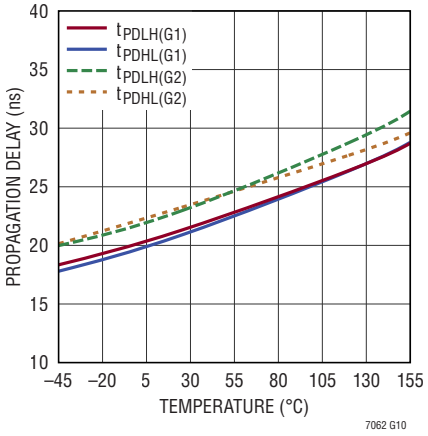


Propagation Delay vs Floating Supply Voltage

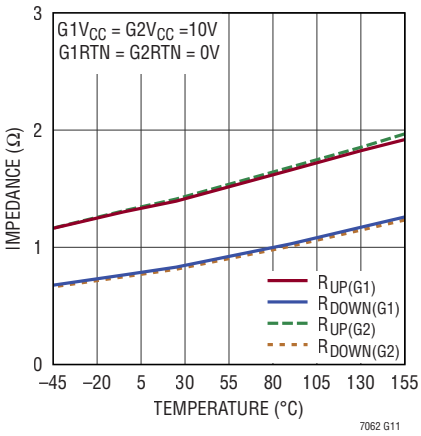


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

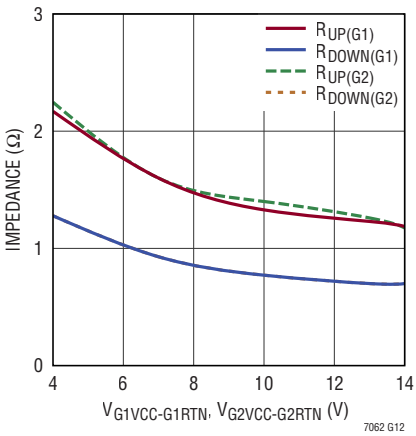
Propagation Delay vs Temperature



G1/G2 Pull-Up and Pull-Down Resistance vs Temperature



G1/G2 Pull-Up and Pull-Down Resistance vs Floating Supply Voltage



PIN FUNCTIONS

V_{CC}: V_{CC} Supply. IC bias supply referred to the SGND pin. An internal 4.5V supply is generated from the V_{CC} supply to bias all the internal circuitry. A bypass capacitor with a minimum value of 0.1µF should be tied between this pin and the SGND pin.

$G2V_{CC}$: G2 MOSFET Driver Supply. The G2 MOSFET gate driver is biased between this pin and G2RTN pin. An external capacitor should be tied between this pin and G2RTN and placed close to the IC.

G2RTN: G2 MOSFET Driver Return. The G2 gate driver is biased between $G2V_{CC}$ and G2RTN. Kelvin connect G2RTN to the G2 MOSFET source pin for high noise immunity. The voltage difference between the G2RTN pin and the SGND can be –10V to 100V.

G2: G2 MOSFET Gate Driver Output. This pin drives the gate of the N-channel MOSFET between G2RTN and $G2V_{CC}$.

$G1V_{CC}$: G1 MOSFET Driver Supply. The G1 MOSFET gate driver is biased between this pin and the G1RTN pin. An external capacitor should be tied between this pin and the G1RTN pin and placed close to the IC.

G1RTN: G1 MOSFET Driver Return. The G1 gate driver is biased between $G1V_{CC}$ and G1RTN. Kelvin connect G1RTN to the G1 MOSFET source pin for high noise immunity. The voltage difference between the G1RTN pin and SGND can be –10V to 100V.

G1: G1 MOSFET Gate Driver Output. This pin drives the gate of the N-channel MOSFET between G1RTN and $G1V_{CC}$.

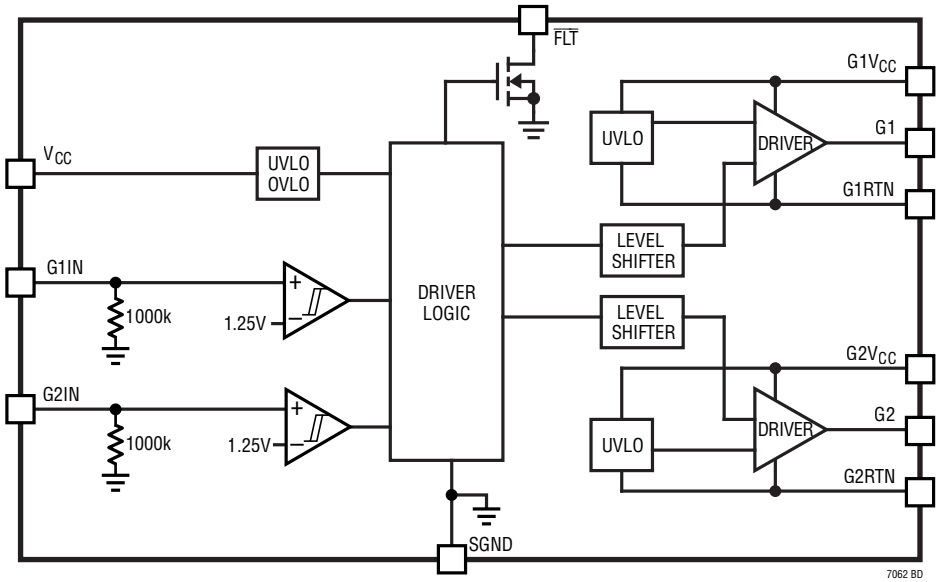
G1IN: Logic input for G1-side driver. If G1IN is unbiased or floating, G1 is held low.

G2IN: Logic input for G2-side driver. If G2IN is unbiased or floating, G2 is held low.

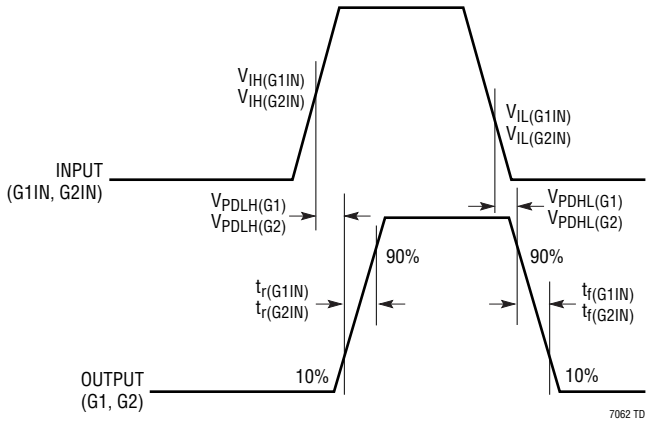
$\overline{FLT}$: Open Drain Fault Output pin referred to the SGND pin. Open-drain output that pulls to SGND during V_{CC} UVLO/OVLO and floating supplies UVLO condition. The typical pull-down resistor is 60Ω.

SGND: Chip Ground. The exposed pad must be soldered to the PCB ground for electrical contact and for rated thermal performance.

BLOCK DIAGRAM



TIMING DIAGRAM



OPERATION

Overview

The LTC7062 has two ground-referenced, low voltage digital signal inputs to drive two N-channel high-side power MOSFETs. The output G2 is driven high or low, swinging between $G2V_{CC}$ and G2RTN, depending on the G2IN pin. Similarly, the output G1 is swinging between $G1V_{CC}$ and G1RTN. Each channel is controlled by its input pints (G1IN and G2IN), allowing independent flexibility to control on and off state of the output.

Both the G1 and G2 drivers are high-side gate drivers. LTC7062 features robust drive with excellent noise and transient immunity, including large negative ground difference tolerance (–10V) on switch node (G1RTN, G2RTN). The two drivers are symmetric and independent of each other, allowing G1 and G2 complementary or non-complementary switching.

V_{CC} Supply

V_{CC} is the power supply for the LTC7062's internal circuitry. An internal 4.5V supply is generated from the V_{CC} supply to bias all the internal circuits referred to SGND. The V_{CC} pin may be tied to the $G2V_{CC}$ pin if SGND and G2RTN are at the same potential. V_{CC} is independent of V_{IN}.

Input Stage (G1IN, G2IN)

The LTC7062 employs two logic inputs with fixed transition thresholds. When the voltage on G1IN is greater than the threshold $V_{IH(G1IN)}$, G1 is pulled up to $G1V_{CC}$, turning the external MOSFET on. This MOSFET will stay on until G1IN falls below $V_{IL(G1IN)}$. Similarly, when G2IN is greater than $V_{IH(G2IN)}$, G2 is pulled up to $G2V_{CC}$, turning the external MOSFET on. G2 will stay high until G2IN falls below the threshold $V_{IL(G2IN)}$.

The hysteresis between the corresponding V_{IH} and V_{IL} voltage levels eliminates false triggering due to the noise during switch transitions. However, care should be taken to keep noise from coupling into the input pins (G1IN, G2IN), particularly in high frequency, high voltage applications.

When G1IN/G2IN pin is floating, there is an internal 1000k pull-down resistor from the G1IN/G2IN pin to SGND, keeping the G1/G2 default state low if the input is not driven.

Both G1IN and G2IN pin can be used by the controller IC to perform the Discontinuous Conduction Mode (DCM) in switching regulator applications.

Output Stage

A simplified version of the LTC7062's output stage is shown in Figure 1. Both G1 and G2 designs are symmetrical and have floating gate-driver outputs. The pull-up device is a P-channel MOSFET with a typical 1.5Ω $R_{DS(ON)}$ and the pull-down device is a N-channel MOSFET with a typical 0.8Ω $R_{DS(ON)}$. The wide driver supply voltage ranging from 4V to 14V enables driving different power MOSFETs, such as logic level or high threshold MOSFETs. However, LTC7062 is optimized for high threshold MOSFETs (e.g., $G1V_{CC}$ – G1RTN = 10V and $G2V_{CC}$ – G2RTN = 10V). The driver output pull-up and pull-down resistance may increase with lower driver supply voltage.

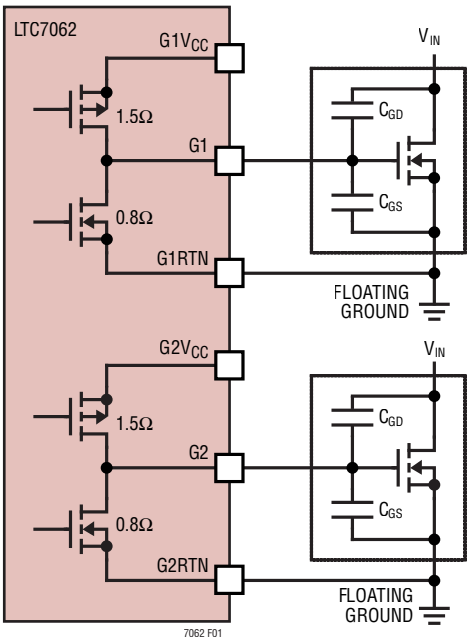


Figure 1. Simplified Output Stage

OPERATION

Since the power MOSFETs generally account for the majority of the power loss in a converter, it is important to turn them on and off quickly, thereby minimizing the transition time and power loss. The LTC7062's typical 1.5Ω pull-up resistance and 0.8Ω pull-down resistance are equivalent to 3A peak pull-up current and 6A peak pull down current at a 10V driver supply. Both G2 and G1 can produce a rapid turn-on transition for the MOSFETs with capability of driving a 3nF load with 18ns rise time.

Protection Circuitry

When using the LTC7062, care must be taken not to exceed any of the Absolute Maximum Ratings. As an added safeguard, the LTC7062 incorporates an overtemperature shutdown feature. If the junction temperature reaches approximately 180°C, the LTC7062 will enter thermal shutdown mode and G2 will be pulled to G2RTN; G1 will be pulled to G1RTN. Normal operation will resume when the junction temperature cools to be less than 165°C. The overtemperature level is not production tested. The LTC7062 is guaranteed to operate at temperatures below 150°C.

The LTC7062 contains both undervoltage and overvoltage lockout detectors that monitor the V_{CC} supply. When V_{CC} falls below 4.3V or rises above 14.6V, the output pins G2 and G1 are pulled to G2RTN and G1RTN, respectively. This turns off both the external MOSFETs. When V_{CC} has adequate supply voltage but less than the overvoltage threshold, normal operation will resume.

Additional undervoltage lockout circuitry is included in each floating driver supply. The G2 will be pulled down to G2RTN when the floating voltage from $G2V_{CC}$ to G2RTN falls below 3.3V. Similarly, the G1 will be pulled down to G1RTN when the floating voltage from $G1V_{CC}$ to G1RTN is less than 3.3V.

The normal operation and undervoltage/overvoltage logic table is shown in Table 1.

Table 1. Normal Operation and Undervoltage/Overvoltage Logic

G1IN	G2IN	V_{CC} UVLO or OVLO	($G1V_{CC}$– G1RTN) UVLO	($G2V_{CC}$– G2RTN) UVLO	Thermal Shutdown	G1	G2	FLTB
X	X	X	X	X	Yes	L	L	L
X	X	Yes	X	X	No	L	L	L
X	H	No	Yes	N	No	L	H	L
H	X	No	No	Yes	No	H	L	L
L	H	No	No	No	No	L	H	H
H	L	No	No	No	No	H	L	H
H	H	No	No	No	No	H	H	H
L	L	No	No	No	No	L	L	H

Note: "X" means "Don't Care", "H" means "High", and "L" means "Low".

FAULT FLAG

$\overline{FLT}$ pin is connected to the open-drain of an internal N-channel MOSFET. It needs a pull-up resistor (e.g. 51k) tied to a supply such as V_{CC} or any other bias voltage up to 15V. The $\overline{FLT}$ pin is pulled low to SGND immediately if any of these conditions are met:

a. The V_{CC} is below its UVLO threshold or above its OVLO threshold.

b. ($G2V_{CC}$ – G2RTN) is below its UVLO threshold.

c. ($G1V_{CC}$ – G1RTN) is below its UVLO threshold.

d. The junction temperature reaches approximately 180°C.

When all the faults are cleared, $\overline{FLT}$ pin is pulled up by the external resistor after a built-in 100µs delay.

APPLICATIONS INFORMATION

Bootstrapped Supply ($G2V_{CC}$ – G2RTN, $G1V_{CC}$ – G1RTN)

Either or both of the $G2V_{CC}$ – G2RTN and $G1V_{CC}$ – G1RTN supplies can be bootstrapped supplies. An external boost capacitor, C_B, connected between $G2V_{CC}$ and G2RTN, or between $G1V_{CC}$ and G1RTN, supplies the gate driver voltage for its respective MOSFET driver. When the external MOSFET is turned on, the driver places the C_B voltage across the gate-source of the MOSFET. This enhances the MOSFET and turns it on.

The charge to turn on the external MOSFET is referred to gate charge, Q_G, and is typically specified in the external MOSFET data sheet. The boost capacitor, C_B, needs to have at least 10 times the gate charge to turn on the external MOSFET fully. Gate charge can range from 5nC to hundreds of nC and is influenced by the gate drive level and type of external MOSFET used. For most applications, a capacitor value of 0.1µF for C_B will be sufficient. However, if multiple MOSFETs are paralleled and drove by the LTC7062, C_B needs to be increased correspondingly and the following relationship for the C_B should be maintained:

$$C_B > \frac{10 \bullet \text{External MOSFET } Q_G}{1V}$$

An external supply, typically V_{CC} connected through a Schottky diode, is required to keep the C_B charged. The LTC7062 does not charge the C_B and always discharges the C_B. When the G2/G1 is high, the total current from $G2V_{CC}$/$G1V_{CC}$ to G2RTN/G1RTN and SGND is typically 146µA; when the G2/G1 is low, the total current from $G2V_{CC}$/$G1V_{CC}$ is typically 9µA.

POWER DISSIPATION

To ensure proper operation and long-term reliability, the LTC7062 must not operate beyond its maximum temperature rating. Package junction temperature can be calculated by:

$$T_J = T_A + (P_D)(\theta_{JA})$$

where:

T_J = junction temperature

T_A = ambient temperature

P_D = power dissipation

θ_{JA} = junction-to-ambient thermal resistance

Power dissipation consists of standby, switching and capacitive load power losses:

$$P_D = P_{DC} + P_{AC} + P_{QG}$$

where:

P_{DC} = quiescent power loss

P_{AC} = internal switching loss at input frequency f_{IN}

P_{QG} = loss due to turning on and off external MOSFET with gate charge Q_G at frequency f_{IN}

The LTC7062 consumes very little quiescent current. The DC power loss at V_{CC} = 10V is only (10V)(0.3mA) = 3mW.

At a particular switching frequency, the internal power loss increases due to both AC currents required to charge and discharge internal nodal capacitances and cross-conduction currents in the internal logic gates. The sum of the quiescent current and internal switching current with no load are shown in the Typical Performance Characteristics plot of Switching Supply Current vs Load Capacitance.

The gate charge losses are primarily due to the large AC currents required to charge and discharge the capacitance of the external MOSFETs during switching. For identical pure capacitive loads C_{LOAD} on BG and TG at switching frequency f_{IN}, the load losses would be:

$$P_{CLOAD}=(C_{LOAD})(f_{IN})[(V_{G1VCC-G1RTN})^2+(V_{G2VCC-G2RTN})^2]$$

In a typical synchronous buck configuration, the V_{CC} is connected to the power for the bottom MOSFET driver, $G2V_{CC}$. $V_{G1VCC–G1RTN}$ is equal to V_{CC} – V_D, where V_D is the forward voltage drop of the external Schottky diode between V_{CC} and $G1V_{CC}$. If this drop is small relative V_{CC}, the load losses can be approximated as:

$$P_{CLOAD} \approx 2(C_{LOAD})(f_{IN})(V_{CC})^2$$

APPLICATIONS INFORMATION

Unlike a pure capacitive load, a power MOSFET's gate capacitance seen by the driver output varies with its V_{GS} voltage level during switching. A MOSFET's capacitive load power dissipation can be calculated using its gate charge, Q_G. The Q_G value corresponding to the MOSFET's V_{GS} value (V_{CC} in this case) can be readily obtained from the manufacturer's Q_G vs V_{GS} curves. For identical MOSFETs on G2 and G1:

$$P_{QG} \approx 2(Q_G)(f_{IN})(V_{CC})$$

BYPASSING AND GROUNDING

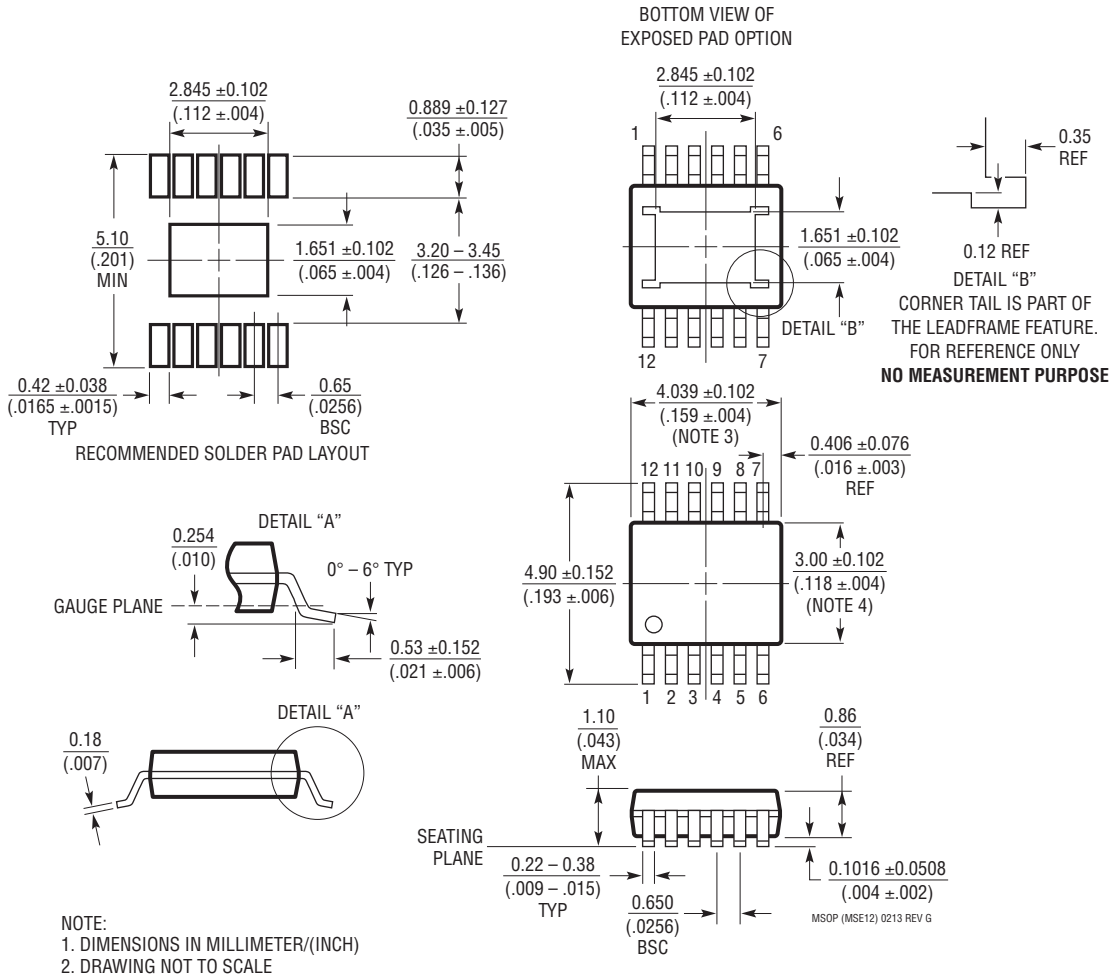
The LTC7062 requires proper bypassing on the V_{CC}, $V_{G1VCC-G1RTN}$ and $V_{G2VCC-G2RTN}$ supplies due to its high speed Switching (nanoseconds) and large AC currents (amperes). Careless component placement and PCB trace routing may cause excessive ringing and under/overshoot.

To obtain the optimum performance form the LTC7062:

- Mount the bypass capacitors as close as possible between the V_{CC} and SGND pins, the $G2V_{CC}$ and G2RTN pins, and the $G1V_{CC}$ and G1RTN pins. The leads should be shortened as much as possible to reduce lead inductance.
- Use a low inductance, low impedance ground place to reduce any ground drop and stray capacitance. Remember that the LTC7062 switches greater than 5A peak currents and any significant ground drop will degrade signal integrity.
- Plan the power/ground routing carefully. Know where the large load switching current is coming from and going to. Maintain separate ground return paths for the input pin and the output power stage.
- Kelvin connect the G1 pin to the G1 MOSFET gate and G1RTN pin to the G1 MOSFET source. Kelvin connect the G2 pin to the G2 MOSFET gate and G2RTN to the G2 MOSFET source. Keep the copper trace between the driver output pin and load short and wide.
- Be sure to solder the Exposed Pad on the back side of the LTC7062 packages to the board. Failure to make good thermal contact between the exposed back side and the copper board will result in thermal resistances far greater than specified for the packages.

PACKAGE DESCRIPTION

MSE Package
12-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1666 Rev G)



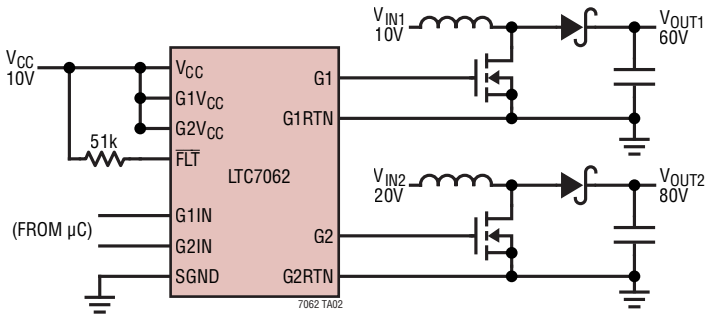
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	08/21	Fixed typo in Overview section.	9
B	11/22	Removed the G2VCC to FLT connection	14

TYPICAL APPLICATION

Dual Outputs Boost Converters



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC7060	100V Half-Bridge Driver with Floating Grounds and Programmable Dead-Time	Up to 100V Supply Voltage, 6V ≤ V_{CC} ≤ 14V, 0.8Ω Pull-Down, 1.5Ω Pull-Up, Symmetric Floating Gate Driver Architecture, Adjustable Dead-Time from 31ns to 76ns
LTC7061	100V Half-Bridge Gate Driver with Floating Grounds and Adjustable Dead-Time	Up to 100V Supply Voltage, 5V ≤ V_{CC} ≤ 14V, 0.8Ω Pull-Down, 1.5Ω Pull-Up, Two Inputs, Symmetric Floating Gate Driver Architecture, Adjustable Dead-Time from 31ns to 76ns
LTC7063	150V Half-Bridge Driver with Floating Grounds and Programmable Dead-Time	Up to 150V Supply Voltage, 6V ≤ V_{CC} ≤ 14V, 0.8Ω Pull-Down, 1.5Ω Pull-Up, Symmetric Floating Gate Driver Architecture, Adjustable Dead-Time from 31ns to 76ns
LTC4449	High Speed Synchronous N-Channel MOSFET Driver	Up to 38V Supply Voltage, 4V ≤ V_{CC} ≤ 6.5V, Adaptive Shoot-Through Protection, 2mm × 3mm DFN-8
LTC4442/ LTC4442-1	High Speed Synchronous N-Channel MOSFET Driver	Up to 38V Supply Voltage, 6V ≤ V_{CC} ≤ 9.5V, 2.4A Peak Pull-Up/5A Peak Pull-Down
LTC4444/ LTC4444-5	High Voltage Synchronous N-Channel MOSFET driver with Shoot-Through Protection	Up to 100V Supply Voltage, 4.5V/7.2V ≤ V_{CC} ≤ 13.5V, 3A Peak Pull-Up/0.55Ω Peak Pull-Down
LTC7851	Quad Output, Multiphase, Step-Down Voltage Mode DC/DC Controller with Accurate Current Sharing	Operates with Power Block, DrMOS or External Drivers and MOSFETs, 3V ≤ V_{IN} ≤ 24V
LTC3861	Dual, Multiphase, Step-Down Voltage Mode DC/DC Controller with Accurate Current Sharing	Operates with Power Block, DrMOS or External Gate Driver and MOSFETs, 3V ≤ V_{IN} ≤ 24V
LTC3774	Dual, Multiphase, Current Mode Synchronous Step-Down DC/DC Controller for Sub-Milliohm DCR Sensing	Operates with DrMOS, Power Blocks or External Drivers/MOSFETs, 4.5V ≤ V_{IN} ≤ 38V, 0.6V ≤ V_{OUT} ≤ 3.5V