



**SN54147, SN54148, SN54LS147, SN54LS148**  
**SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148**  
**10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS**

SDLS053B – OCTOBER 1976 – REVISED MAY 2004

**description/ordering information**

These TTL encoders feature priority decoding of the inputs to ensure that only the highest-order data line is encoded. The '147 and 'LS147 devices encode nine data lines to four-line (8-4-2-1) BCD. The implied decimal zero condition requires no input condition, as zero is encoded when all nine data lines are at a high logic level. The '148 and 'LS148 devices encode eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input EI and enable output EO) has been provided to allow octal expansion without the need for external circuitry. For all types, data inputs and outputs are active at the low logic level. All inputs are buffered to represent one normalized Series 54/74 or 54/74LS load, respectively.

**ORDERING INFORMATION**

T <sub>A</sub>	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74LS148N	SN74LS148N
	SOIC – D	Tube	SN74LS148D	LS148
		Tape and reel	SN74LS148DR	
	SOP – NS	Tape and reel	SN74LS148NSR	74LS148
–55°C to 125°C	CDIP – J	Tube	SNJ54LS148J	SNJ54LS148J
	CFP – W	Tube	SNJ54LS148W	SNJ54LS148W
	LCCC – FK	Tube	SNJ54LS148FK	SNJ54LS148FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

**FUNCTION TABLE – '147, 'LS147**

INPUTS									OUTPUTS			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	L	H	H	H	H	H	L	L	H
X	X	X	L	H	H	H	H	H	H	L	H	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

H = high logic level, L = low logic level, X = irrelevant



**SN54147, SN54148, SN54LS147, SN54LS148**  
**SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148**  
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FUNCTION TABLE – '148, 'LS148

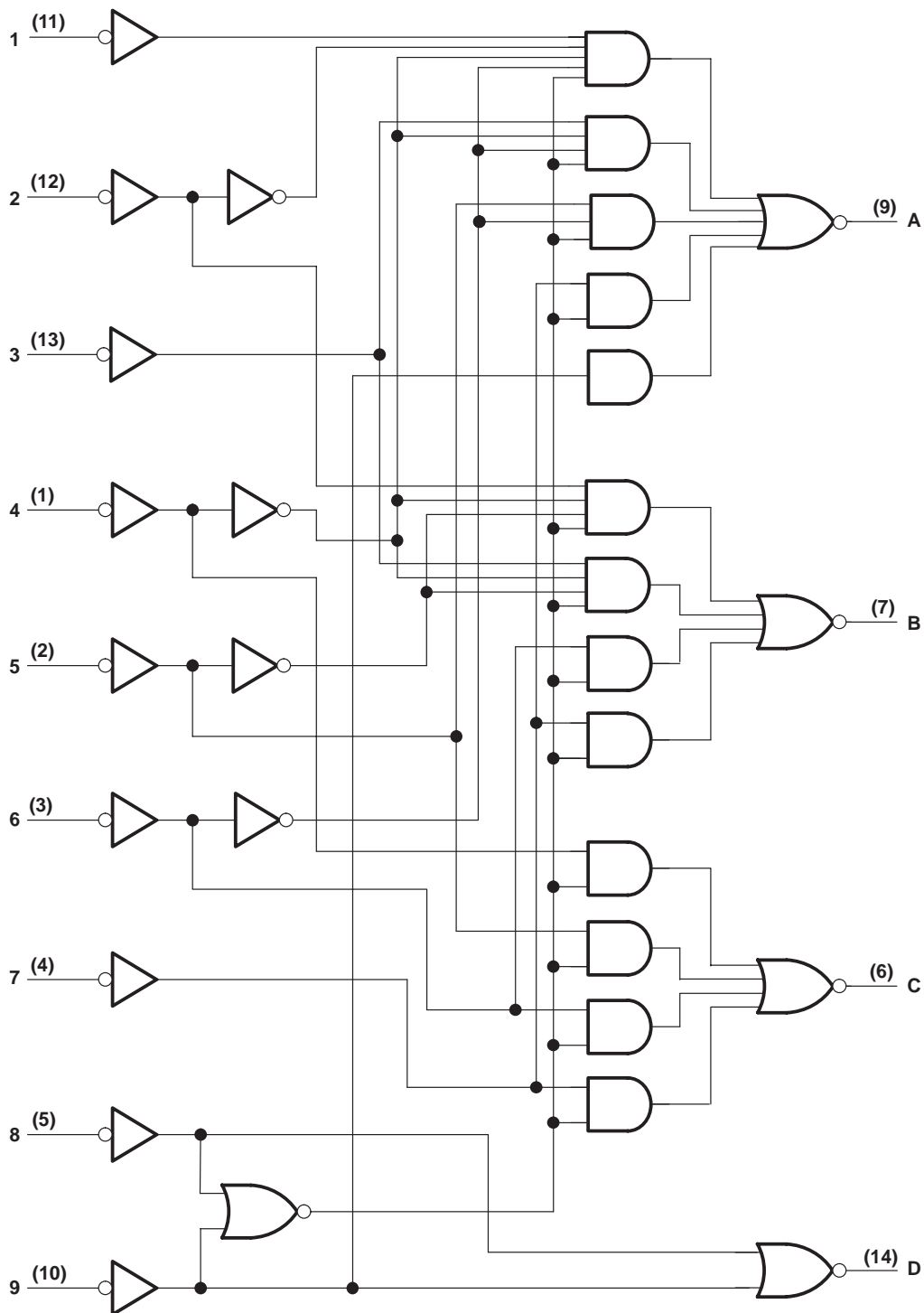
EI	INPUTS								OUTPUTS				
	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	L	H	H	H	H	L	H	H	L	H
L	X	X	L	H	H	H	H	H	H	L	L	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

H = high logic level, L = low logic level, X = irrelevant

**SN54147, SN54148, SN54LS147, SN54LS148  
 SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148  
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**'147, 'LS147 logic diagram (positive logic)**



Pin numbers shown are for D, J, N, and W packages.

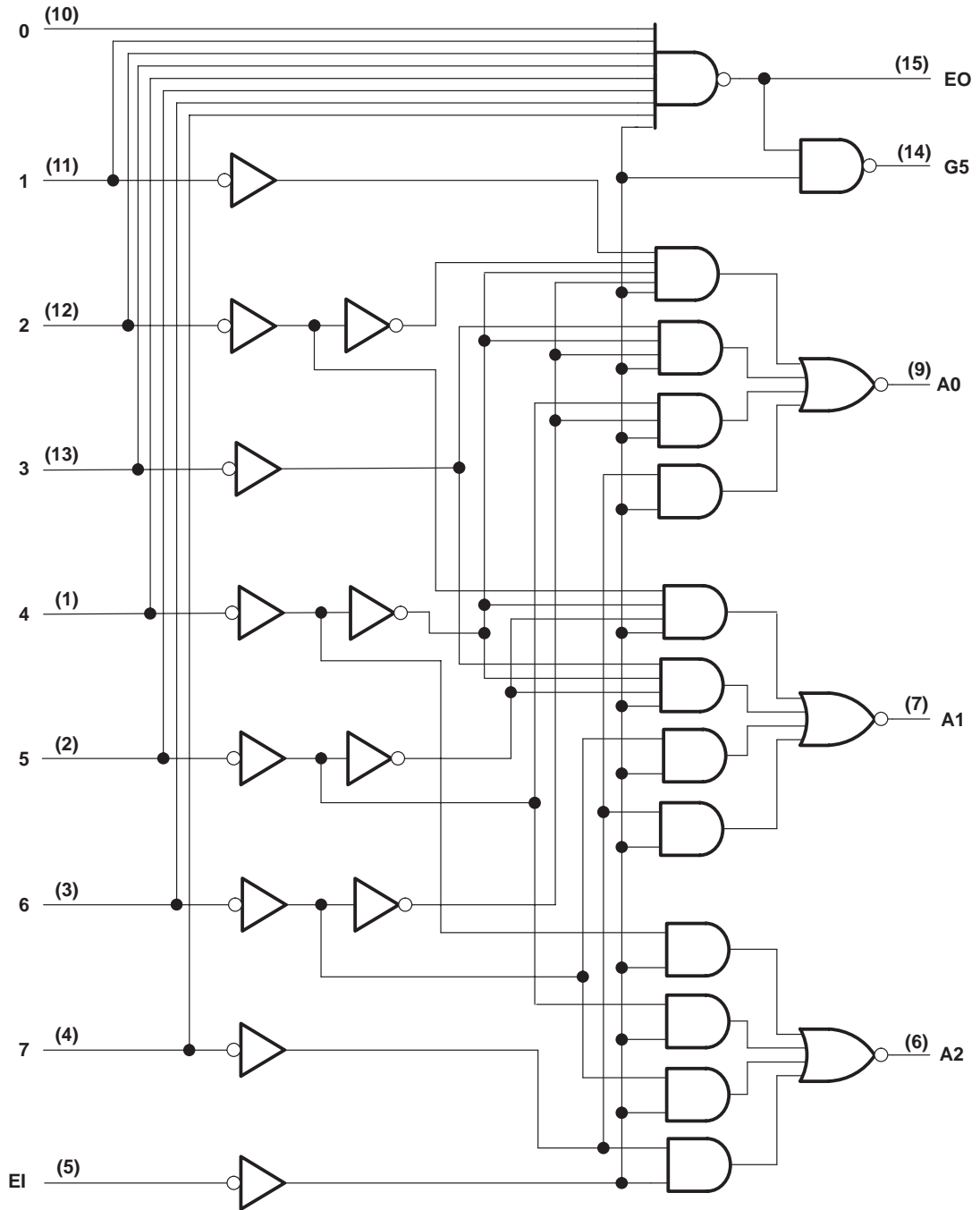


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**SN54147, SN54148, SN54LS147, SN54LS148  
SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148  
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'148, 'LS148 logic diagram (positive logic)



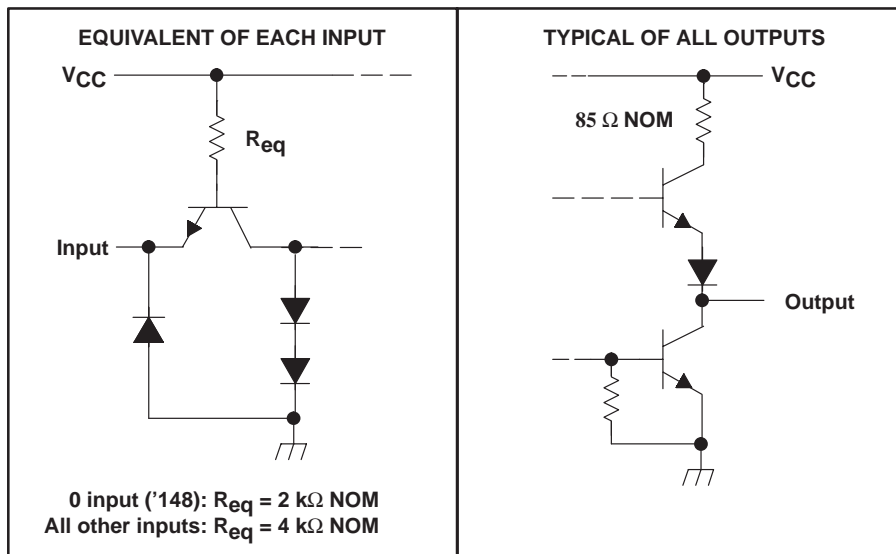
Pin numbers shown are for D, J, N, NS, and W packages.

**SN54147, SN54148, SN54LS147, SN54LS148  
 SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148  
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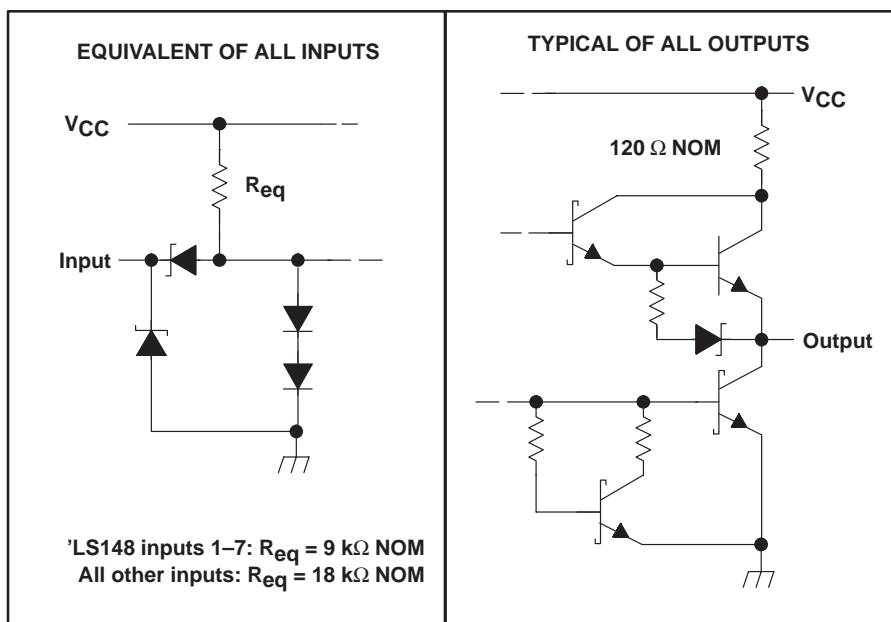
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**schematics of inputs and outputs**

'147, '148



'LS147, 'LS148



**SN54147, SN54148, SN54LS147, SN54LS148  
SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148  
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**absolute maximum ratings over operating free-air temperature (unless otherwise noted)†**

Supply voltage, $V_{CC}$ (see Note 1) .....	7 V
Input voltage, $V_I$ : '147, '148 .....	5.5 V
'LS147, 'LS148 .....	7 V
Inter-emitter voltage: '148 only (see Note 2) .....	5.5 V
Package thermal impedance $\theta_{JA}$ (see Note 3): D package .....	73°C/W
N package .....	67°C/W
NS package .....	64°C/W
Storage temperature range, $T_{Stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Voltage values, except inter-emitter voltage, are with respect to the network ground terminal.  
 2. This is the voltage between two emitters of a multiple-emitter transistor. For '148 circuits, this rating applies between any two of the eight data lines, 0 through 7.  
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions (see Note 4)**

	SN54'			SN74'			SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$ Supply voltage	4.5	5	5.5	4.75	5	5.25	4.5	5	5.5	4.75	5	5.25	V
$I_{OH}$ High-level output current			–800			–800			–400			–400	μA
$I_{OL}$ Low-level output current			16			16			4			8	mA
$T_A$ Operating free-air temperature	–55		125	0		70	–55		125	0		70	°C

NOTE 4: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



**SN54147, SN54148, SN54LS147, SN54LS148  
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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS†	'147			'148			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IH</sub>	High-level input voltage		2			2		V	
V <sub>IL</sub>	Low-level input voltage				0.8		0.8	V	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -12 mA			-1.5		-1.5	V	
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.8 V, V <sub>IH</sub> = 2 V, I <sub>OH</sub> = -800 μA	2.4	3.3		2.4	3.3	V	
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.8 V, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 16 mA		0.2	0.4		0.2	0.4	V
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MIN, V <sub>I</sub> = 5.5 V			1		1	mA	
I <sub>IH</sub>	High-level input current	0 input					40	μA	
		Any input except 0	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V		40		80		
I <sub>IL</sub>	Low-level input current	0 input					-1.6	mA	
		Any input except 0	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V		-1.6		-3.2		
I <sub>OS</sub>	Short-circuit output current§	V <sub>CC</sub> = MAX	-35		-85	-35		mA	
I <sub>CC</sub>	Supply current	V <sub>CC</sub> = MAX (See Note 5)	Condition 1	50	70	40	60	mA	
			Condition 2	42	62	35	55		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time.

NOTE 5: For '147, I<sub>CC</sub> (Condition 1) is measured with input 7 grounded, other inputs and outputs open; I<sub>CC</sub> (Condition 2) is measured with all inputs and outputs open. For '148, I<sub>CC</sub> (Condition 1) is measured with inputs 7 and EI grounded, other inputs and outputs open; I<sub>CC</sub> (Condition 2) is measured with all inputs and outputs open.

**SN54147, SN74147 switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	Any	Any	In-phase output	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 400 Ω		9	14	ns
t <sub>PHL</sub>						7	11	
t <sub>PLH</sub>	Any	Any	Out-of-phase output			13	19	ns
t <sub>PHL</sub>						12	19	





**SN54147, SN54148, SN54LS147, SN54LS148**  
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**SN54148, SN74148 switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (see Figure 1)**

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	1–7	A0, A1, or A2	In-phase output	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 400 Ω	10	15	ns	
t <sub>PHL</sub>								
t <sub>PLH</sub>	1–7	A0, A1, or A2	Out-of-phase output		12	19	ns	
t <sub>PHL</sub>								6
t <sub>PLH</sub>	0–7	EO	Out-of-phase output		14	25	ns	
t <sub>PHL</sub>								18
t <sub>PLH</sub>	0–7	GS	In-phase output		14	25	ns	
t <sub>PHL</sub>								10
t <sub>PLH</sub>	EI	A0, A1, or A2	In-phase output		10	15	ns	
t <sub>PHL</sub>								8
t <sub>PLH</sub>	EI	GS	In-phase output		10	15	ns	
t <sub>PHL</sub>								10
t <sub>PLH</sub>	EI	EO	In-phase output		10	15	ns	
t <sub>PHL</sub>								17

† t<sub>PLH</sub> = propagation delay time, low-to-high-level output.  
t<sub>PHL</sub> = propagation delay time, high-to-low-level output.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS†	SN54LS'		SN74LS'		UNIT		
			MIN	TYP‡	MAX	MIN		TYP‡	MAX
V <sub>IH</sub>	High-level input voltage		2		2		V		
V <sub>IL</sub>	Low-level input voltage			0.7		0.8	V		
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA		-1.5		-1.5	V		
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -400 μA	2.5	3.4	2.7	3.4	V		
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>IL</sub> MAX	I <sub>OL</sub> = 4 mA		0.25	0.4	V		
			I <sub>OL</sub> = 8 mA			0.35		0.5	
I <sub>I</sub>	Input current at maximum input voltage	'LS148 inputs 1–7	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V		0.2		0.2	mA	
		All other inputs			0.1		0.1		
I <sub>IH</sub>	High-level input current	'LS148 inputs 1–7	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V		40		40	μA	
		All other inputs			20		20		
I <sub>IL</sub>	Low-level input current	'LS148 inputs 1–7	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V		-0.8		-0.8	mA	
		All other inputs			-0.4		-0.4		
I <sub>OS</sub>	Short-circuit output current§	V <sub>CC</sub> = MAX	-20	-100	-20	-100	mA		
I <sub>CC</sub>	Supply current	V <sub>CC</sub> = MAX (See Note 6)	Condition 1		12	20	12	20	mA
			Condition 2		10	17	10	17	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time.

NOTE 6: For 'LS147, I<sub>CC</sub> (Condition 1) is measured with input 7 grounded, other inputs and outputs open; I<sub>CC</sub> (Condition 2) is measured with all inputs and outputs open. For 'LS148, I<sub>CC</sub> (Condition 1) is measured with inputs 7 and EI grounded, other inputs and outputs open; I<sub>CC</sub> (Condition 2) is measured with all inputs and outputs open.



**SN54147, SN54148, SN54LS147, SN54LS148**  
**SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148**  
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**SN54LS147, SN74LS147 switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (see Figure 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Any	Any	In-phase output	$C_L = 15\text{ pF}$ , $R_L = 2\text{ k}\Omega$	12	18	ns	
$t_{PHL}$					12	18		
$t_{PLH}$	Any	Any	Out-of-phase output		21	33	ns	
$t_{PHL}$					15	23		

**SN54LS148, SN74LS148 switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (see Figure 2)**

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	1–7	A0, A1, or A2	In-phase output	$C_L = 15\text{ pF}$ , $R_L = 2\text{ k}\Omega$	14	18	ns	
$t_{PHL}$					15	25		
$t_{PLH}$	1–7	A0, A1, or A2	Out-of-phase output		20	36	ns	
$t_{PHL}$					16	29		
$t_{PLH}$	0–7	EO	Out-of-phase output		7	18	ns	
$t_{PHL}$					25	40		
$t_{PLH}$	0–7	GS	In-phase output		35	55	ns	
$t_{PHL}$					9	21		
$t_{PLH}$	EI	A0, A1, or A2	In-phase output		16	25	ns	
$t_{PHL}$					12	25		
$t_{PLH}$	EI	GS	In-phase output		12	17	ns	
$t_{PHL}$					14	36		
$t_{PLH}$	EI	EO	In-phase output		12	21	ns	
$t_{PHL}$					23	35		

†  $t_{PLH}$  = propagation delay time, low-to-high-level output

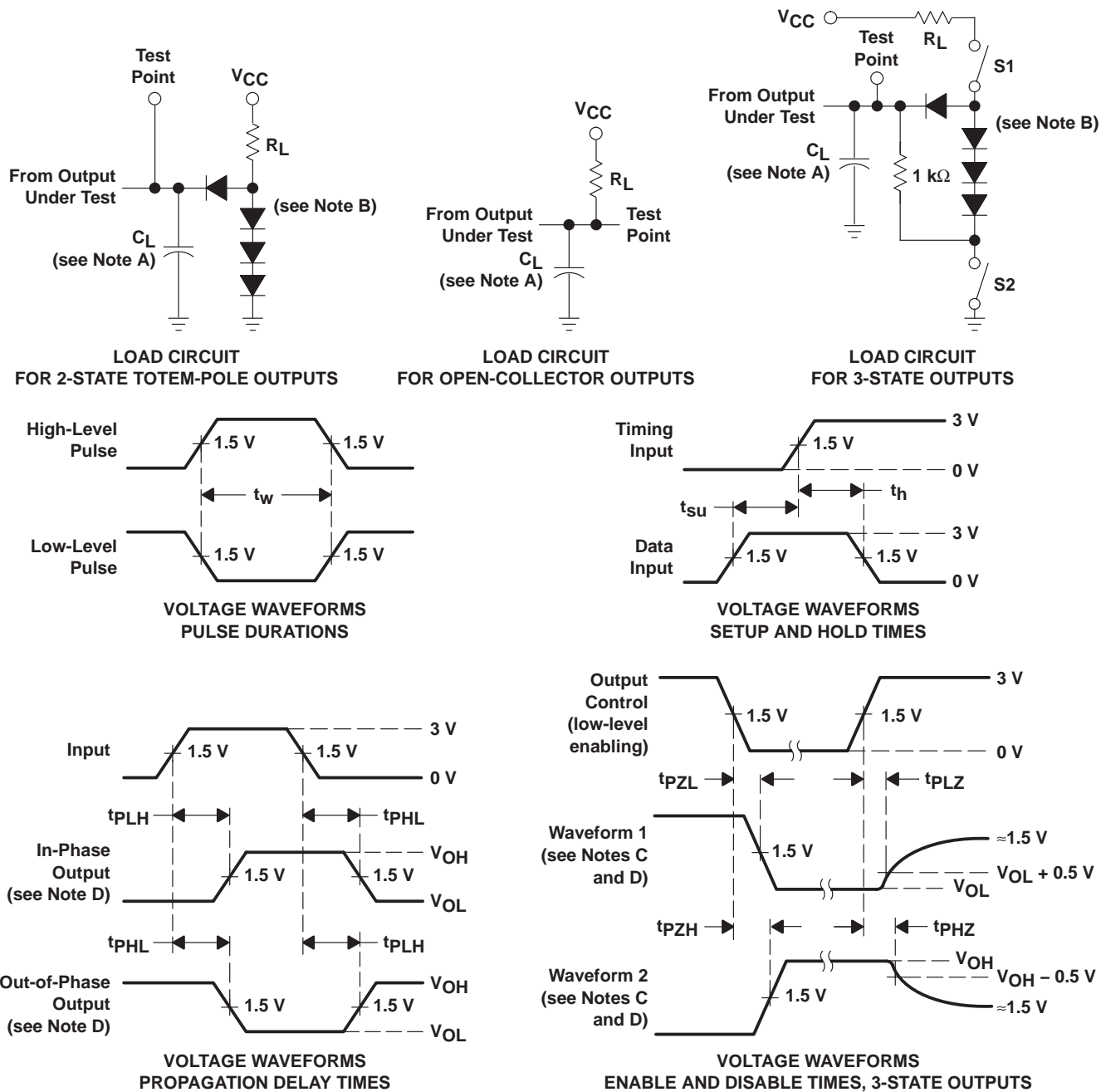
$t_{PHL}$  = propagation delay time, high-to-low-level output



**SN54147, SN54148, SN54LS147, SN54LS148**  
**SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148**  
**10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS**

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**PARAMETER MEASUREMENT INFORMATION**  
**SERIES 54/74 DEVICES**



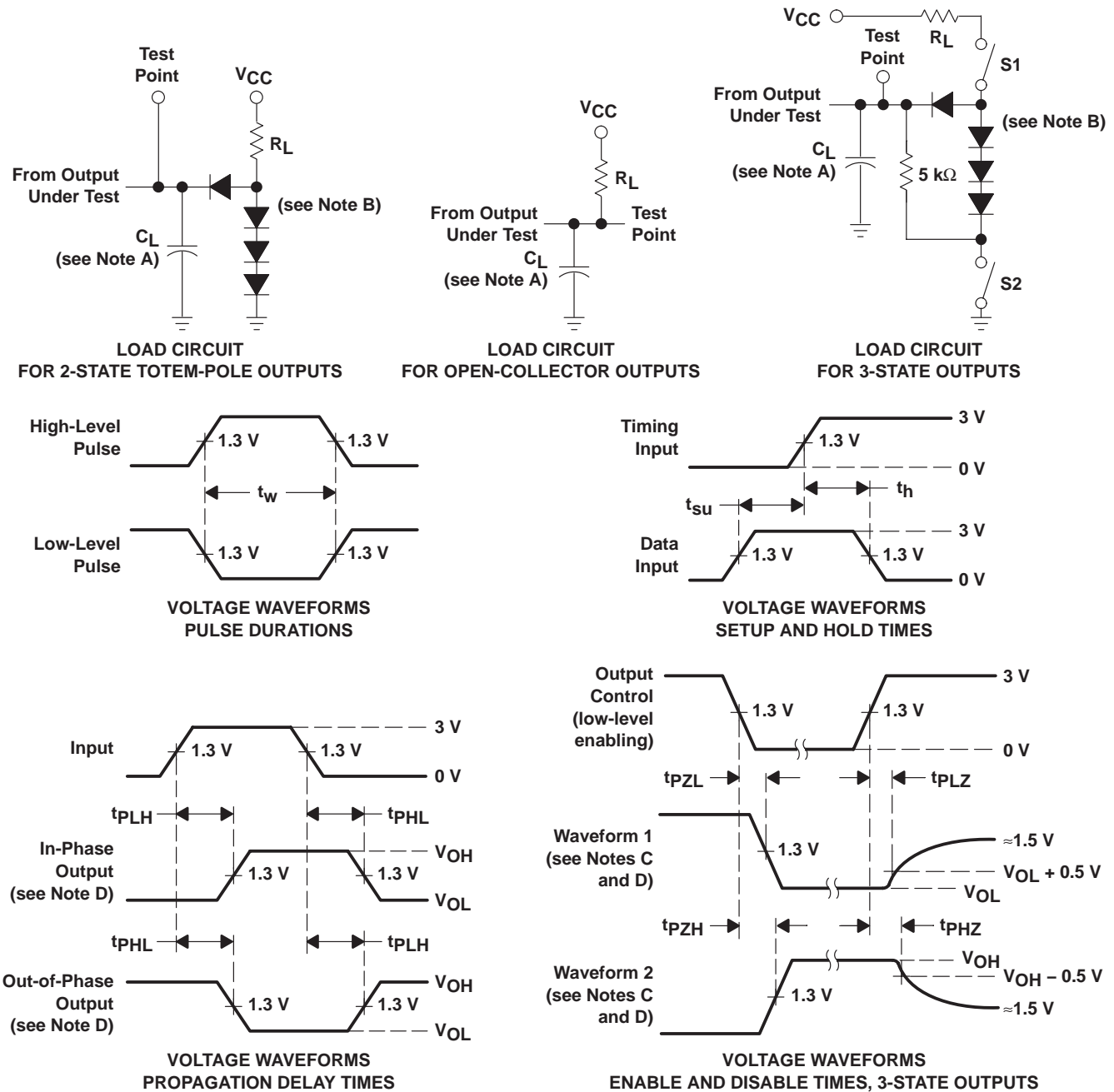
- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. All diodes are 1N3064 or equivalent.
  - C. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - D. S1 and S2 are closed for  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_{PHZ}$ , and  $t_{PLZ}$ ; S1 is open, and S2 is closed for  $t_{PZH}$ ; S1 is closed, and S2 is open for  $t_{PZL}$ .
  - E. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_0 \approx 50 \Omega$ ;  $t_r$  and  $t_f \leq 7$  ns for Series 54/74 devices and  $t_r$  and  $t_f \leq 2.5$  ns for Series 54S/74S devices.
  - F. The outputs are measured one at a time, with one input transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**

**SN54147, SN54148, SN54LS147, SN54LS148  
SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148  
10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS**

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**PARAMETER MEASUREMENT INFORMATION  
SERIES 54LS/74LS DEVICES**



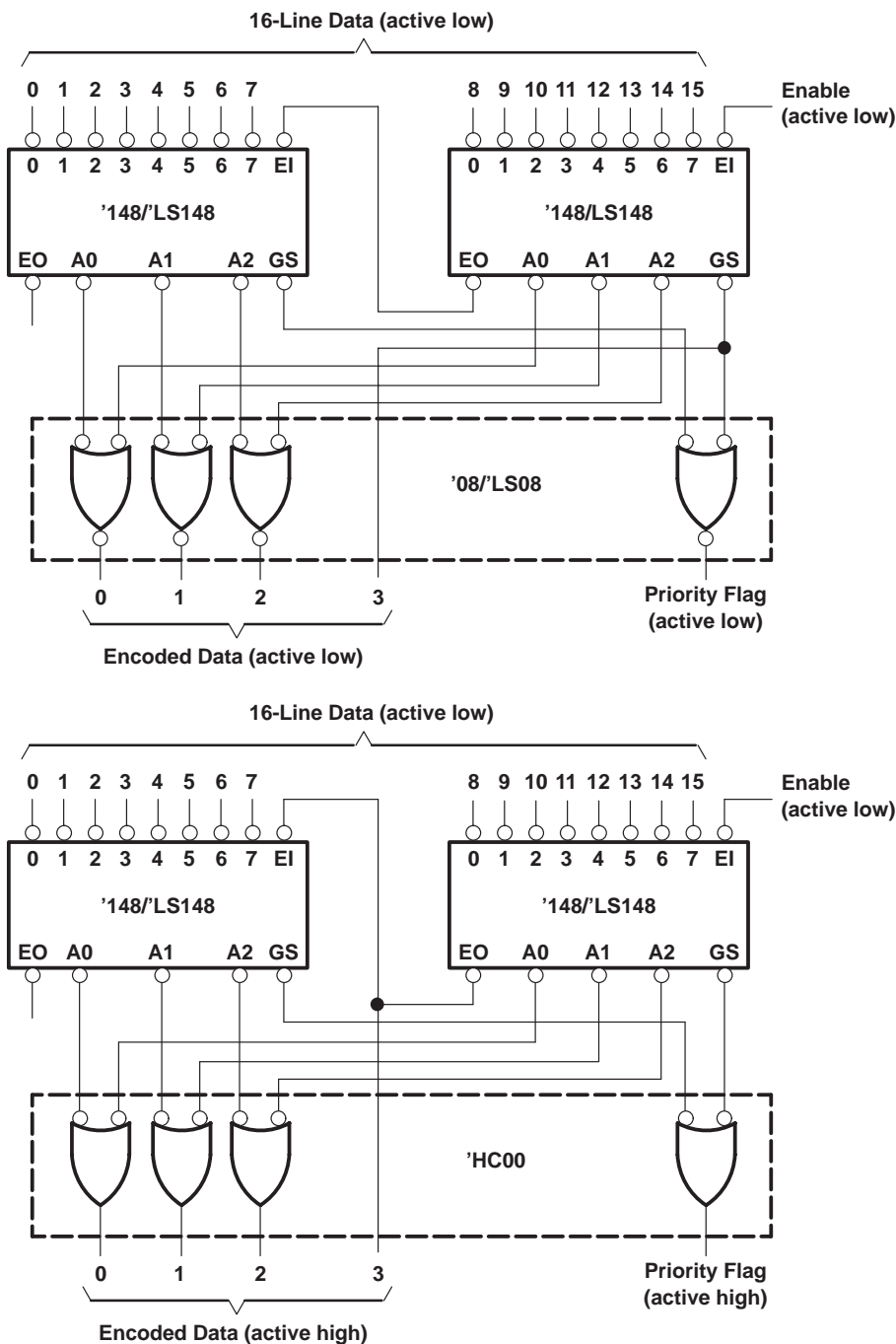
- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All diodes are 1N3064 or equivalent.  
 C. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 D. S1 and S2 are closed for  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_{PHZ}$ , and  $t_{PZL}$ ; S1 is open, and S2 is closed for  $t_{PZH}$ ; S1 is closed, and S2 is open for  $t_{PZL}$ .  
 E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.  
 F. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O \approx 50 \Omega$ ,  $t_r \leq 1.5$  ns,  $t_f \leq 2.6$  ns.  
 G. The outputs are measured one at a time, with one input transition per measurement.

**Figure 2. Load Circuits and Voltage Waveforms**

**SN54147, SN54148, SN54LS147, SN54LS148  
SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148  
10-LINE TO 4-LINE AND 8-LINE TO 3-LINE PRIORITY ENCODERS**

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**APPLICATION INFORMATION**



**Figure 3. Priority Encoder for 16 Bits**

Because the '147/LS147 and '148/LS148 devices are combinational logic circuits, wrong addresses can appear during input transients. Moreover, for the '148/LS148 devices, a change from high to low at EI can cause a transient low on GS when all inputs are high. This must be considered when strobing the outputs.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
78027012A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	78027012A SNJ54LS 148FK	<a href="#">Samples</a>
7802701EA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7802701EA SNJ54LS148J	<a href="#">Samples</a>
7802701FA	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7802701FA SNJ54LS148W	<a href="#">Samples</a>
JM38510/36001B2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 36001B2A	<a href="#">Samples</a>
JM38510/36001BEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 36001BEA	<a href="#">Samples</a>
JM38510/36001BFA	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 36001BFA	<a href="#">Samples</a>
M38510/36001B2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 36001B2A	<a href="#">Samples</a>
M38510/36001BEA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 36001BEA	<a href="#">Samples</a>
M38510/36001BFA	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 36001BFA	<a href="#">Samples</a>
SN54LS148J	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS148J	<a href="#">Samples</a>
SN74LS148D	LIFEBUY	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS148	
SN74LS148DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS148	<a href="#">Samples</a>
SN74LS148N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS148N	<a href="#">Samples</a>
SN74LS148NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS148	<a href="#">Samples</a>
SNJ54LS148FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	78027012A SNJ54LS 148FK	<a href="#">Samples</a>
SNJ54LS148J	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7802701EA SNJ54LS148J	<a href="#">Samples</a>
SNJ54LS148W	ACTIVE	CFP	W	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7802701FA SNJ54LS148W	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54LS148, SN74LS148 :**

● Catalog : [SN74LS148](#)

● Military : [SN54LS148](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS148DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS148NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS148DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74LS148NSR	SO	NS	16	2000	367.0	367.0	38.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
78027012A	FK	LCCC	20	1	506.98	12.06	2030	NA
7802701FA	W	CFP	16	1	506.98	26.16	6220	NA
JM38510/36001B2A	FK	LCCC	20	1	506.98	12.06	2030	NA
JM38510/36001BFA	W	CFP	16	1	506.98	26.16	6220	NA
M38510/36001B2A	FK	LCCC	20	1	506.98	12.06	2030	NA
M38510/36001BFA	W	CFP	16	1	506.98	26.16	6220	NA
SN74LS148D	D	SOIC	16	40	507	8	3940	4.32
SN74LS148N	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS148N	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54LS148FK	FK	LCCC	20	1	506.98	12.06	2030	NA
SNJ54LS148W	W	CFP	16	1	506.98	26.16	6220	NA



# PACKAGE OUTLINE

## NS0016A

### SOP - 2.00 mm max height

SOP



4220735/A 12/2021

#### NOTES:

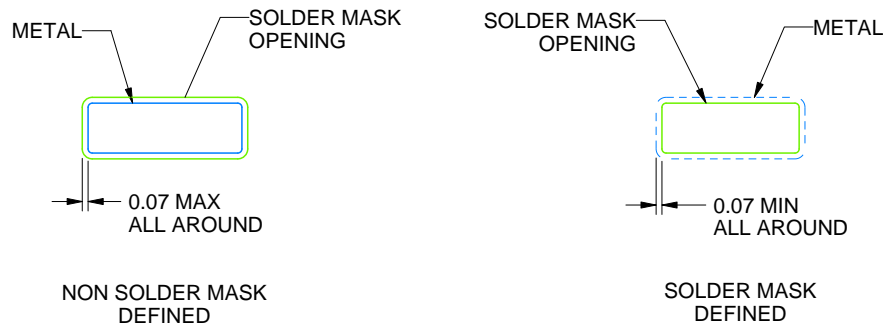
- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

# EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

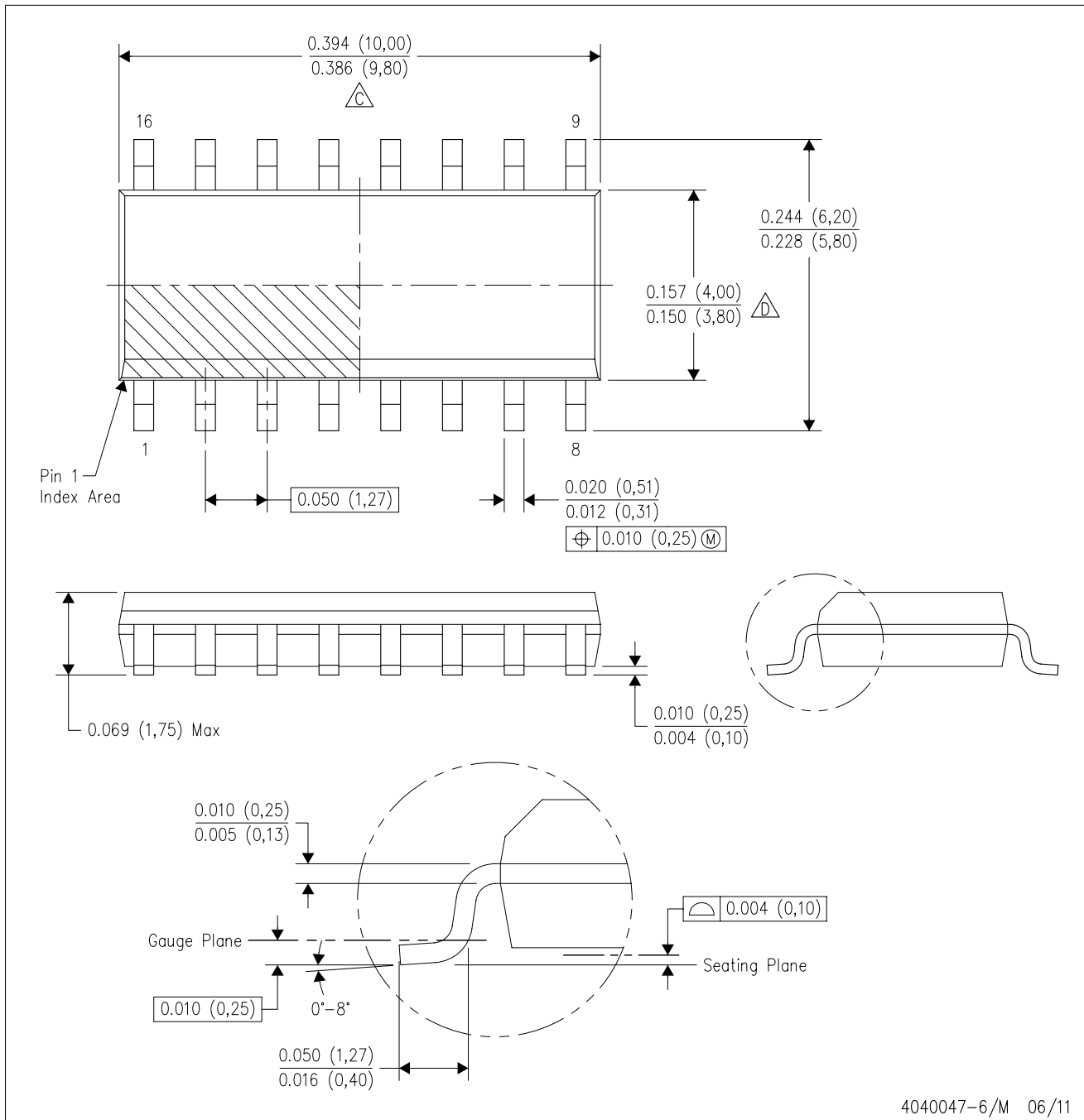
4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

## MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

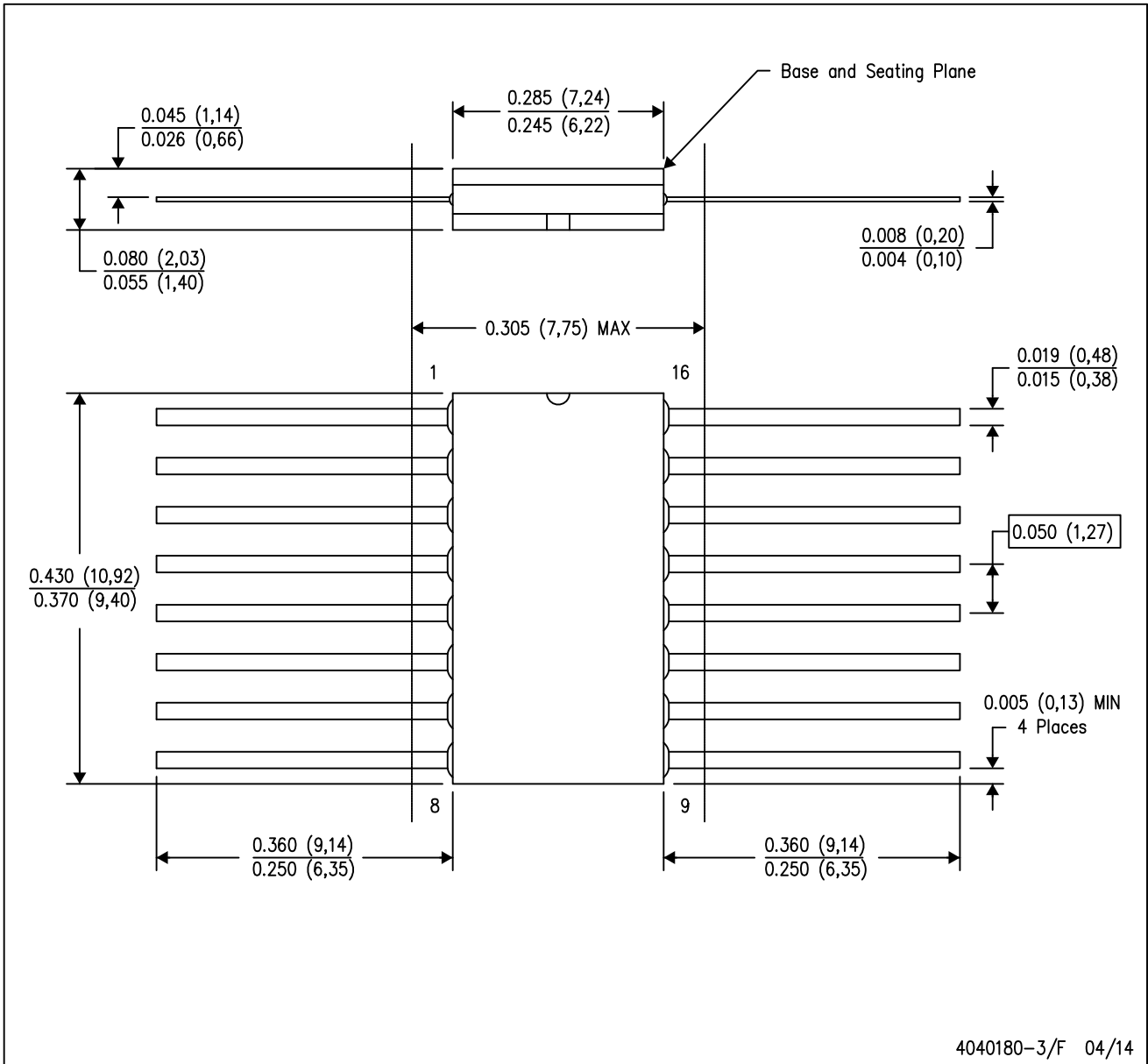


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP2-F16

## GENERIC PACKAGE VIEW

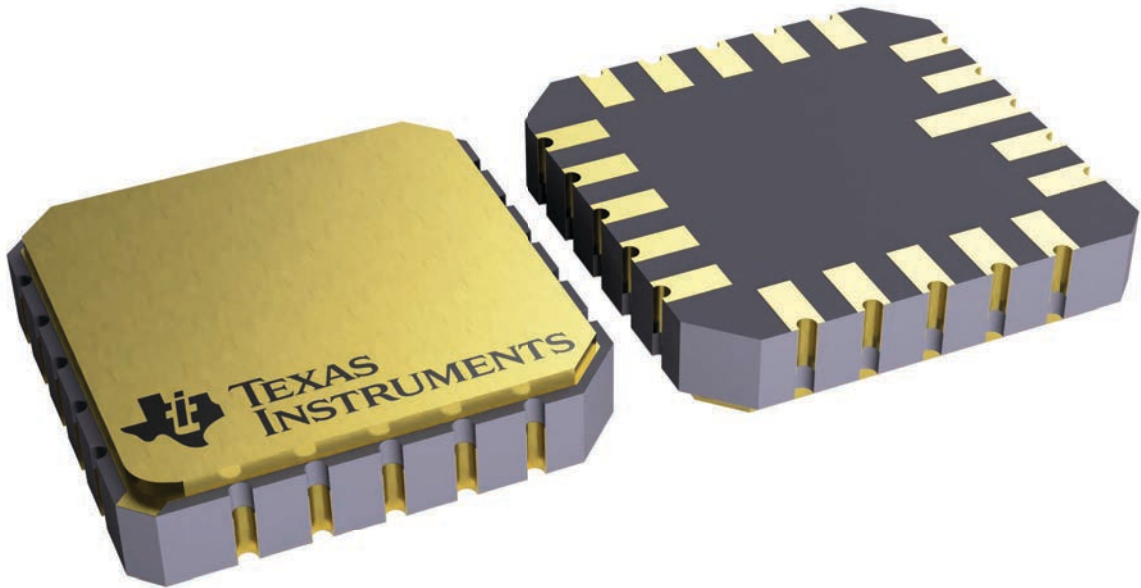
**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

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