- State-of-the-Art Advanced BICMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments Widebus™ Family
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Support Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Packaged In Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVT16244A . . . WD PACKAGE
SN74LVT16244A . . . DGG OR DL PACKAGE
(TOP VIEW)

1OE	1	48	2OE
1Y1	2	47	1A1
1Y2	3	46	1A2
GND	4	45	GND
1Y3	5	44	1A3
1Y4	6	43	1A4
V_{CC}	7	42	V_{CC}
2Y1	8	41	2A1
2Y2	9	40	2A2
GND	10	39	GND
2Y3	11	38	2A3
2Y4	12	37	2A4
3Y1	13	36	3A1
3Y2	14	35	3A2
GND	15	34	GND
3Y3	16	33	3A3
3Y4	17	32	3A4
V_{CC}	18	31	V_{CC}
4Y1	19	30	4A1
4Y2	20	29	4A2
GND	21	28	GND
4Y3	22	27	4A3
4Y4	23	26	4A4
4OE	24	25	3OE

description

The 'LVT16244A are 16-bit buffers and line drivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and symmetrical active-low output-enable ($\overline{OE}$) inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT16244A is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

Widebus is a trademark of Texas Instruments Incorporated.

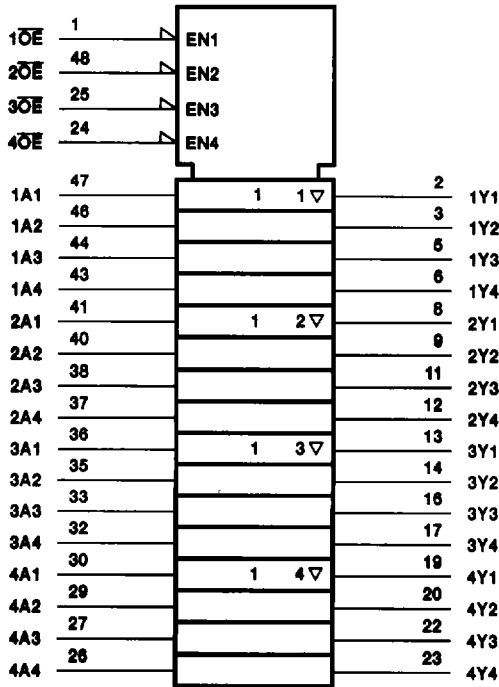**TEXAS INSTRUMENTS**
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

description (continued)

The SN54LVT16244A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LVT16244A is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†

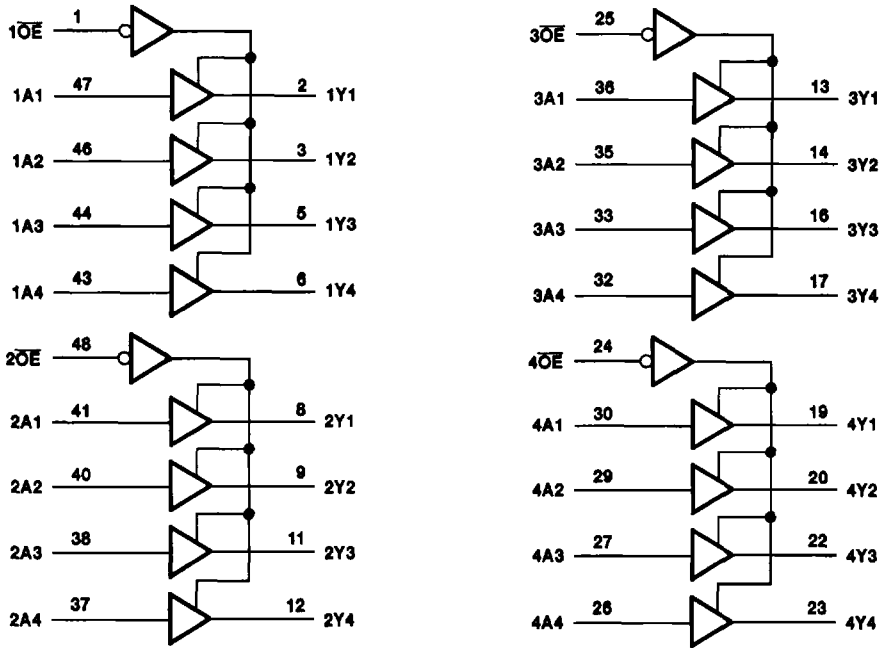† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

TEXAS
INSTRUMENTS
POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

logic diagram (positive logic)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) .... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT16244A .... 96 mA
                      SN74LVT16244A .... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT16244A .... 48 mA
                       SN74LVT16244A .... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) .... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) .... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package .... 0.85 W
                                       DL package .... 1.2 W
Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BICMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 4)

		SN54LVT16244A		SN74LVT16244A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		−24		−32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled	10		10	ns/V
T_A	Operating free-air temperature	−55	125	−40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT16244A		SN74LVT16244A			UNIT
				MIN	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 2.7$ V,	$I_I = −18$ mA			−1.2			−1.2	V
V_{OH}	$V_{CC} = $ MIN to MAX‡,	$I_{OH} = −100$ μA		$V_{CC}−0.2$		$V_{CC}−0.2$			V
	$V_{CC} = 2.7$ V,	$I_{OH} = −8$ mA		2.4		2.4			
	$V_{CC} = 3$ V	$I_{OH} = −24$ mA		2					
		$I_{OH} = −32$ mA					2		
V_{OL}	$V_{CC} = 2.7$ V	$I_{OL} = 100$ μA			0.2			0.2	V
		$I_{OL} = 24$ mA			0.5			0.5	
	$V_{CC} = 3$ V	$I_{OL} = 16$ mA			0.4			0.4	
		$I_{OL} = 32$ mA			0.5			0.5	
		$I_{OL} = 48$ mA			0.55				
		$I_{OL} = 64$ mA						0.55	
I_I	$V_{CC} = 0$ or MAX‡,	$V_I = 5.5$ V			50			10	μA
	$V_{CC} = 3.6$ V	$V_I = V_{CC}$ or GND	Control inputs		±1			±1	
		$V_I = V_{CC}$	Data inputs		1			1	
		$V_I = 0$			−5			−5	
I_{off}	$V_{CC} = 0$,	V_I or $V_O = 0$ to 4.5 V						±100	μA
$I_{I(hold)}$	$V_{CC} = 3$ V	$V_I = 0.8$ V	A inputs	75		75			μA
		$V_I = 2$ V		−75		−75			
I_{OZH}	$V_{CC} = 3.6$ V,	$V_O = 3$ V			5			5	μA
I_{OZL}	$V_{CC} = 3.6$ V,	$V_O = 0.5$ V			−5			−5	μA
I_{CC}	$V_{CC} = 3.6$ V, $V_I = V_{CC}$ or GND	$I_O = 0$,	Outputs high		0.19			0.09	mA
			Outputs low		5			5	
			Outputs disabled		0.19			0.09	
ΔI_{CC}§	$V_{CC} = 3$ V to 3.6 V, One input at $V_{CC} − 0.6$ V, Other inputs at V_{CC} or GND				0.2			0.2	mA
C_i	$V_I = 3$ V or 0						4		pF
C_o	$V_O = 3$ V or 0						10		pF

† All typical values are at $V_{CC} = 3.3$ V, $T_A = 25$°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

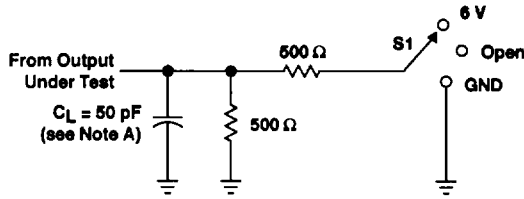| PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT16244A				SN74LVT16244A					UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX	
t_{PLH}	A	Y	1	4.4		5.1	1	2.3	4.1		5	ns
t_{PHL}			1	4.5		5.3	1	2.3	4.1		5.2	
t_{PZH}	$\overline{OE}$	Y	1	5.3		6.4	1	2.6	5.2		6.3	ns
t_{PZL}			1	5.3		6.8	1	2.6	5.2		6.7	
t_{PHZ}	$\overline{OE}$	Y	2.1	7		7.7	2.2	3.9	5.7		6.3	ns
t_{PLZ}			1.9	5.9		5.9	2	3.7	5.1		5.6	

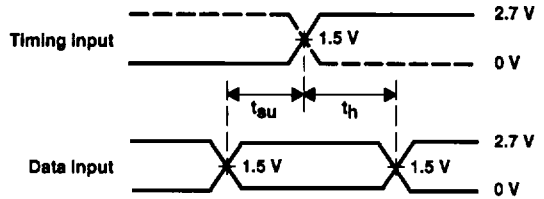† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

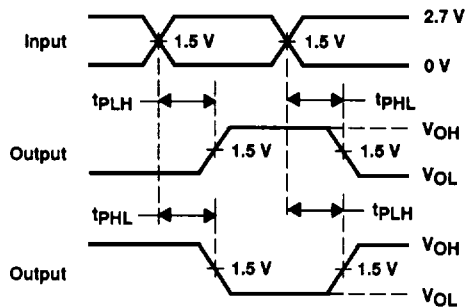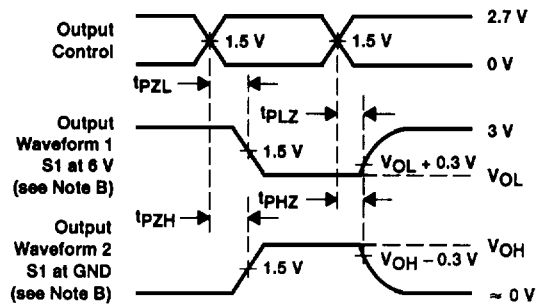| TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	6 V
tPHZ/tPZH	GND

LOAD CIRCUIT FOR OUTPUTS
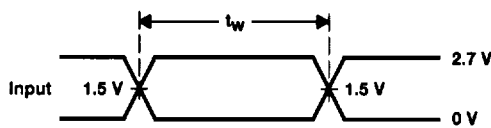
VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

TEXAS
INSTRUMENTS
POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265