SDLS037

# DUAL J-$\overline{K}$ POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

DECEMBER 1983 – REVISED MARCH 1988

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

## description

These devices contain two independent J-$\overline{K}$ positive-edge-triggered flip-flops. A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the J and $\overline{K}$ inputs meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and $\overline{K}$ inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding $\overline{K}$ and tying J high. They also can perform as D-type flip-flops if J and $\overline{K}$ are tied together.

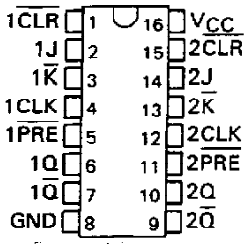
The SN54109 and SN54LS109A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74109 and SN74LS109A are characterized for operation from 0°C to 70°C.

**FUNCTION TABLE (each flip-flop)**

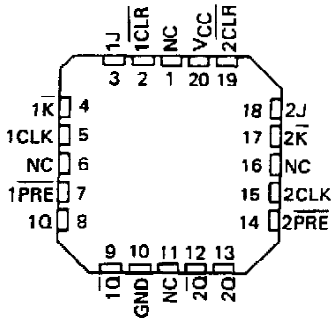
| INPUTS | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|
| $\overline{PRE}$ | $\overline{CLR}$ | CLK | J | K | Q | $\overline{Q}$ |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H† | H† |
| H | H | ↑ | L | L | L | H |
| H | H | ↑ | H | L | TOGGLE | |
| H | H | ↑ | L | H | $Q_0$ | $\overline{Q}_0$ |
| H | H | ↑ | H | H | H | L |
| H | H | L | X | X | $Q_0$ | $\overline{Q}_0$ |

† The output levels in this configuration are not guaranteed to meet the minimum levels for $V_{OH}$ if the lows at preset and clear are near $V_{IL}$ maximum. Furthermore, this configuration is nonstable; that is, it will not persist when preset or clear return to their inactive (high) level.

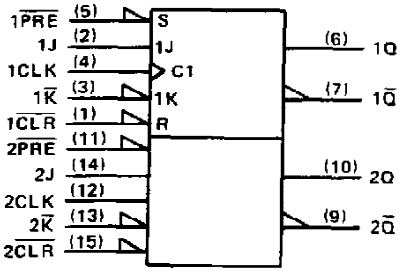
**SN54109, SN54LS109A . . . J OR W PACKAGE**
**SN74109 . . . N PACKAGE**
**SN74LS109A . . . D OR N PACKAGE**
**(TOP VIEW)**




**SN54LS109A . . . FK PACKAGE**
**(TOP VIEW)**




## logic symbol‡

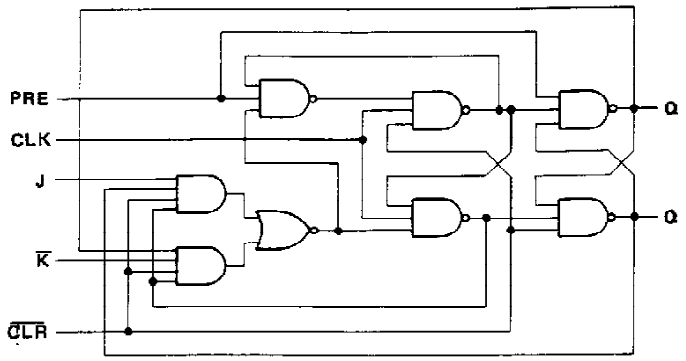



‡This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

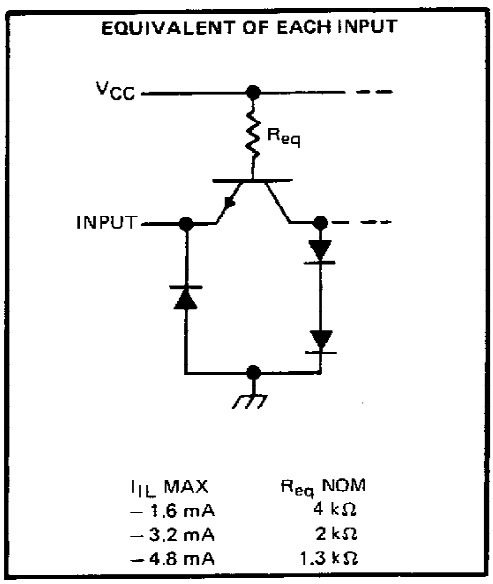
## logic diagram (positive logic)

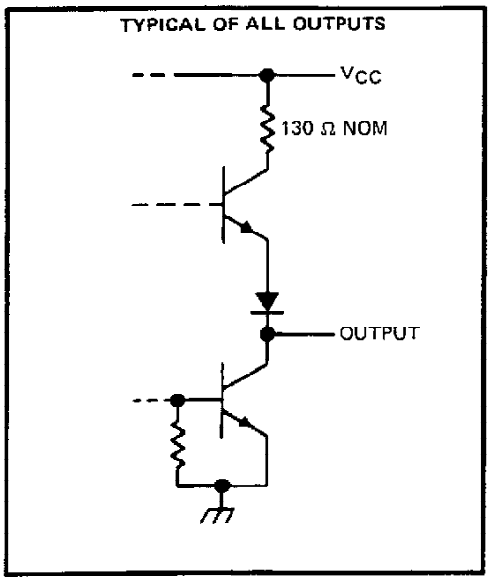
'109



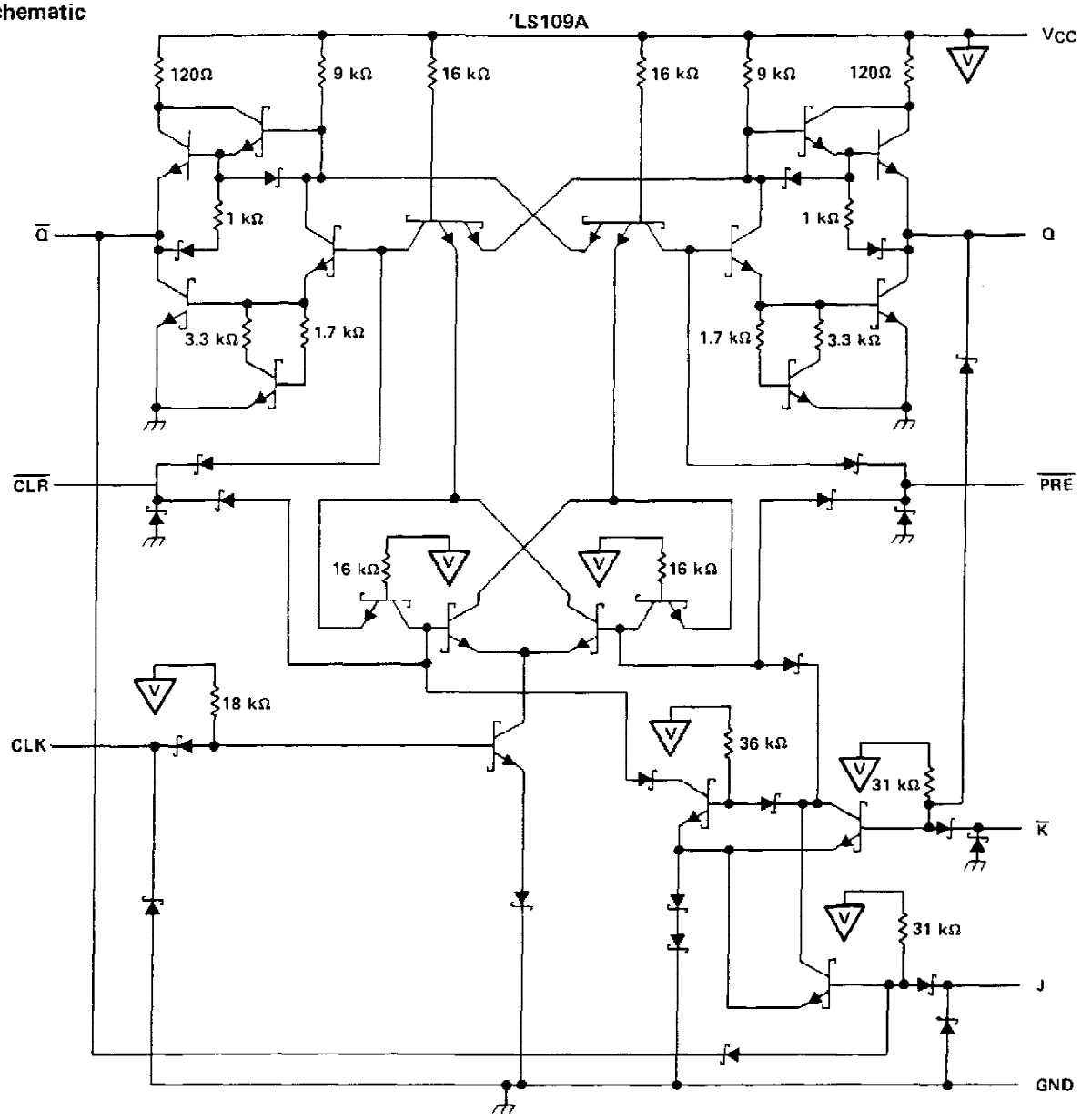

## schematics of inputs and outputs

'109



schematic




**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage: '109 . . . . . 5.5 V
'LS109A . . . . . 7 V
Operating free-air temperature range: SN54' . . . . . −55°C to 125°C
SN74' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

| | | | SN54109 | | | SN74109 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | | −0.8 | | | −0.8 | mA |
| $I_{OL}$ | Low-level output current | | | | 16 | | | 16 | mA |
| $t_w$ | Pulse duration | CLK high or low | 20 | | | 20 | | | ns |
| | | $\overline{PRE}$ or $\overline{CLR}$ low | 20 | | | 20 | | | |
| $t_{su}$ | Input setup time before CLK↑ | | 10 | | | 10 | | | ns |
| $t_h$ | Input hold time-data after CLK↑ | | 6 | | | 6 | | | ns |
| $T_A$ | Operating free-air temperature | | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | | SN54109 | | | SN74109 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | | $V_{CC}$ = MIN, | $I_I$ = −12 mA | | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | | $V_{CC}$ = MIN, $I_{OH}$ = −0.8 mA | $V_{IH}$ = 2 V, | $V_{IL}$ = 0.8 V, | 2.4 | 3.4 | | 2.4 | 3.4 | | V |
| $V_{OL}$ | | $V_{CC}$ = MIN, $I_{OL}$ = 16 mA | $V_{IH}$ = 2 V, | $V_{IL}$ = 0.8 V, | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| $I_I$ | | $V_{CC}$ = MAX, | $V_I$ = 5.5 V | | | | 1 | | | 1 | mA |
| $I_{IH}$ | J or $\overline{K}$ | $V_{CC}$ = MAX, | $V_I$ = 2.4 V | | | | 40 | | | 40 | μA |
| | $\overline{CLR}$ | | | | | | 160 | | | 160 | |
| | $\overline{PRE}$ or CLK | | | | | | 80 | | | 80 | |
| $I_{IL}$ | J or $\overline{K}$ | $V_{CC}$ = MAX, | $V_I$ = 0.4 V | | | | −1.6 | | | −1.6 | mA |
| | $\overline{CLR}$¶ | | | | | | −4.8 | | | −4.8 | |
| | $\overline{PRE}$¶ | | | | | | −3.2 | | | −3.2 | |
| | CLK | | | | | | −3.2 | | | −3.2 | |
| $I_{OS}$§ | | $V_{CC}$ = MAX | | | −30 | | −85 | −30 | | −85 | mA |
| $I_{CC}$# | | $V_{CC}$ = MAX, | See Note 2 | | | 9 | 15 | | 9 | 15 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ Not more than one output should be shorted at a time.
¶ Clear is tested with preset high and preset is tested with clear high.
# Average per flip-flop.
NOTE 2: With all outputs open, $I_{CC}$ is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C (see note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{max}$ | | | $R_L$ = 400 Ω, $C_L$ = 15 pF | 25 | 33 | | MHz |
| $t_{PLH}$ | $\overline{PRE}$ | Q | | | 10 | 15 | ns |
| $t_{PHL}$ | | $\overline{Q}$ | | | 23 | 35 | ns |
| $t_{PLH}$ | $\overline{CLR}$ | $\overline{Q}$ | | | 10 | 15 | ns |
| $t_{PHL}$ | | Q | | | 17 | 25 | ns |
| $t_{PLH}$ | CLK | Q or $\overline{Q}$ | | | 10 | 16 | ns |
| $t_{PHL}$ | | | | | 18 | 28 | ns |

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

## recommended operating conditions

| | | | SN54LS109A | | | SN74LS109A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.7 | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | | −0.4 | | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | | | | 4 | | | 8 | mA |
| $f_{clock}$ | Clock frequency | | 0 | | 25 | 0 | | 25 | MHz |
| $t_w$ | Pulse duration | CLK high | 25 | | | 25 | | | ns |
| | | $\overline{PRE}$ or $\overline{CLR}$ low | 25 | | | 25 | | | |
| $t_{su}$ | Setup time before CLK ↑ | High-level data | 35 | | | 35 | | | ns |
| | | Low-level data | 25 | | | 25 | | | |
| $t_h$ | Hold time-data after CLK ↑ | | 5 | | | 5 | | | ns |
| $T_A$ | Operating free-air temperature | | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | | SN54LS109A | | | SN74LS109A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | | $V_{CC}$ = MIN, | $I_I$ = −18 mA | | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | | $V_{CC}$ = MIN, $I_{OH}$ = −0.4 mA | $V_{IH}$ = 2 V, | $V_{IL}$ = MAX, | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| $V_{OL}$ | | $V_{CC}$ = MIN, $I_{OL}$ = 4 mA | $V_{IL}$ = MAX, | $V_{IH}$ = 2 V, | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | $V_{CC}$ = MIN, $I_{OL}$ = 8 mA | $V_{IL}$ = MAX, | $V_{IH}$ = 2 V, | | | | | 0.35 | 0.5 | |
| $I_I$ | J, $\overline{K}$ or CLK | $V_{CC}$ = MAX, | $V_I$ = 7 V | | | | 0.1 | | | 0.1 | mA |
| | $\overline{CLR}$ or $\overline{PRE}$ | | | | | | 0.2 | | | 0.2 | |
| $I_{IH}$ | J, $\overline{K}$ or CLK | $V_{CC}$ = MAX, | $V_I$ = 2.7 V | | | | 20 | | | 20 | μA |
| | $\overline{CLR}$ or $\overline{PRE}$ | | | | | | 40 | | | 40 | |
| $I_{IL}$ | J, $\overline{K}$ or CLK | $V_{CC}$ = MAX, | $V_I$ = 0.4 V | | | | −0.4 | | | −0.4 | mA |
| | $\overline{CLR}$ or $\overline{PRE}$ | | | | | | −0.8 | | | −0.8 | |
| $I_{OS}$§ | | $V_{CC}$ = MAX, | See Note 4 | | −20 | | −100 | −20 | | −100 | mA |
| $I_{CC}$ (Total) | | $V_{CC}$ = MAX, | See Note 2 | | | 4 | 8 | | 4 | 8 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: With all outputs open, $I_{CC}$ is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.
NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with $V_O$ = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively with the minimum and maximum limits reduced to one half of their stated values.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C (see note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | | | $R_L$ = 2 kΩ, | $C_L$ = 15 pF | 25 | 33 | | MHz |
| $t_{PLH}$ | $\overline{CLR}$, $\overline{PRE}$ or CLK | Q or $\overline{Q}$ | | | | 13 | 25 | ns |
| $t_{PHL}$ | | | | | | 25 | 40 | ns |

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| JM38510/30109B2A | NRND | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | JM38510/ 30109B2A | |
| JM38510/30109BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30109BEA | Samples |
| JM38510/30109BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30109BEA | Samples |
| JM38510/30109BFA | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30109BFA | Samples |
| JM38510/30109BFA | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30109BFA | Samples |
| JM38510/30109SEA | NRND | CDIP | J | 16 | 25 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30109SEA | |
| JM38510/30109SEA | NRND | CDIP | J | 16 | 25 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30109SEA | |
| JM38510/30109SFA | NRND | CFP | W | 16 | 25 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30109SFA | |
| JM38510/30109SFA | NRND | CFP | W | 16 | 25 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30109SFA | |
| M38510/30109B2A | NRND | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | JM38510/ 30109B2A | |
| M38510/30109B2A | NRND | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | JM38510/ 30109B2A | |
| M38510/30109BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30109BEA | Samples |
| M38510/30109BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30109BEA | Samples |
| M38510/30109BFA | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30109BFA | Samples |
| M38510/30109BFA | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30109BFA | Samples |
| M38510/30109SEA | NRND | CDIP | J | 16 | 25 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30109SEA | |
| M38510/30109SEA | NRND | CDIP | J | 16 | 25 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30109SEA | |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| M38510/30109SFA | NRND | CFP | W | 16 | 25 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30109SFA | |
| M38510/30109SFA | NRND | CFP | W | 16 | 25 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/ 30109SFA | |
| SN54LS109AJ | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SN54LS109AJ | Samples |
| SN54LS109AJ | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SN54LS109AJ | Samples |
| SN74109N | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN74109N | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN74LS109AD | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS109A | Samples |
| SN74LS109AD | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS109A | Samples |
| SN74LS109ADR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS109A | Samples |
| SN74LS109ADR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS109A | Samples |
| SN74LS109ADRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS109A | Samples |
| SN74LS109ADRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS109A | Samples |
| SN74LS109AN | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS109AN | Samples |
| SN74LS109AN | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS109AN | Samples |
| SN74LS109AN3 | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN74LS109AN3 | OBSOLETE | PDIP | N | 16 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN74LS109ANE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS109AN | Samples |
| SN74LS109ANE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74LS109AN | Samples |
| SN74LS109ANSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS109A | Samples |
| SN74LS109ANSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74LS109A | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SNJ54LS109AFK | NRND | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | SNJ54LS 109AFK | |
| SNJ54LS109AFK | NRND | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | SNJ54LS 109AFK | |
| SNJ54LS109AJ | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SNJ54LS109AJ | Samples |
| SNJ54LS109AJ | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SNJ54LS109AJ | Samples |
| SNJ54LS109AW | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SNJ54LS109AW | Samples |
| SNJ54LS109AW | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SNJ54LS109AW | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**OTHER QUALIFIED VERSIONS OF SN54LS109A, SN54LS109A-SP, SN74LS109A :**

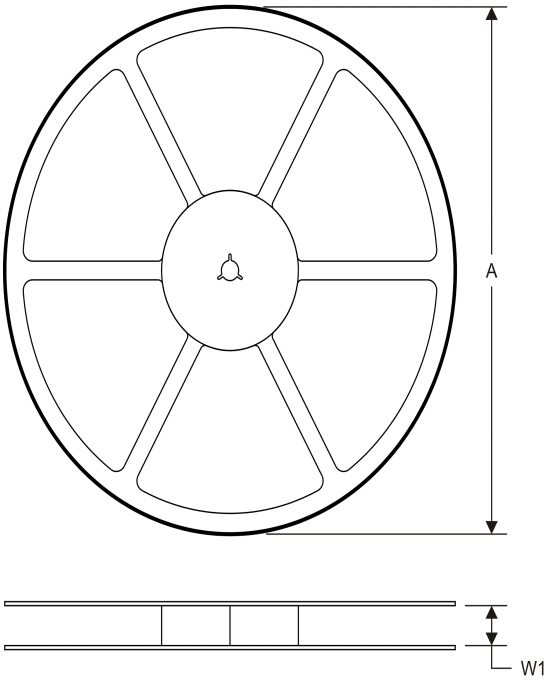
- Catalog: SN74LS109A, SN54LS109A
- Military: SN54LS109A
- Space: SN54LS109A-SP

NOTE: Qualified Version Definitions:

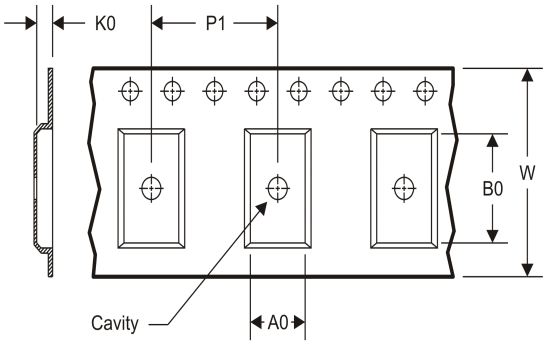
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**




**TAPE DIMENSIONS**



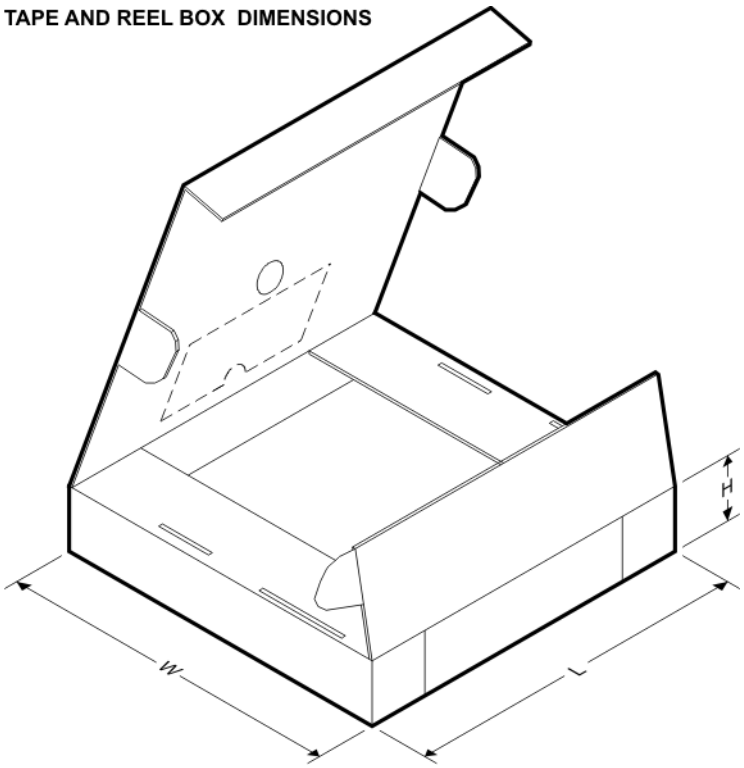

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**TAPE AND REEL INFORMATION**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LS109ADR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LS109ANSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LS109ADR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| SN74LS109ANSR | SO | NS | 16 | 2000 | 367.0 | 367.0 | 38.0 |

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