National Semiconductor

T-52-09

MM54HC240/MM74HC240 Inverting Octal TRI-STATE® Buffer MM54HC241/MM74HC241 Octal TRI-STATE Buffer

General Description

These TRI-STATE buffers utilize advanced silicon-gate CMOS technology. They possess high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits achieve speeds comparable to low power Schottky devices, while retaining the advantage of CMOS circuitry, i.e., high noise immunity and low power consumption. Each has a fanout of 15 LS-TTL equivalent inputs.

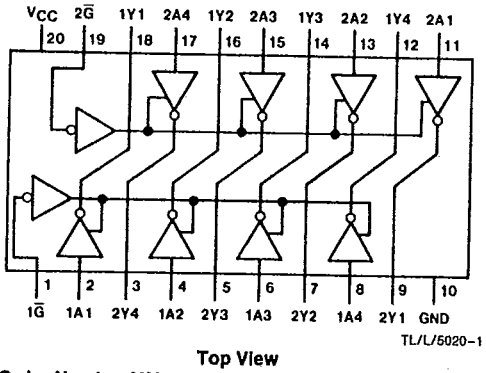
The MM54HC240/MM74HC240 is an inverting buffer and has two active low enables ($1\overline{G}$ and $2\overline{G}$). Each enable independently controls 4 buffers. MM54HC241/MM74HC241 is a non-inverting buffer that has one active low enable and one active high enable, each again controlling 4 buffers. Neither device has Schmitt trigger inputs.

All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 12 ns
- TRI-STATE outputs for connection to system buses
- Wide power supply range: 2–6V
- Low quiescent supply current: 80 μA (74 Series)
- Output current: 6 mA

Connection Diagrams Dual-In-Line Packages



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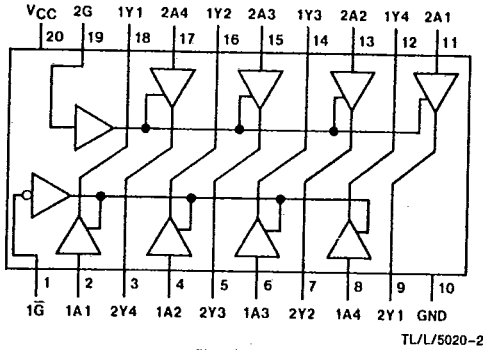
Top View
Order Number MM54HC240/241* or MM74HC240/241*

*Please look into Section 8, Appendix D for availability of various package types.



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Top View
Order Number MM54HC240/241* or MM74HC240/241*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Tables

('HC240)

$1\overline{G}$	1A	1Y	$2\overline{G}$	2A	2Y
L	L	H	L	L	H
L	H	L	L	H	L
H	L	Z	H	L	Z
H	H	Z	H	H	Z

H = high level, L = low level, Z = high impedance

('HC241)

$1\overline{G}$	1A	1Y	2G	2A	2Y
L	L	L	L	L	Z
L	H	H	L	H	Z
H	L	Z	H	L	L
H	H	Z	H	H	H

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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions T-52-09

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤6.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$≤7.8 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤6.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$≤7.8 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND $\overline{G}$=V_{IH}, G=V_{IL}	6.0V		±0.5	±5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics MM54HC240/MM74HC240 $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=45$ pF	12	18	ns
t_{PZH}, t_{PZL}	Maximum Enable Delay to Active Output	$R_L=1$ kΩ $C_L=45$ pF	14	28	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Delay from Active Output	$R_L=1$ kΩ $C_L=5$ pF	13	25	ns

AC Electrical Characteristics MM54HC240/MM74HC240

$V_{CC}=2.0V$ to 6.0V, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C		54HC $T_A=-55$ to 125°C		Units
				Typ	Guaranteed Limits				
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=50$ pF	2.0V	55	100		126	149	ns
		$C_L=150$ pF	2.0V	80	150		190	224	ns
		$C_L=50$ pF	4.5V	12	20		25	30	ns
		$C_L=150$ pF	4.5V	22	30		38	45	ns
		$C_L=50$ pF	6.0V	11	17		21	25	ns
		$C_L=150$ pF	6.0V	28	26		32	38	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ							
		$C_L=50$ pF	2.0V	75	150		189	224	ns
		$C_L=150$ pF	2.0V	100	200		252	298	ns
		$C_L=50$ pF	4.5V	15	30		38	45	ns
		$C_L=150$ pF	4.5V	20	40		50	60	ns
		$C_L=50$ pF	6.0V	13	26		32	38	ns
		$C_L=150$ pF	6.0V	17	34		43	51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ	2.0V	75	150		189	224	ns
		$C_L=50$ pF	4.5V	15	30		38	45	ns
			6.0V	13	26		32	38	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V		60		75	90	ns
			4.5V		12		15	18	ns
			6.0V		10		13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per buffer)							
		$\overline{G}=V_{IH}$		12					pF
		$\overline{G}=V_{IL}$		50					pF
C_{IN}	Maximum Input Capacitance			5	10		10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20		20	20	pF

AC Electrical Characteristics MM54HC241/MM74HC241 $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions		Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=45$ pF		13	20	ns
t_{PZH}, t_{PZL}	Maximum Enable Delay to Active Output	$R_L=1$ kΩ	$1\overline{G}$	17	28	ns
		$C_L=45$ pF	$2\overline{G}$	17	28	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Delay from Active Input	$R_L=1$ kΩ	$1\overline{G}$	15	25	ns
		$C_L=5$ pF	$2\overline{G}$	13	25	ns

AC Electrical Characteristics MM54HC241/MM74HC241

$V_{CC}=2.0V$ to 6.0V, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=50$ pF	2.0V	58	115	145	171	ns
		$C_L=150$ pF	2.0V	83	165	208	246	ns
		$C_L=50$ pF	4.5V	14	23	29	34	ns
		$C_L=150$ pF	4.5V	17	33	42	49	ns
		$C_L=50$ pF	6.0V	10	20	25	29	ns
		$C_L=150$ pF	6.0V	14	28	35	42	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	75	150	189	224	ns
		$C_L=150$ pF	2.0V	100	200	252	298	ns
		$C_L=50$ pF	4.5V	15	30	38	45	ns
		$C_L=150$ pF	4.5V	20	40	50	60	ns
		$C_L=50$ pF	6.0V	13	26	32	38	ns
		$C_L=150$ pF	6.0V	17	34	43	51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ	2.0V	75	150	189	224	ns
		$C_L=50$ pF	4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V		60	75	90	ns
			4.5V		12	15	18	ns
			6.0V		10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per buffer)						
		$G=V_{IL}$, $\overline{G}=V_{IH}$		12				pF
		$G=V_{IH}$, $\overline{G}=V_{IL}$		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

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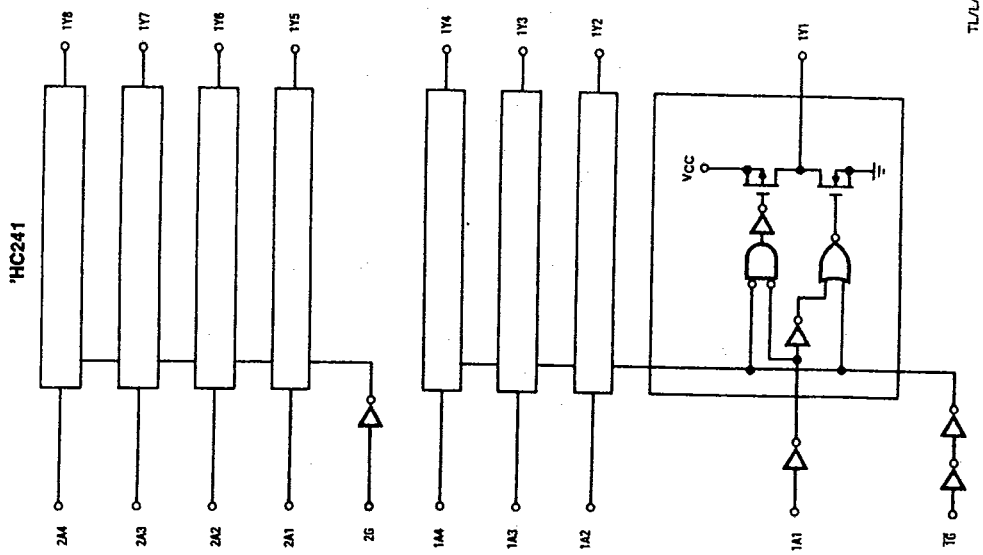
Logic Diagrams



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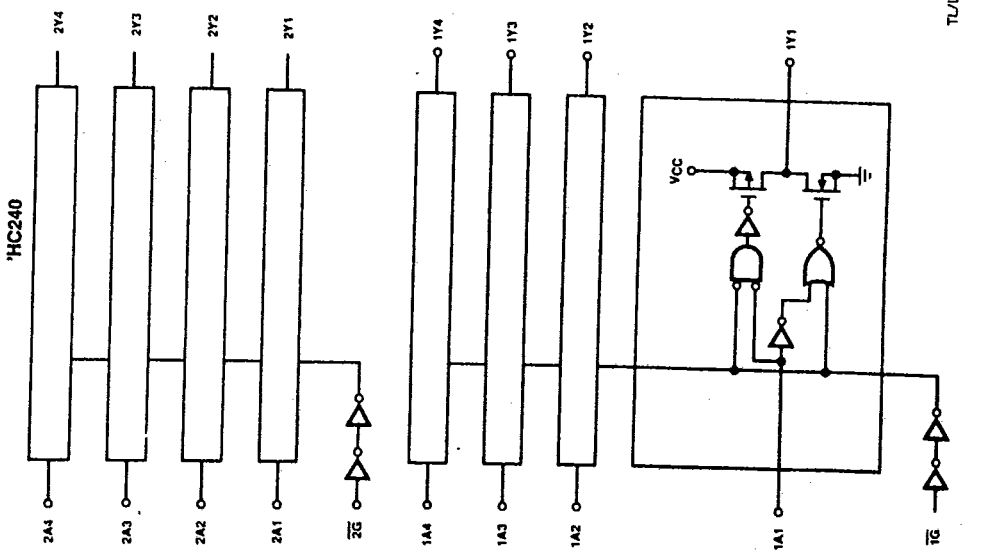

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