National Semiconductor

October 1993

GAL22CV10-10 24-Pin Generic Array Logic Family

General Description

The EECMOS GAL22CV10 devices are fabricated using electricaly erasable floating gate technology. This programmable memory technology applied to array logic provides designers with reconfigurable logic and bipolar performance at significantly reduced power levels.

The 24-pin GAL22CV10 features 10 programmable Output Logic Macrocells (OLMCs) allowing each TRI-STATE® output to be configured by the user. The GAL22CV10 is also cabable of emulating most popular 24-pin PAL® devices.

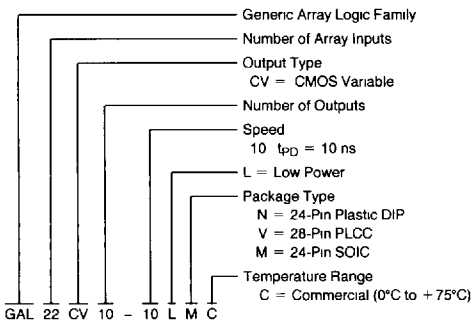
Programming is accomplished using popular hardware and software tools. NSC guarantees a minimum of 100 erase/write cycles.

Unique test circuitry and reprogrammable cells allow complete AC, DC, cell, and functionality testing during manufacture. Therefore, NSC guarantees 100% field programmability and functionality of NSC GAL® devices. In addition, a security circuit is built-in, providing proprietary designs with copy protection.

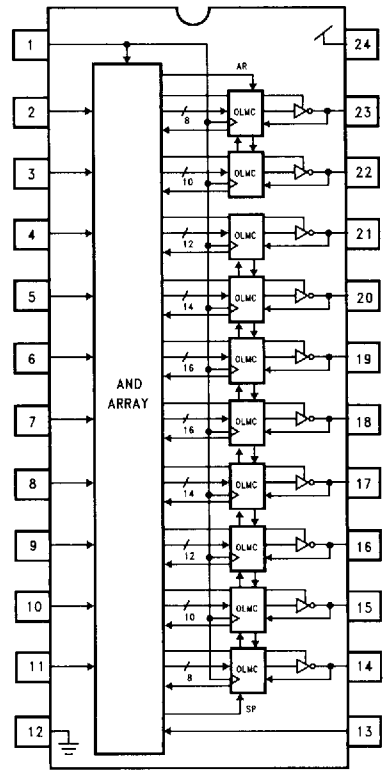
Features

- High performance EECMOS technology
  - 10 ns maximum propagation delay
  - 6 ns setup time delay
  - TTL compatible 16 mA outputs
  - 2000V ESD protection
- Reduced power
  - I_{CC} max = 130 mA @ 25 MHz
- Electrically erasable cell technology
  - Reconfigurable logic
  - 100% tested at manufacture
- Output Logic Macrocells (OLMCs)
  - Maximum flexibility for complex logic design
  - Programmable output polarity
  - Emulates popular PAL devices
- Fully supported by National OPAL™ and OPALjr development software as well as 3rd-party PLD development tools
- Security cell prevents copying logic

Ordering Information



Block Diagram



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OPAL™ is a trademark of National Semiconductor Corporation
GAL® is a registered trademark of Lattice Semiconductor
PAL® is a registered trademark of and used under license from AMD Inc

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to V_{CC} + 0.6V
Off-State Output Voltage (Note 2)	−0.5V to V_{CC} + 0.6V
Output Current	±100 mA
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
ESD Tolerance	2000V
C_{ZAP} = 100 pF R_{ZAP} = 1500Ω Test Method: Human Body Model Test spec.: NSC SOP-5-028	

Recommended Operating Conditions

Symbol	Parameter	Commercial			Units
		Min	Typ	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
T_A	Operating Free-Air Temperature	0	25	75	°C
t_r	Clock Rise Time			250	ns
t_f	Clock Fall Time			250	ns
$t_{rV_{CC}}$	V_{CC} Rise Time			250	ms

Electrical Characteristics

Symbol	Parameter	Conditions	Commercial		Units
			Min	Max	
V_{IH}	High Level Input Voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Low Level Input Voltage		−0.3	0.8	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = −3.2 mA	2.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.5	V
I_{OS}	Output Short Circuit Current	V_{CC} = 5.0V, V_O = 0.5V, T_A = 25°C (One output, duration < 1 sec.)	−30	−135	mA
C_I	Input Capacitance	V_{CC} = 5.0V, T_A = 25°C, f = 25 MHz		6	pF
$C_{I/O}$	I/O Capacitance	V_{CC} = 5.0V, T_A = 25°C, f = 25 MHz		12	pF

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions

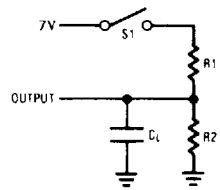
Note 2: Some device pins may be raised above these limits during programming and preload operations according to the applicable specification

AC Specifications

Symbol	Parameter	Conditions (Note 3)	Commercial GAL22CV10-10L Min	Commercial GAL22CV10-10L Max	Units
t_{PD}	Input or F/B to Combinatorial Output	S1 Open, C_L = 50 pF		10	ns
t_{SU}	Input or F/B Setup Time before Clock			6	ns
t_H	Hold Time (Input after Clock)			0	ns
t_{CLK}	Clock to Registered Ouput or F/B	S1 Open, C_L = 50 pF		8	ns
t_{CFB}	Clock to Registered F/B	S1 Open, C_L = 50 pF		7	ns
f_{MAX}	Clock Frequency	With Feedback Without Feedback	71 125		MHz
t_W	Clock Pulse Width (High/Low)	Referenced at 10% and 90%	4		ns
t_{CYCLE}	Clock Period (with F/B)	$t_{CYCLE} = t_{SU} + t_{CLK}$	12		ns
$t_{PZH/L}$	Input to Output Enable	C_L = 50 pF		10	ns
$t_{PZH/LZ}$	Input to Output Disable	C_L = 50 pF		11	ns
t_{AP}	Input to Asynchronous Reset			13	ns
t_{AR}	Asynchronous Reset Recovery Time			9	ns
t_{RESET}	Power-Up to Registered Output High	S1 Open, C_L = 50 pF		7.5	μs
I_{CC}	Supply Current	f = 25 MHz, V_{CC} = max, No Load		130	mA

Note 3: See AC test load

AC Test Load



R1 = R2 = 500Ω
C_L = 50 pF

For

t_{pd} S1 open
$t_{PZH/HZ}$ S1 open
$t_{PZL/LZ}$ S1 closed

Active to TRI-STATE measurement level = active output level ±0.3V

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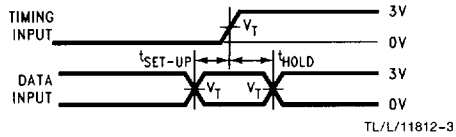
Test Waveforms

Setup and Hold



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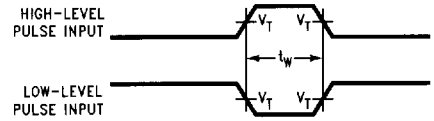
Pulse Width



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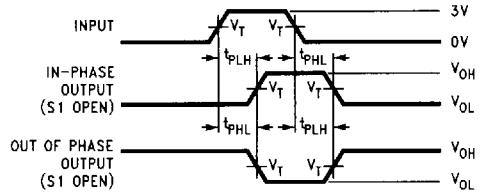
Propagation Delay



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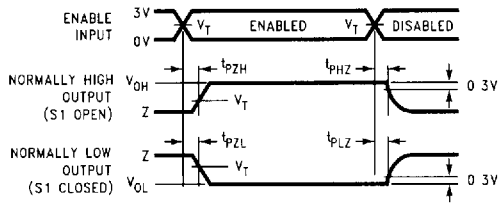
Enable and Disable



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Notes:

C_L includes probe and jig capacitance

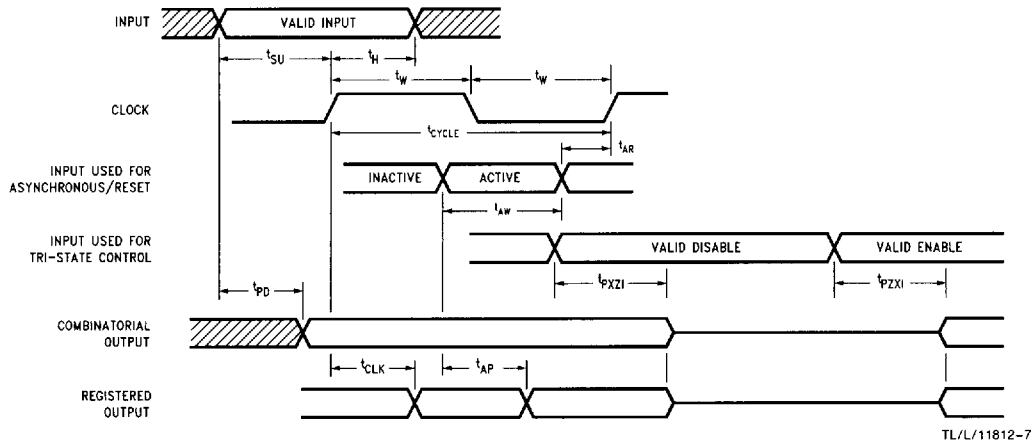
V_T = 1.5V

V_{TZ} = active output level ±0.3V

Test inputs have rise and fall times of 3 ns 10%–90%

In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily

Switching Waveform



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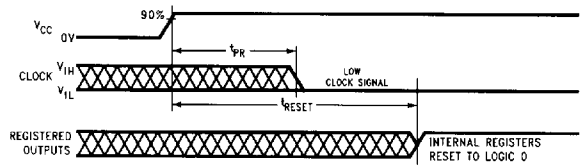
Power-Up Reset Waveform



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Functional Description

The GAL22CV10 logic array consists of a programmable AND array with fixed OR-gate connections, similar to the traditional bipolar PAL architecture. The logic array is organized as 22 complementary input lines crossing 132 "product term" lines with a programmable EEPROM cell at each intersection (5808 cells). Each programmable cell may establish a connection between an input line (true or complement phase of an array input signal) and a product term. A product term is satisfied (logically true) when all of the input lines "connected" to it are in the high logic state.

Of the 132 product terms, 130 are distributed among ten "output logic macrocells" (OLMCs) with a varying number of terms allocated to each OLMC. For a given OLMC, 8, 10, 12, 14, or 16 product terms feed into an OR-gate to produce each output value. This varied distribution of product terms among outputs allows more optimum use of device resources. One additional product term in each of the additional OLMCs is used to control the associated TRI-STATE device output. One global product term is used to control an asynchronous reset and another global product term controls a synchronous preset.

Under control of an OLMC, each output may be designated either registered or combinatorial (non-registered). In the registered output configuration, the logic function output passes through a D-type flip-flop triggered by the rising edge of the clock input. Additionally, the logic function's output polarity may be designated active-high or active-low. OLMC options such as these are selected by a set of programmable architecture control EEPROM cells. These cells are normally configured automatically by the development software or programming hardware.

The four possible output configurations of each OLMC are: registered active-high, registered-active-low, combinatorial active-high, and combinatorial active-low. The registered configurations include an internal feedback path taken directly from the register output. The combinatorial configurations include feedback from the I/O pin, thus allowing for bidirectional I/O or additional input channels.

All registers in a GAL22CV10 device are reset to the low state upon powering up. Outputs, in turn, assume either low or high logic levels depending on the selected output polarity. Power-up reset may simplify sequential circuit design and test by initializing the device to a known state. To ensure successful power-up reset, V_{CC} must rise monotonically until the specified operating voltage is attained.

The GAL22CV10 includes a programmable security EEPROM cell which, once programmed, prevents unauthorized reading or copying of designs programmed into the device.

Programmable Preset and Reset

The ten macrocell flip-flops share common programmable preset and reset control for easy system initialization. The Q outputs of the register will go to the logic high state following a low-to-high transition of the clock input when the synchronous preset (SP) product term is asserted. The register will be forced to the logic low state independent of the clock when the asynchronous reset (AR) product term is asserted. Product term control allows preset and reset to be functions of any combination of device inputs and output feedback. The outputs will be high or low depending upon the polarity option chosen.

Note that preset and reset control the flip-flop, not the output. Thus, if active low polarity is selected, a synchronous preset would produce low-level outputs, and an asynchronous reset would produce high-level outputs (if enabled).

GAL22CV10 Block Diagram—DIP and SOIC Connections

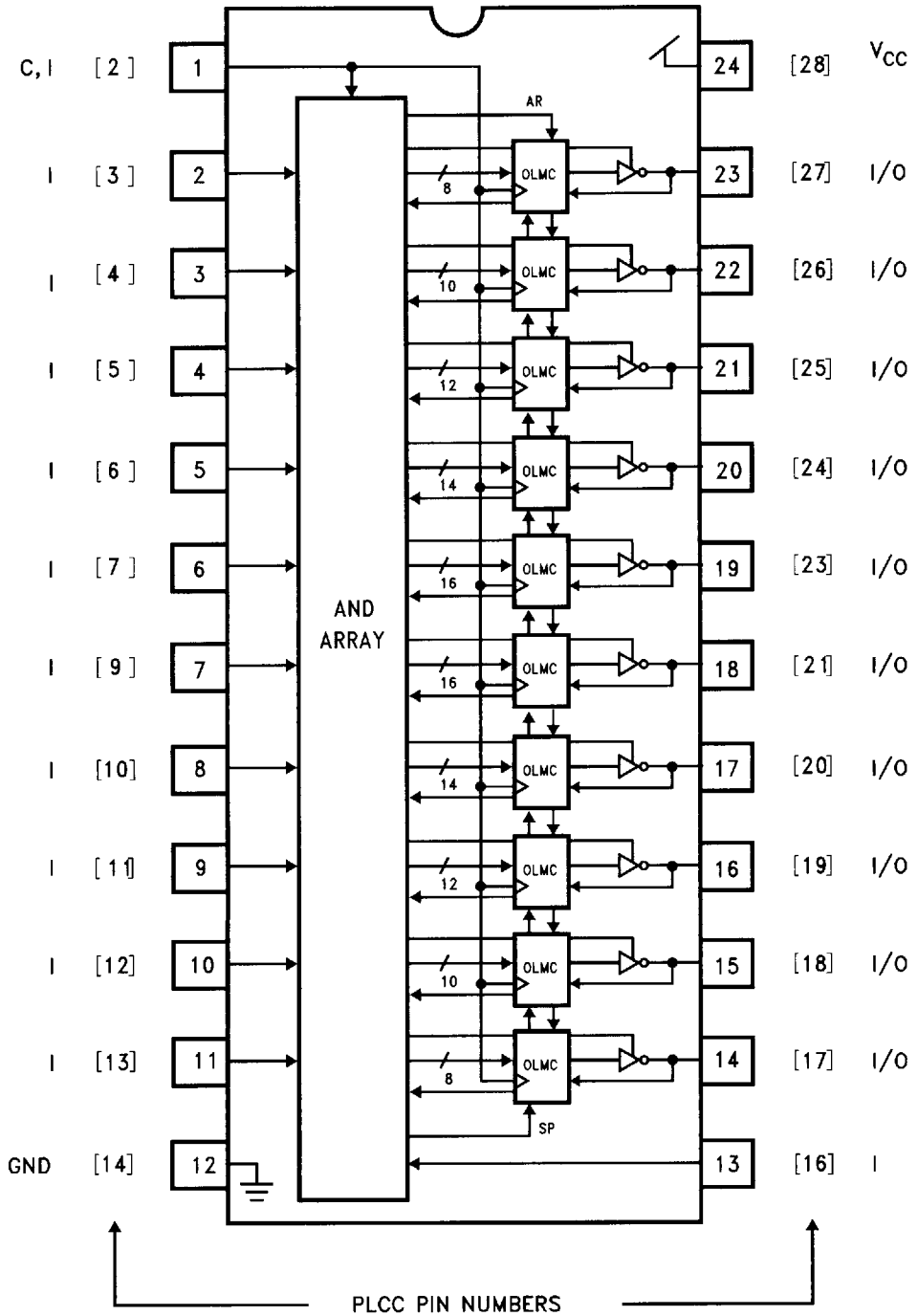

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FIGURE 1

28-Lead PLCC Connection Diagram

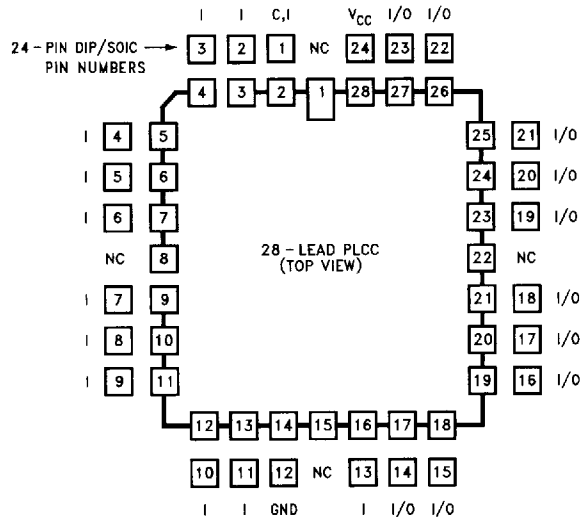

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FIGURE 2

Clock/Input Frequency Specifications

The clock frequency (f_{CLK}) parameter listed in the AC Specifications table specifies the maximum speed at which the GAL22CV10 registers are guaranteed to operate. Clock frequency is defined differently for the two cases in which register feedback is used versus when it is not. In a data-path type application, when the logic functions fed into the registers are not dependent on register feedback from the previous cycle (i.e. based only on external inputs), the minimum required cycle period (f_{CLK}^{-1} without feedback) is defined as the greater of the minimum clock period (t_w high + t_w low) and the minimum "data window" period (t_{SU} + t_H). This assumes optimal alignment between data inputs and the clock input. In sequential logic applications such as state machines, the minimum required cycle period (t_{CYCLE} = f_{CLK}^{-1} with feedback) is defined as t_{CLK} + t_{SU}. This provides sufficient time for outputs from the registers to feed back through the logic array and set up on the inputs to the registers before the end of each cycle.

Design Development Support

A variety of software tools and programming equipment are available to support the development of designs using GAL22CV10 products. Typical software packages, including National's OPAL software, accept Boolean logic equations to define desired functions. Most are available to run on personal computers and generate a JEDEC-compatible "cell-map" (analogous to a PAL "fuse-map"). The industry-standard JEDEC format ensures that the resulting cell-map file can be down-loaded into industry standard programming equipment.

National strongly recommends using only approved programming hardware Programming using unapproved equipment generally voids all guarantees.

The GAL22CV10 can accept fuse-maps prepared for other PAL22V10 devices. PAL22V10 fuse-maps can be created by any JEDEC-compatible PAL development software or by loading the fuse pattern from an existing programmed PAL22V10 device into the programming unit (provided the PAL device has not been secured).

Detailed logic diagrams showing all JEDEC cell-map addresses in the GAL22CV10 logic array and OLMC are provided for direct map editing and diagnostic purposes. *Figures 3* and *4* show details of the OLMC and the programmable architecture cell combinations. *Figure 5* shows the JEDEC logic diagram and details of all programmable cell locations. For a list of current software and programming support tools available for these devices, please contact your local National sales representative or distributor.

Security Cell

A security cell is provided on all GAL22CV10 devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, the circuitry enabling array access is disabled, preventing further programming or verification of the array. The security cell can be erased only in conjunction with the array during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed.

Bulk Erase

The programming equipment automatically performs a bulk erase operation prior to each programming operation. No special erase operation need be performed by the user. Bulk erase clears the logic array, architecture cells and security cell. The GAL device is thereby reverted back to its virgin state.

Manufacturer Testing

Because of EECMOS technology, GAL devices can be reprogrammed. This allows each device to be completely tested by the manufacturer using numerous logic array and architecture patterns prior to shipping. Every programmable cell and every logic path through every device is fully tested for programmability, functionality and performance to all AC and DC parameters. The customer can therefore expect 100% programming and functional yield and 100% compliance of all GAL products to datasheet specifications.

OLMC Logic Diagram

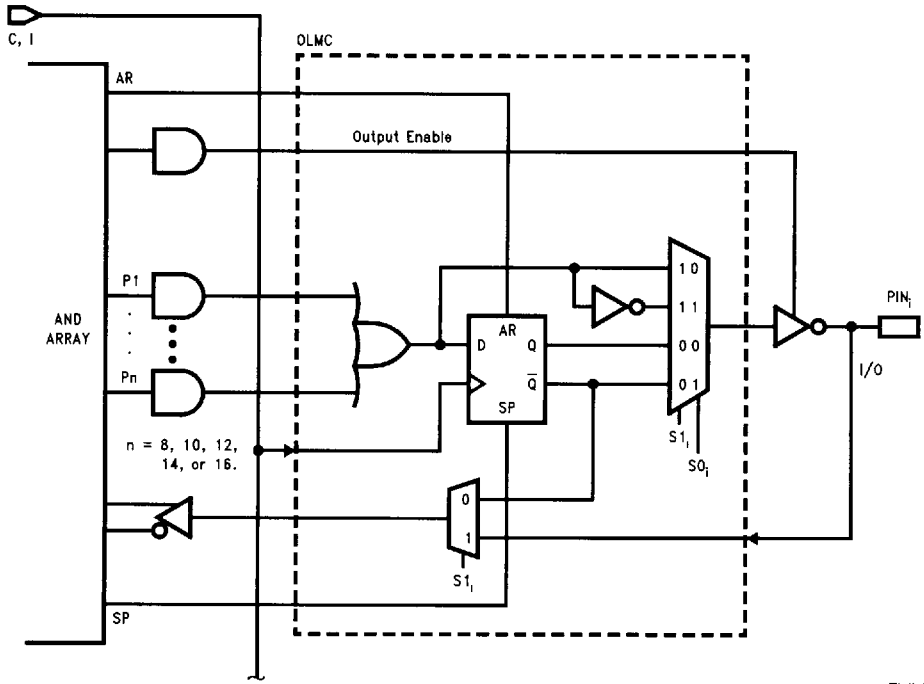

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FIGURE 3

TABLE I

S1	S0	Output Configuration
0	0	Registered/Active Low
0	1	Registered/Active High
1	0	Combinatorial/Active Low
1	1	Combinatorial/Active High

OLMC Selection Table

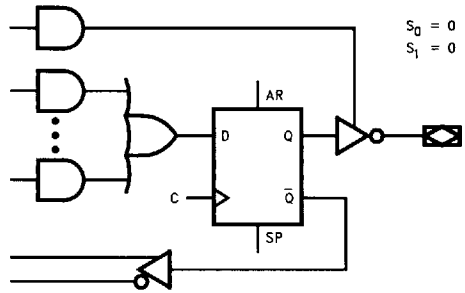

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FIGURE 4-1. Registered/Active Low

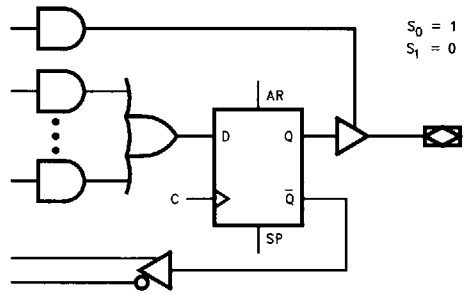

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FIGURE 4-2. Registered/Active High

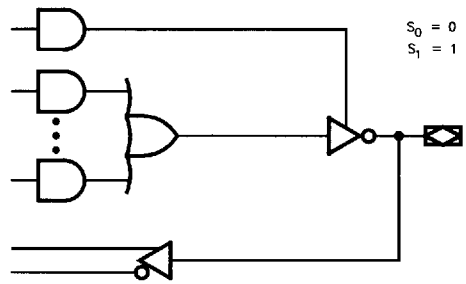

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FIGURE 4-3. Combinatorial/Active Low

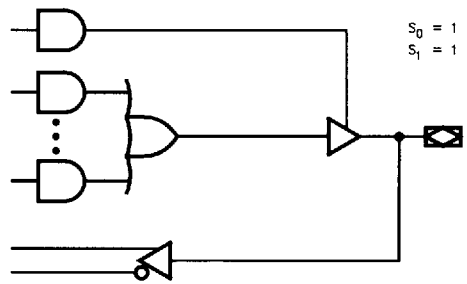

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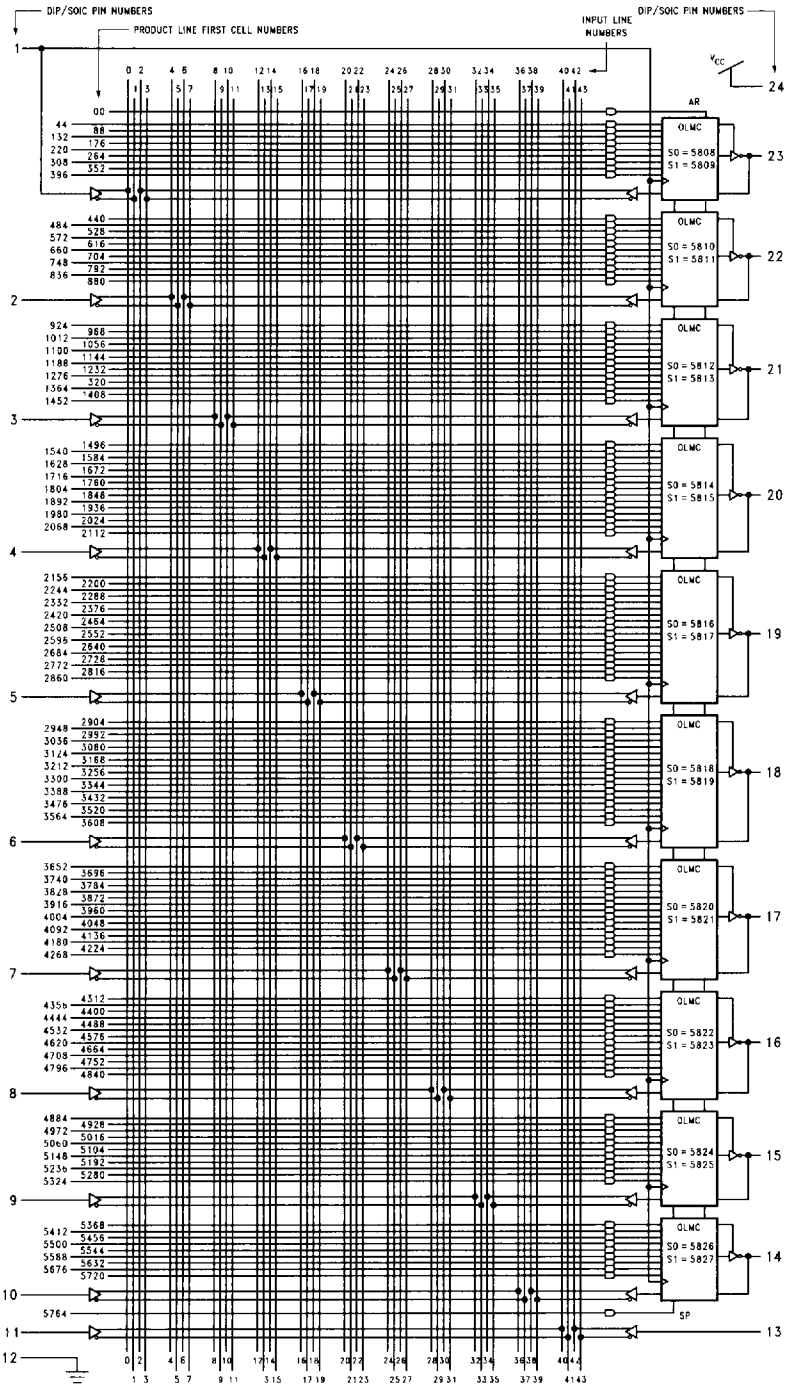
FIGURE 4-4. Combinatorial/Active High

GAL22CV10 Logic Diagram



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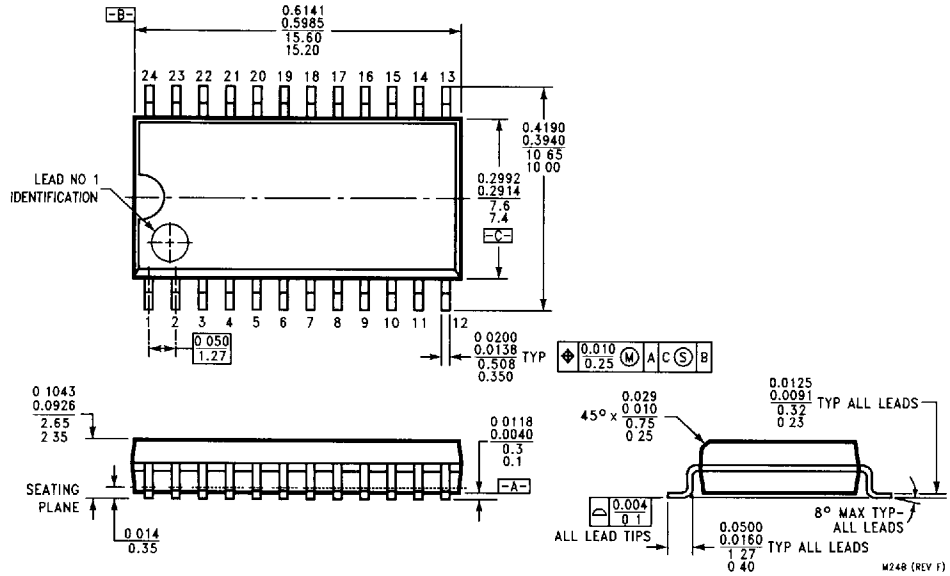
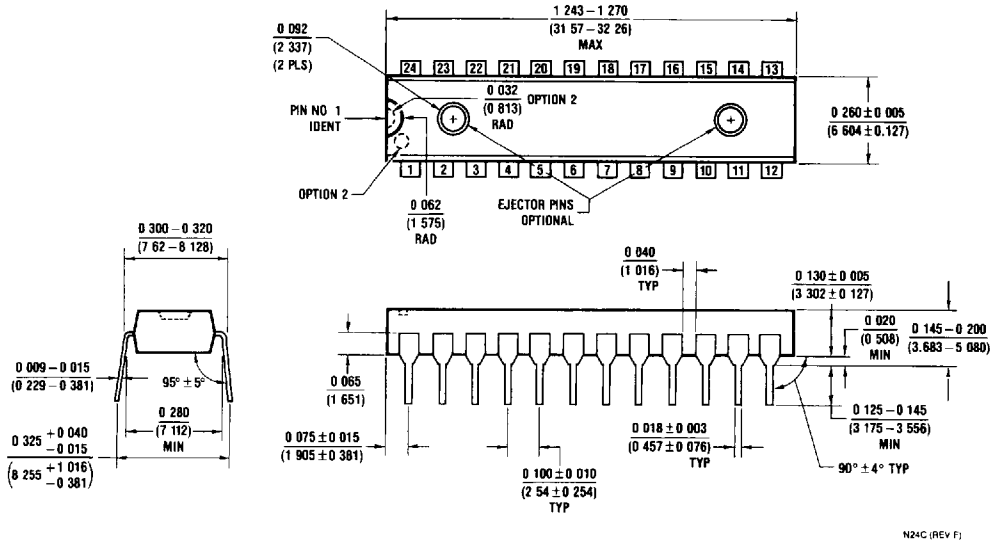
JEDEC Logic Array Cell Numbers = Product Line First Cell Number + Input Line Numbers

FIGURE 5

Physical Dimensions inches (millimeters) (Continued)

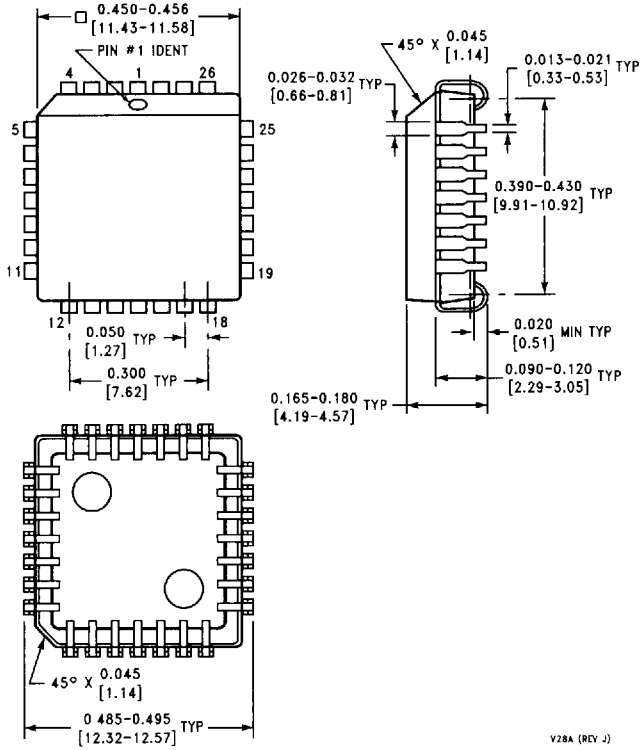


24-Lead Small Outline Integrated Circuit (SOIC) (M)
NS Package Number M24B



24-Lead Narrow Plastic Dual-In-Line Package (N)
NS Package Number N24C

Physical Dimensions inches (millimeters) (Continued)



28-Lead Plastic Chip Carrier (V)
NS Package Number V28A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
2900 Semiconductor Drive
P O Box 58090
Santa Clara CA 95052-8090
Tel 1(800) 272 9959
TWX (910) 339 9240

National Semiconductor GmbH
Industriestrasse 10
D-8080 Fürstenfeldbruck
Germany
Tel (0-81-41) 103-0
Telex 527649
Fax (0-81-41) 10 35-06

National Semiconductor Japan Ltd.
Sanseido Bldg 5F
4-15-3 Nishi Shinjuku
Shinjuku-Ku,
Tokyo 160, Japan
Tel 3 3299 7001
FAX 3 3299 7000

National Semiconductor Hong Kong Ltd
13th Floor, Straight Block
Ocean Centre 5 Canton Rd
Tsimshatsui, Kowloon
Hong Kong
Tel (852) 737 1600
Telex 51292 NSHKL
Fax (852) 736 9960

National Semiconductores Do Brazil Ltda.
Av. Brig Faria Lima, 1409
6 Andar
Cep 01451, Paulistano
Sao Paulo SP Brazil
Tel (55-11) 212-5066
Telex 391 1131931 NSBR BR
Fax (55-11) 212 1181

National Semiconductor (Australia) Pty. Ltd
16 Business Park Dr
Notting Hill VIC 3168
Australia
Tel (3) 558-9999
Fax (3) 558 9998