August 29, 2011

LMH2180

75 MHz Dual Clock Buffer

General Description

The LMH2180 is a high speed dual clock buffer designed for portable communications and applications requiring multiple accurate multi-clock systems. The LMH2180 integrates two 75 MHz low noise buffers with independent shutdown pins into a small package. The LMH2180 ensures superb system operation between the baseband and the oscillator signal path by eliminating crosstalk between the multiple clock signals.

Unique technology and design provides the LMH2180 with the ability to accurately drive both large capacitive and resistive loads. Low supply current combined with shutdown pins for each channel means the LMH2180 is ideal for battery powered applications. This part does not use an internal ground reference, thus providing additional system flexibility.

The flexible buffers provide system designers the capacity to manage complex clock signals in the latest wireless applications. Each buffer delivers 106 V/µs internal slew rate with independent shutdown and duty cycle precision. Each input is internally biased to 1V, removing the need for external resistors. Both channels have rail-to-rail inputs and outputs, a gain of one, and are AC coupled with the use of one capacitor.

Replacing a discrete buffer solution with the LMH2180 provides many benefits: simplified board layout, minimized parasitic components, simplified BOM, design durability across multiple applications, simplification of clock paths, and the ability to reduce the number of clock signal generators in the system. The LMH2180 is produced in the tiny packages minimizing the required PCB space.

Features

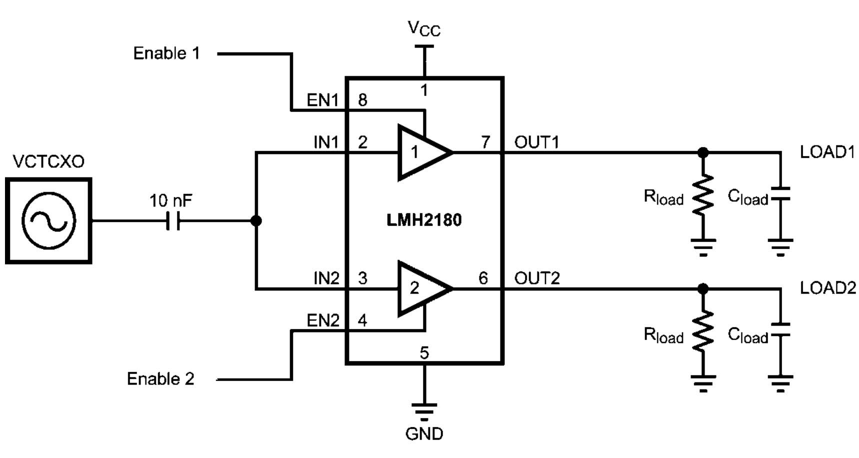
(Typical values are: V_{SUPPLY} = 2.7V and C_L = 10 pF, unless otherwise specified.)

- Small signal bandwidth 78 MHz
- Supply voltage range 2.4V to 5V
- Phase noise (V_{IN} = 1 V_{PP}, f_C = 38.4 MHz, Δf = 1 kHz) −123 dBc/Hz
- Slew rate 106 V/µs
- Total supply current 2.3 mA
- Shutdown current 30 µA
- Rail-to-rail input and output
- Individual buffer enable pins
- Rapid T_{on} technology
- Crosstalk rejection circuitry
- Packages:
  - 8-Pin LLP, Solder Bump and no Pullback
  - 8-Bump micro SMD
- Temperature range −40°C to 85°C

Applications

- 3G mobile applications
- WLAN–WiMAX modules
- TD_SCDMA multi-mode MP3 and camera
- GSM modules
- Oscillator modules

Typical Application



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltages ($V^+ - V^-$)	5.5V
ESD Tolerance	
Human Body (Note 4)	2000V
Machine Model (Note 5)	200V
Charged Device Model	1000V
Storage Temperature Range	−65°C to 150°C
Junction Temperature (Note 3)	150°C
Soldering Information	
Infrared or Convection (35 sec.)	235°C

Operating Ratings (Note 1)

Supply Voltage ($V^+ - V^-$)	2.4V to 5.0V
Temperature Range (Note 2, Note 3)	−40°C to 85°C
Package Thermal Resistance (Note 2, Note 3)	
8-Pin LLP (θ_{JA})	217°C/W
8-Bump micro SMD (θ_{JA})	90°C/W

2.7V Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V_{DD} = 2.7V, V_{SS} = 0V, V_{CM} = 1V, $Enable_{1,2} = V_{DD}$, C_L = 10 pF, R_L = 30 kΩ, Load is connected to V_{SS}, $C_{COUPLING}$ = 10 nF. **Boldface** limits apply at temperature range extremes of operating condition. See (Note 2)

Symbol	Parameter	Conditions	Min (Note 7)	Typ (Note 6)	Max (Note 7)	Units
Frequency Domain Response						
SSBW	Small Signal Bandwidth	V_{IN} = 100 mV_{PP}; −3 dB		78		MHz
LSBW	Large Signal Bandwidth	V_{IN} = 1.0 V_{PP}; −3 dB		60		MHz
GFN	Gain Flatness < 0.1 dB	f > 100 kHz		4.9		MHz
Distortion and Noise Performance						
φ_n	Phase Noise	V_{IN} = 1 V_{PP}, f_C = 38.4 MHz, Δf = 1 kHz		−123		dBc/Hz
		V_{IN} = 1 V_{PP}, f_C = 38.4 MHz, Δf = 10 kHz		−132		dBc/Hz
e_n	Input-Referred Voltage Noise	f = 1 MHz, R_{SOURCE} = 50Ω		13		$nV/\sqrt{Hz}$
$I_{SOLATION}$	Output to Input	f = 1 MHz, R_{SOURCE} = 50Ω		84		dB
CT	Crosstalk Rejection	f = 38.4 MHz, V_{IN} = 1 V_{PP}		41		dB
Time Domain Response						
t_r	Rise Time	0.1 V_{PP} Step (10-90%)		6		ns
t_f	Fall Time			5		ns
t_s	Settling Time to 0.1%	1 V_{PP} Step		120		ns
OS	Overshoot	0.1 V_{PP} Step		37		%
SR	Slew Rate (Note 8)	V_{IN} = 2 V_{PP}		106		V/μs
Static DC Performance						
I_S	Supply Current	$Enable_{1,2} = V_{DD}$; No Load		2.3	2.7 **2.9**	mA
		$Enable_1 = V_{DD}$, $Enable_2 = V_{SS}$, No Load		1.3	1.5 **1.6**	mA
		$Enable_{1,2} = V_{SS}$; No Load		30	41 **46**	μA
PSRR	Power Supply Rejection Ratio	DC (3.0V to 5.0V)	65 **64**	68		dB
A_{CL}	Small Signal Voltage Gain	V_{IN} = 0.2 V_{PP}	**0.95**	1.0	**1.05**	V/V
V_{OS}	Output Offset Voltage			-0.5	17 **18**	mV
TC V_{OS}	Temperature Coefficient Output Offset Voltage (Note 9)			2.8		μV/°C
R_{OUT}	Output Resistance	f = 100 kHz		0.6		Ω
		f = 38.4 MHz		166		
		disabled		High Impedance		

Symbol	Parameter	Conditions	Min (Note 7)	Typ (Note 6)	Max (Note 7)	Units
Miscellaneous Performance						
R_{IN}	Input Resistance per Buffer	Enable = V_{DD}		137		kΩ
		Enable = V_{SS}		137		
C_{IN}	Input Capacitance per Buffer	Enable = V_{DD}		1.3		pF
		Enable = V_{SS}		1.3		
Z_{IN}	Input Impedance	f = 38.4 MHz, Enable = V_{DD}		4.5		kΩ
		f = 38.4 MHz, Enable = V_{SS}		4.2		
V_O	Output Swing Positive	$V_{IN} = V_{DD}$	2.66 **2.65**	2.69		V
	Output Swing Negative	$V_{IN} = V_{SS}$		19	35 **37**	mV
I_{SC}	Output Short-Circuit Current (Note 10, Note 11)	Sourcing, $V_{IN} = V_{DD}$, $V_{OUT} = V_{SS}$	−21 **−18**	−25		mA
		Sinking, $V_{IN} = V_{SS}$, $V_{OUT} = V_{DD}$	23 **15**	25		
V_{en_hmin}	Enable High Active Minimum Voltage			1.2		V
V_{en_lmax}	Enable Low Inactive Maximum Voltage			0.6		

5V Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for $T_A = 25°C$, $V_{DD} = 5V$, $V_{SS} = 0V$, $V_{CM} = 1V$, $Enable_{1,2} = V_{DD}$, $C_L = 10$ pF, $R_L = 30$ kΩ, Load is connected to V_{SS}, $C_{COUPLING} = 10$ nF. **Boldface** limits apply at temperature range extremes of operating condition. See (Note 2)

Symbol	Parameter	Conditions	Min (Note 7)	Typ (Note 6)	Max (Note 7)	Units
Frequency Domain Response						
SSBW	Small Signal Bandwidth	$V_{IN} = 100\ mV_{PP}$; −3 dB		87		MHz
LSBW	Large Signal Bandwidth	$V_{IN} = 1.0\ V_{PP}$; −3 dB		68		MHz
GFN	Gain Flatness < 0.1 dB	f > 100 kHz		25		MHz
Distortion and Noise Performance						
φ_n	Phase Noise	$V_{IN} = 1\ V_{PP}$, $f_C = 38.4$ MHz, Δf = 1 kHz		−123		dBc/Hz
		$V_{IN} = 1\ V_{PP}$, $f_C = 38.4$ MHz, Δf = 10 kHz		−132		dBc/Hz
e_n	Input-Referred Voltage Noise	f = 1 MHz, $R_{SOURCE} = 50Ω$		12		$nV/\sqrt{Hz}$
$I_{SOLATION}$	Output to Input	f = 1 MHz, $R_{SOURCE} = 50Ω$		84		dB
CT	Crosstalk Rejection	f = 38.4 MHz, $P_{IN} = 0$ dBm		59		dB
Time Domain Response						
t_r	Rise Time	0.1 V_{PP} Step (10-90%)		6		ns
t_f	Fall Time			6		ns
t_s	Settling Time to 0.1%	1 V_{PP} Step		70		ns
OS	Overshoot	0.1V_{PP} Step		13		%
SR	Slew Rate (Note 8)	$V_{IN} = 2\ V_{PP}$		124		V/μs
Static DC Performance						
I_S	Supply Current	$Enable_{1,2} = V_{DD}$; No Load		3.4	4.0 **4.1**	mA
		$Enable_1 = V_{DD}$, $Enable_2 = V_{SS}$; No Load		1.8	2.2 **2.3**	mA
		$Enable_{1,2} = V_{SS}$; No Load		32	43 **49**	μA

Symbol	Parameter	Conditions	Min (Note 7)	Typ (Note 6)	Max (Note 7)	Units
PSRR	Power Supply Rejection Ratio	DC (3.0V to 5.0V)	65 **64**	68		dB
A_{CL}	Small Signal Voltage Gain	V_{IN} = 0.2 V_{PP}	**0.95**	1.0	**1.05**	V/V
V_{OS}	Output Offset Voltage			−1.4	21 **22**	mV
TC V_{OS}	Temperature Coefficient Output Offset Voltage (Note 9)			2.4		µV/°C
R_{OUT}	Output Resistance	f = 100 kHz		0.5		Ω
		f = 38.4 MHz		126		
		disabled	High Impedance			
Miscellaneous Performance						
R_{IN}	Input Resistance per Buffer	Enable = V_{DD}		138		kΩ
		Enable = V_{SS}		138		
C_{IN}	Input Capacitance per Buffer	Enable = V_{DD}		1.3		pF
		Enable = V_{SS}		1.3		
Z_{IN}	Input Impedance	f = 38.4 MHz, Enable = V_{DD}		4.3		kΩ
		f = 38.4 MHz, Enable = V_{SS}		4.2		
V_O	Output Swing Positive	V_{IN} = V_{DD}	4.96 **4.95**	4.99		V
	Output Swing Negative	V_{IN} = V_{SS}		10	35 **50**	mV
I_{SC}	Output Short-Circuit Current (Note 10, Note 11)	Sourcing, V_{IN} = V_{DD}, V_{OUT} = V_{SS}	−80 **−62**	−90		mA
		Sinking, V_{IN} = V_{SS}, V_{OUT} = V_{DD}	60 **43**	65		
V_{en_hmin}	Enable High Active Minimum Voltage			1.2		V
V_{en_lmax}	Enable Low Inactive Maximum Voltage			0.6		

Note 1: “Absolute Maximum Ratings” indicate limits beyond which damage to the device may occur, including inoperability and degradation of the device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{J(MAX)}$, θ_{JA} , and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in the *Absolute Maximum Ratings*, whichever is lower.

Note 4: Human body model, applicable std. JESD22–A114C.

Note 5: Machine model, applicable std. JESD22–A115–A.

Note 6: Typical values represent the most likely parametric norms at T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 7: Datasheet min/max specification limits are guaranteed by test or statistical analysis.

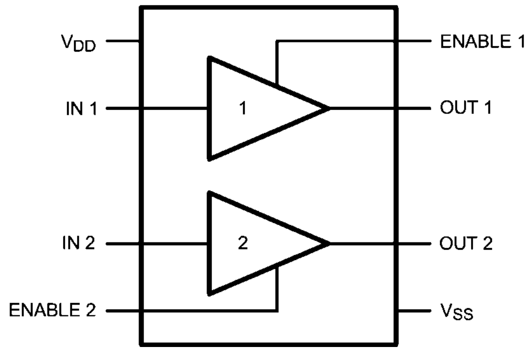
Note 8: Slew rate is the average of the rising and falling slew rates.

Note 9: Average Temperature Coefficient is determined by dividing the changing in a parameter at temperature extremes by the total temperature change.

Note 10: Short–Circuit test is a momentary test. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 11: Positive current corresponds to current flowing into the device.

Block Diagram



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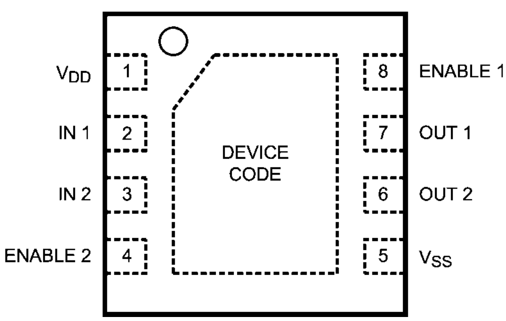
Pin Descriptions

Pin No. LLP	Pin No. microSMD	Pin Name	Description
1	A3	V_{DD}	Voltage supply connection
2	A2	IN 1	Input 1
3	A1	IN 2	Input 2
4	B1	ENABLE 2	Enable buffer 2
5	C1	V_{SS}	Ground connection
6	C2	OUT 2	Output 2
7	C3	OUT 1	Output 1
8	B3	ENABLE 1	Enable buffer 1

Connection Diagrams

8-Pin LLP



Top View

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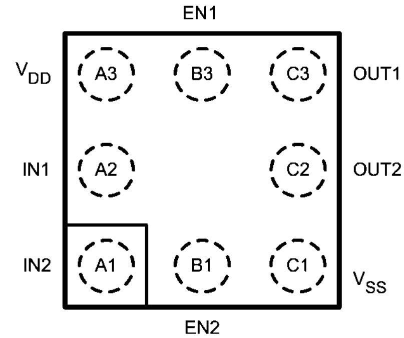
8-Bump micro SMD



Top View

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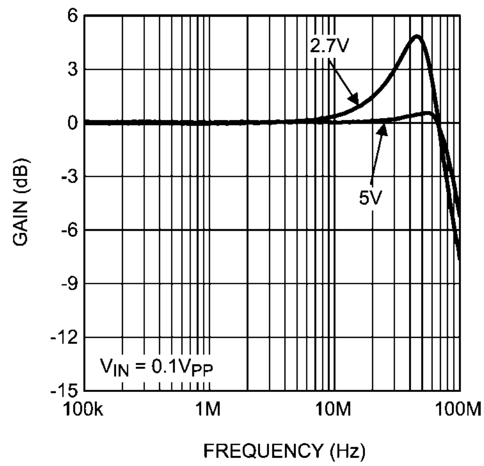
Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
8-Pin LLP Solder Bump	LMH2180YD	2180Y	1k Units Tape and Reel	YDA08A
	LMH2180YDX		4.5k Units Tape and Reel	
8-Pin LLP No Pullback	LMH2180SD	2180S	1k Units Tape and Reel	SDA08A
	LMH2180SDE		250 Units Tape and Reel	
	LMH2180SDX		4.5k Units Tape and Reel	
8-Bump micro SMD	LMH2180TM	CA	250 Units Tape and Reel	TMD08AAA
	LMH2180TMX		3k Units Tape and Reel	

Typical Performance Characteristics

T_A = 25°C, V_{DD} = 2.7V, V_{SS} = 0V, $Enable_{1,2}$ = V_{DD}, C_L = 10 pF, R_L = 30 kΩ and $C_{COUPLING}$ = 10 nF, unless otherwise specified.

Frequency Response



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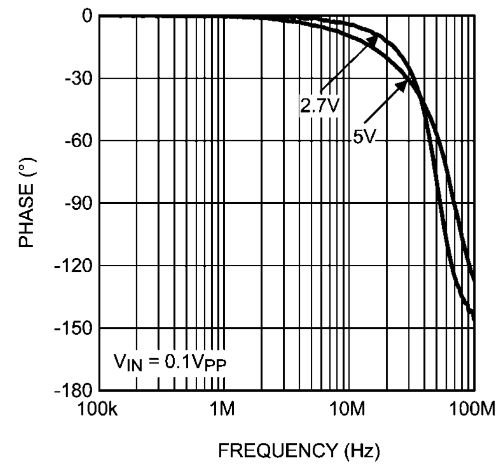
Phase Response



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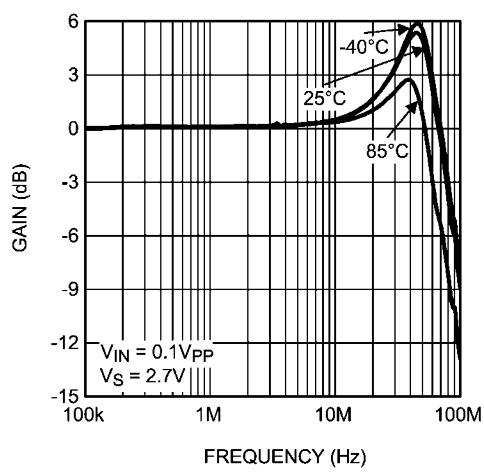
Frequency Response Over Temperature



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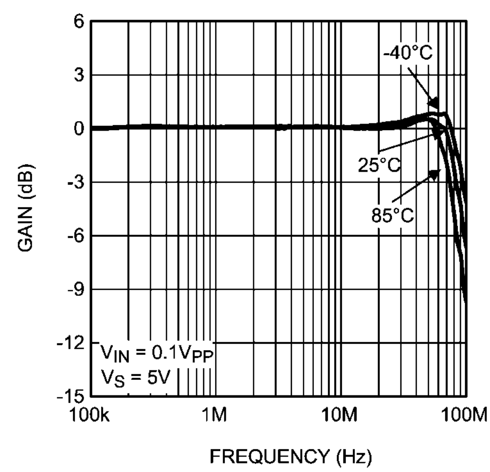
Frequency Response Over Temperature



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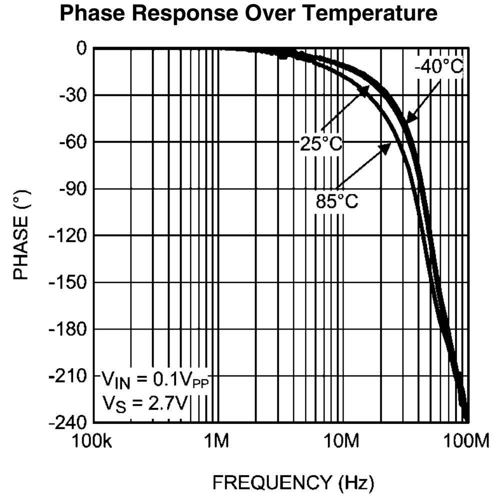
Phase Response Over Temperature



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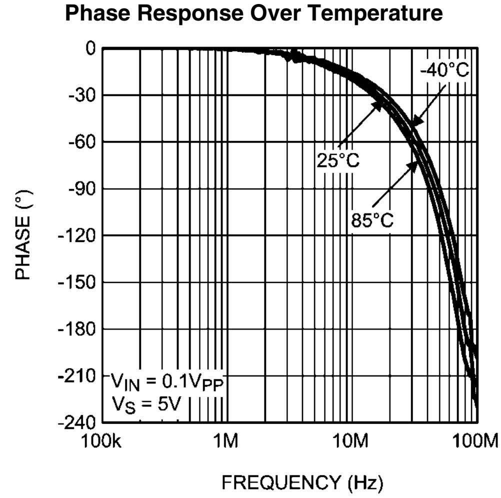
Phase Response Over Temperature



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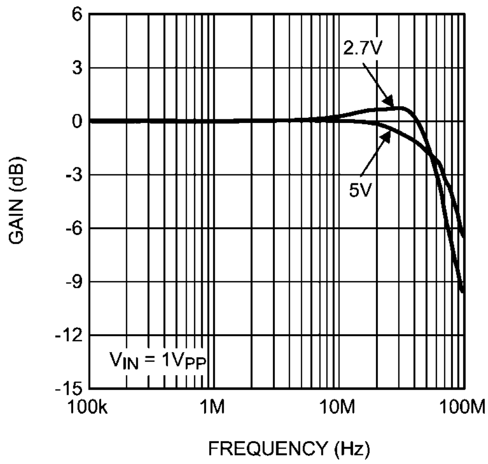
Large Signal Bandwidth



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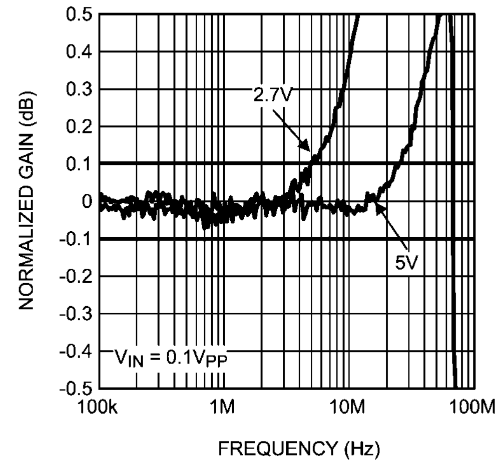
Gain Flatness < 0.1 dB (GFN)



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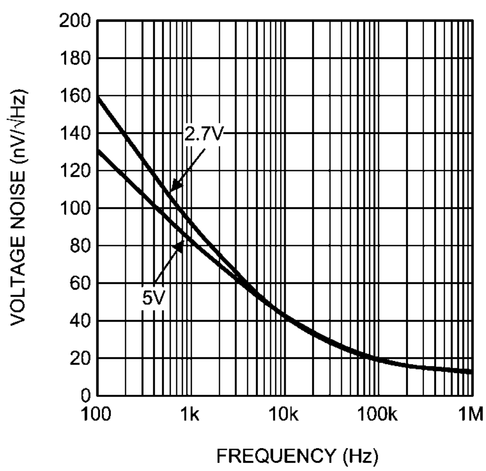
Voltage Noise



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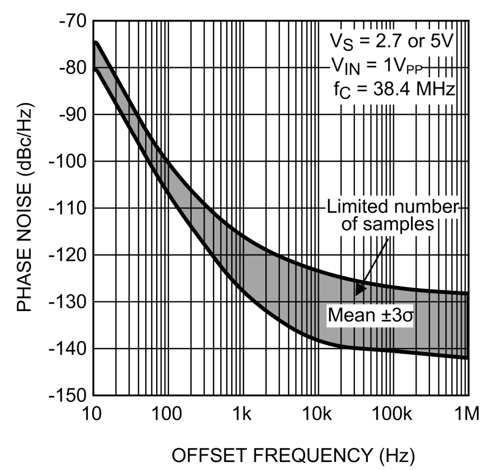
Phase Noise



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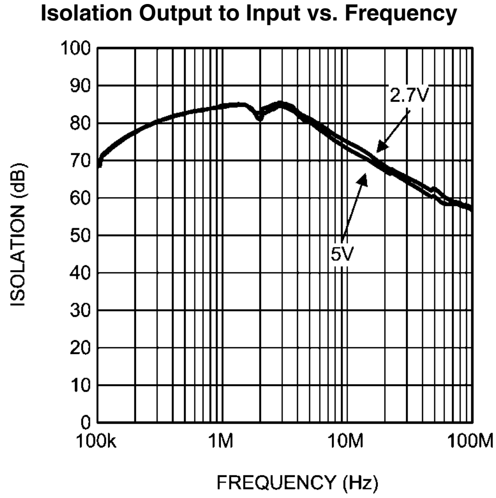
Isolation Output to Input vs. Frequency



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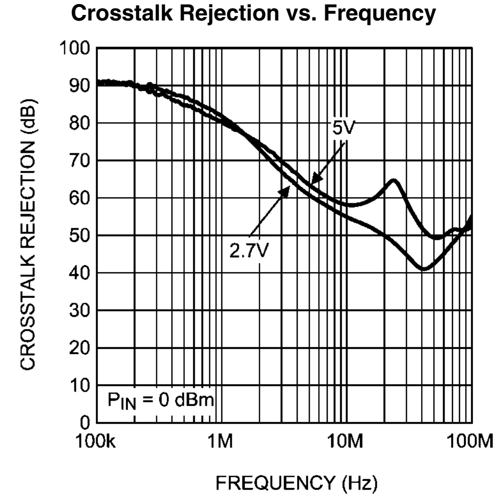
Crosstalk Rejection vs. Frequency



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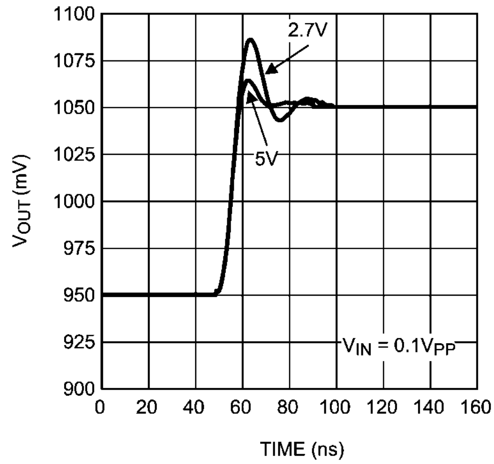
Transient Response Positive



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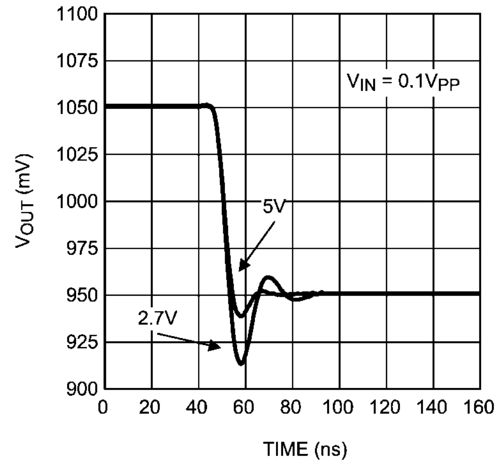
Transient Response Negative



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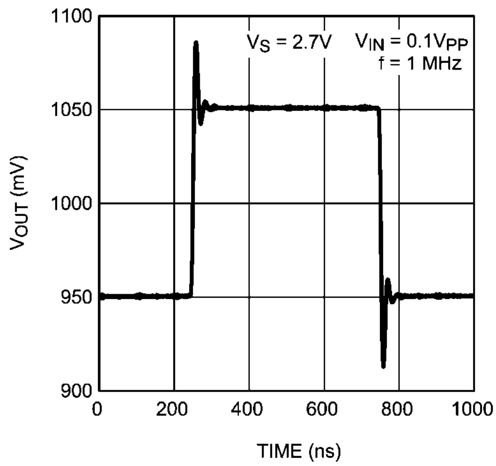
Small Signal Pulse Response



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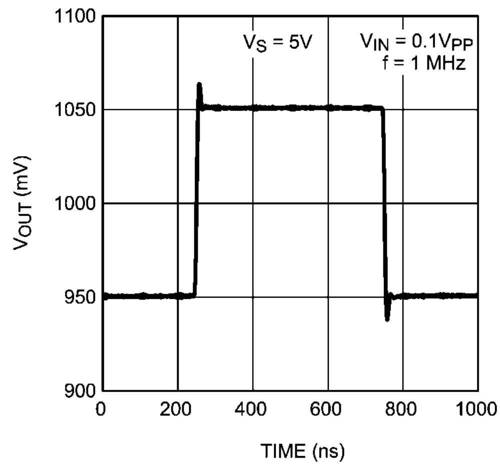
Small Signal Pulse Response



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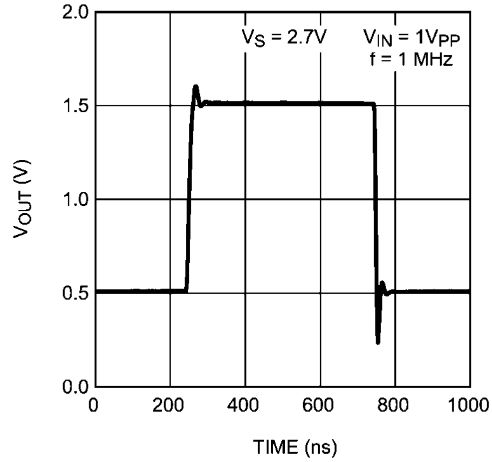
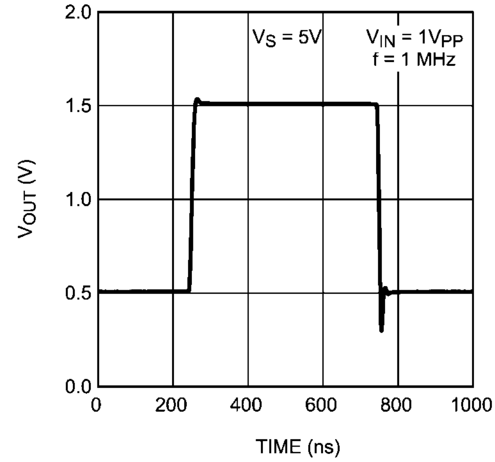
Large Signal Response



30024619

Large Signal Response



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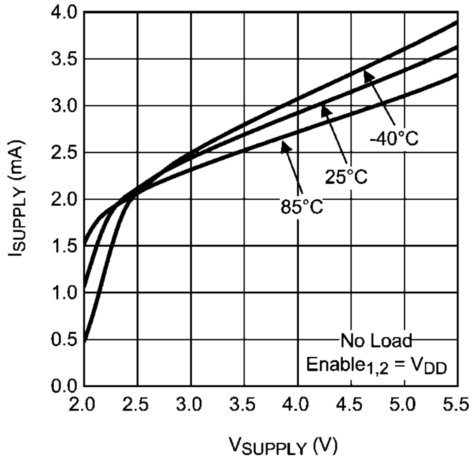
I_{SUPPLY} vs. V_{SUPPLY}



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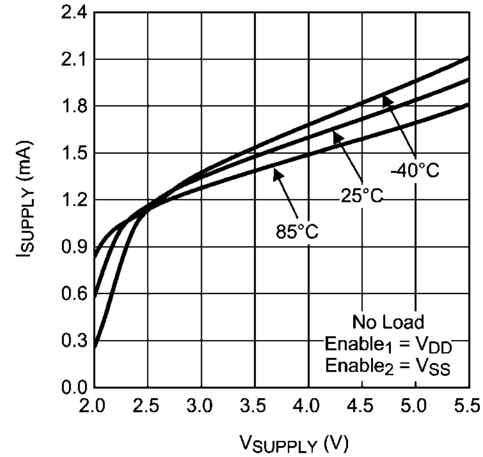
I_{SUPPLY} vs. V_{SUPPLY}



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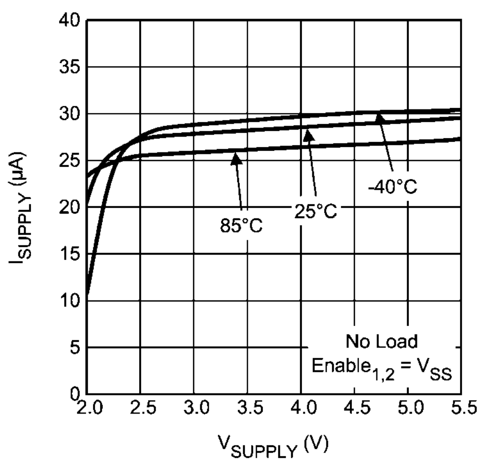
I_{SUPPLY} vs. V_{SUPPLY}



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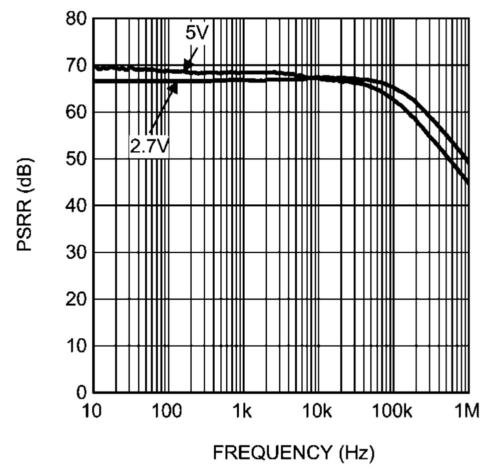
PSRR vs. Frequency



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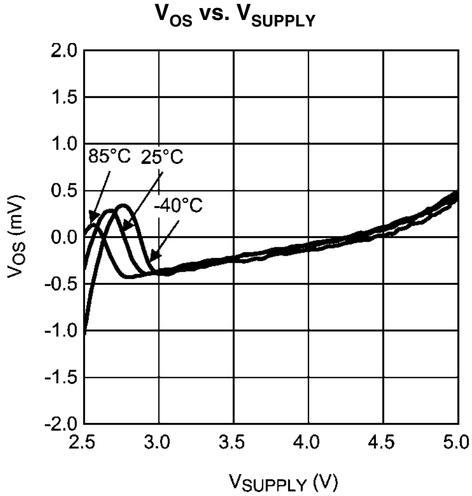
V_{OS} vs. V_{SUPPLY}



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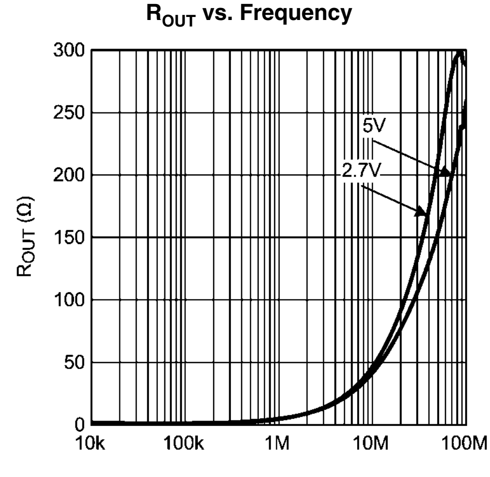
R_{OUT} vs. Frequency



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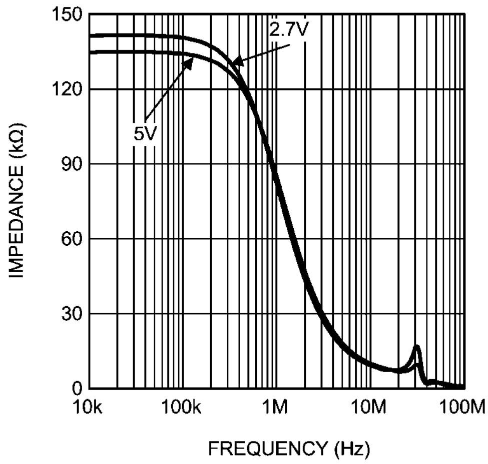
Input Impedance vs. Frequency



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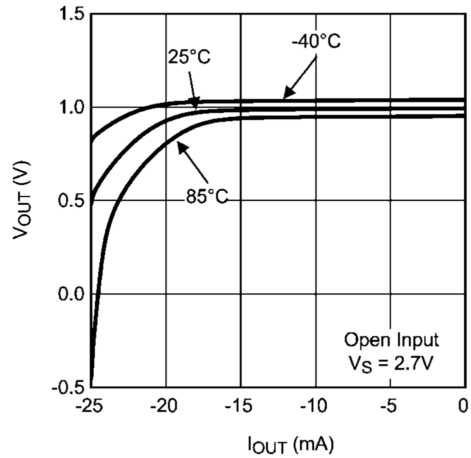
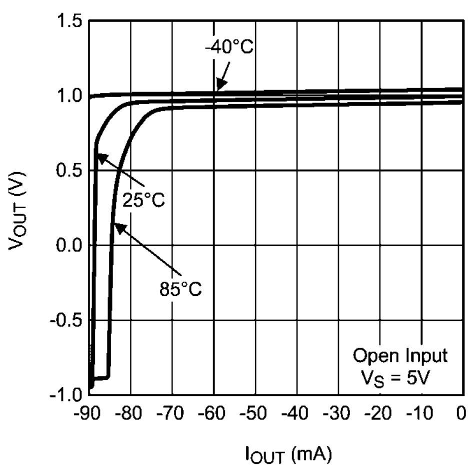
V_{OUT} vs. I_{OUT} (Sourcing)



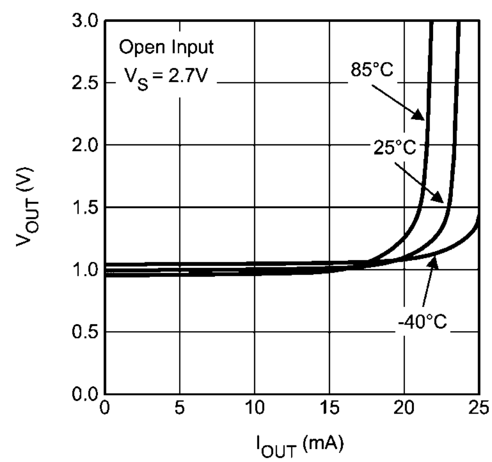
30024628

V_{OUT} vs. I_{OUT} (Sourcing)



30024629

V_{OUT} vs. I_{OUT} (Sinking)



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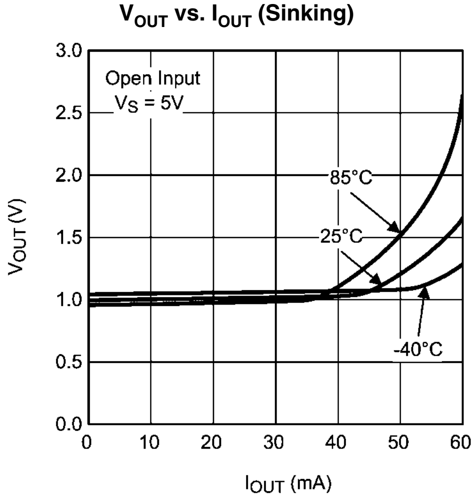
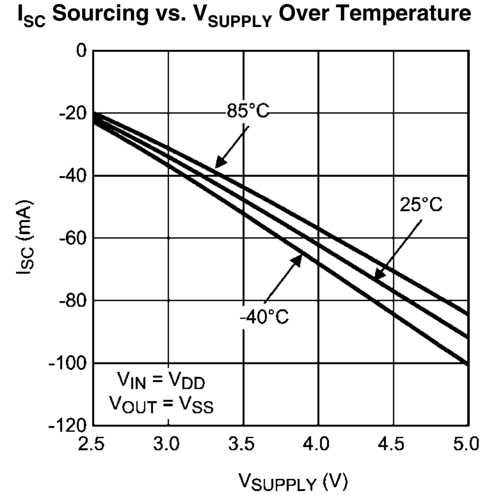
V_{OUT} vs. I_{OUT} (Sinking)



30024632

I_{SC} Sourcing vs. V_{SUPPLY} Over Temperature



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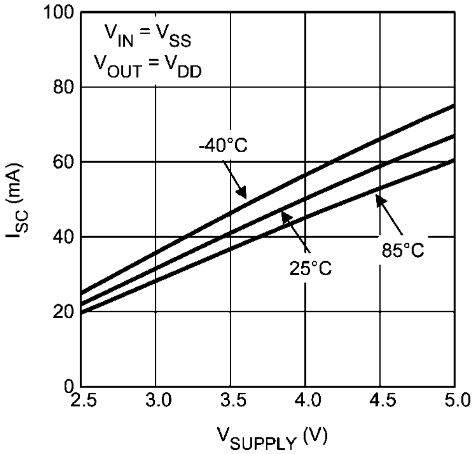
I_{SC} Sinking vs. V_{SUPPLY} Over Temperature



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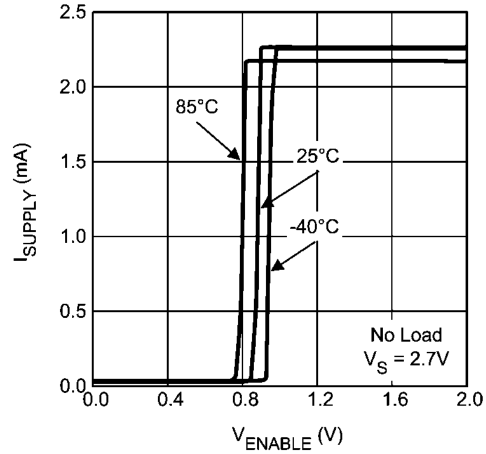
I_{SUPPLY} vs. V_{ENABLE}



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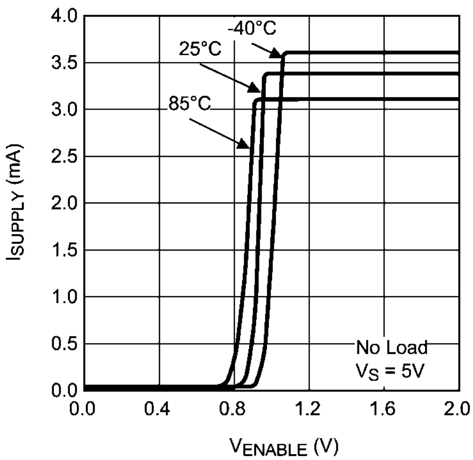
I_{SUPPLY} vs. V_{ENABLE}



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Application Information

GENERAL

The LMH2180 is designed to minimize the effects of spurious signals from the base chip to the oscillator. Also the influence of varying load resistance and capacitance to the oscillator is minimized, while the drive capability is increased.

The inputs of the LMH2180 are internally biased at 1V, making AC coupling possible without external bias resistors.

To optimize current consumption, a buffer that is not in use can be disabled by connecting it's enable pin to V_{SS}.

The LMH2180 has no internal ground reference; therefore, either single or split supply configurations can be used.

The LMH2180 is an easy replacement for discrete circuitry. It simplifies board layout and minimizes the effect of layout related parasitic components.

INPUT CONFIGURATION

The internal 1V input biasing allows AC coupling of the input signal. This biasing avoids the use of external resistors, as depicted in *Figure 1*. The biasing prevents a large DC load at the oscillators output that creates a load impedance and may affect it's oscillating frequency. As a result of this biasing, the maximum amplitude of the AC signal is $2V_{PP}$.

The coupling capacitance C1 should be large enough to let the AC signal pass. This is a unity gain buffer with rail-to-rail inputs and outputs.

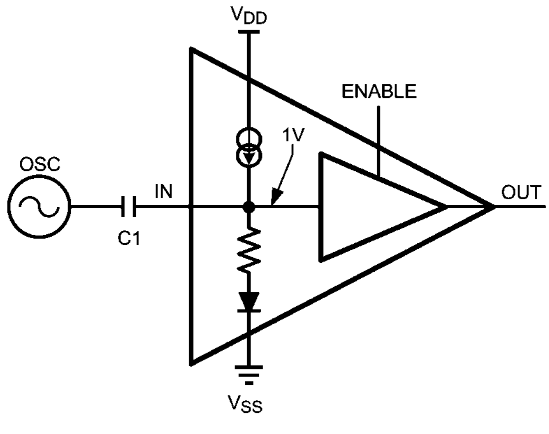


FIGURE 1. Input Configuration

FREQUENCY PULLING

Frequency pulling is the frequency variation of an oscillator caused by a varying load. In the typical application, the load of the oscillator is a fixed capacitor (C1) in series with the input impedance of the buffer.

To keep the input impedance as constant as possible, the input is biased at 1V, even when the part is disabled. A simplified schematic of the input configuration is shown in *Figure 1*.

ISOLATION AND CROSSTALK

Output to input isolation prevents the clock signal of the oscillator from being affected by spurious signals generated by the digital blocks behind the output buffer. See the characteristic graphic entitled Isolation Output to Input vs. Frequency.

A block diagram of the isolation is shown in *Figure 2*. Crosstalk rejection between buffers prevents signals from affecting each other. *Figure 2* shows a Baseband IC and a Bluetooth module as an example. See the characteristic graphic labeled Crosstalk Rejection vs. Frequency for more information.

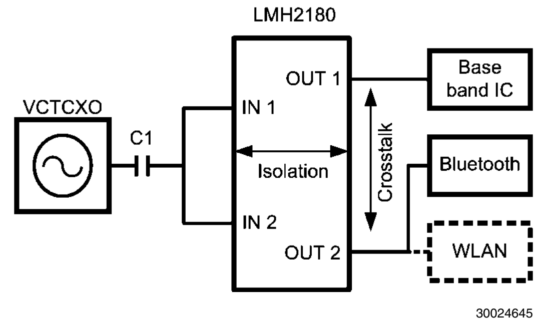


FIGURE 2. Isolation Block Diagram

DRIVING CAPACITIVE LOADS

Each buffer can drive a capacitive load. Be aware that every capacitor directly connected to the output becomes part of the loop of the buffer. In most applications the load consists of the capacitance of copper tracks and the input capacitance of the application blocks. Capacitance reduces the gain/phase margin and decreases the stability. This leads to peaking in the frequency response and in extreme situations oscillations can occur. To drive a large capacitive load it is recommended to include a series resistor between the buffer and the load capacitor. The best value for this isolation resistance can be found by experimentation.

The LMH2180 datasheet reflects measurements with capacitive loads of 10 pF at the output of the buffers. Most common applications will probably use a lower capacitive load, which will result in lower peaking and significantly greater bandwidth, see *Figure 3*.

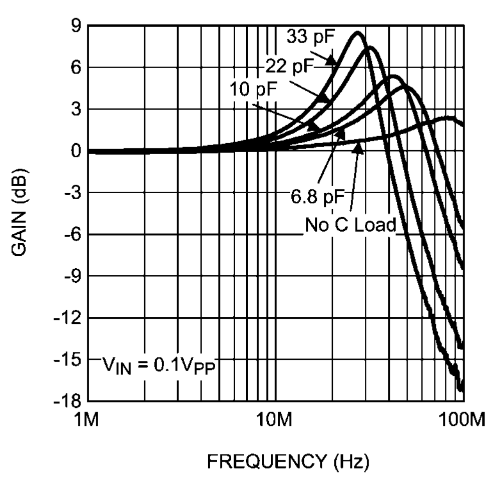


FIGURE 3. Bandwidth and Peaking

PHASE NOISE

A clock buffer adds noise to the clock signal. This noise causes uncertainty in the phase of the clock signal. This uncertainty is described by jitter (time domain) or phase noise (frequency domain). Communication systems, such as Wireless LAN, require a low jitter/phase noise clock signal to obtain a low Bit Error Rate. *Figure 4* shows the frequency domain representation of a clock signal with frequency f_C. Without Phase Noise the entire signal power would only be located at the frequency f_C. Phase Noise spreads some of the power to adjacent frequencies. Phase Noise is usually specified in dBc/Hz at a given frequency offset Δf from the carrier, where dBc is the power level in dB relative to the carrier. The noise power is measured within a 1 Hz bandwidth.

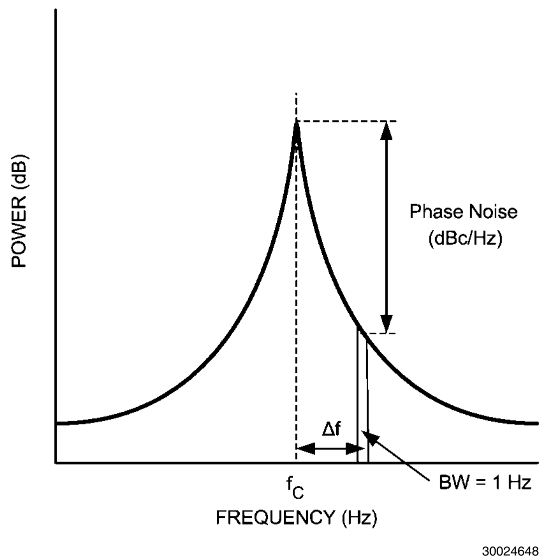


FIGURE 4. Phase Noise

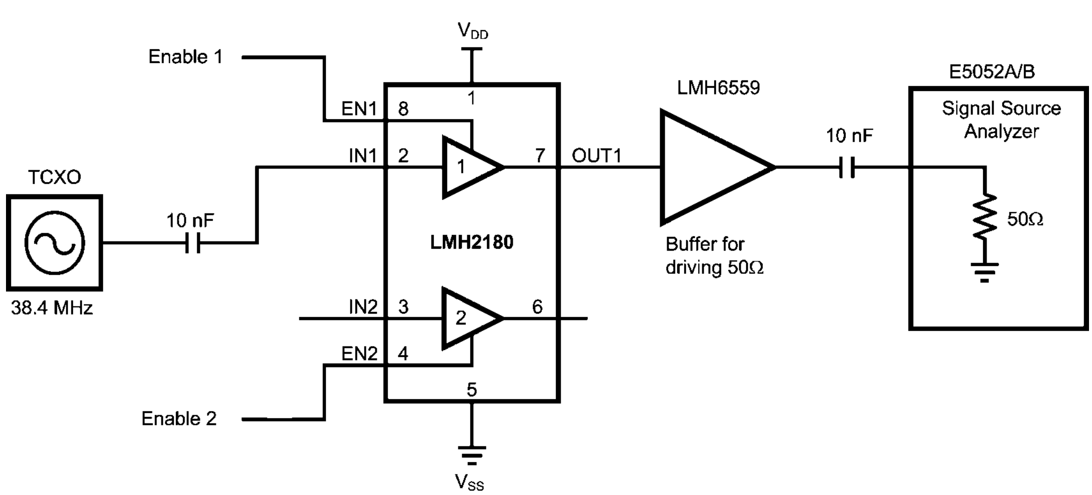


FIGURE 5. Measurement Setup

Figure 5 shows the setup used to measure the LMH2180 phase noise. The clock driving the LMH2180 is a state of the art 38.4MHz TCXO. Both the TCXO phase noise and the phase noise at the LMH2180 output were measured. At offset frequencies of 1 kHz and higher from the carrier, the TCXO phase noise is sufficiently low to accurately calculate the LMH2180 contribution to the phase noise at the output. The LMH6559, whose phase noise contribution can be neglected, is used to drive the 50Ω input impedance of the Signal Source Analyzer.

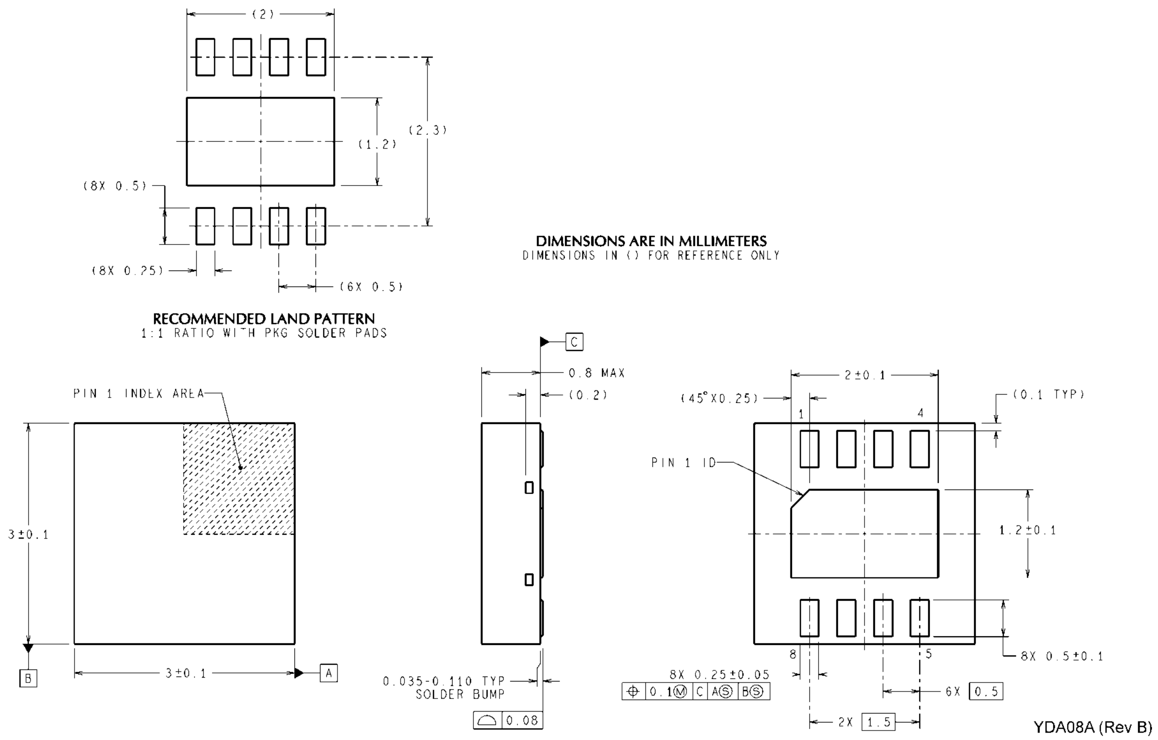
LAYOUT DESIGN RECOMMENDATION

Careful consideration during circuit design and PCB layout will eliminate problems and will optimize the performance of the LMH2180. It is best to have the same ground plane on the PCB for all decoupling and other ground connections.

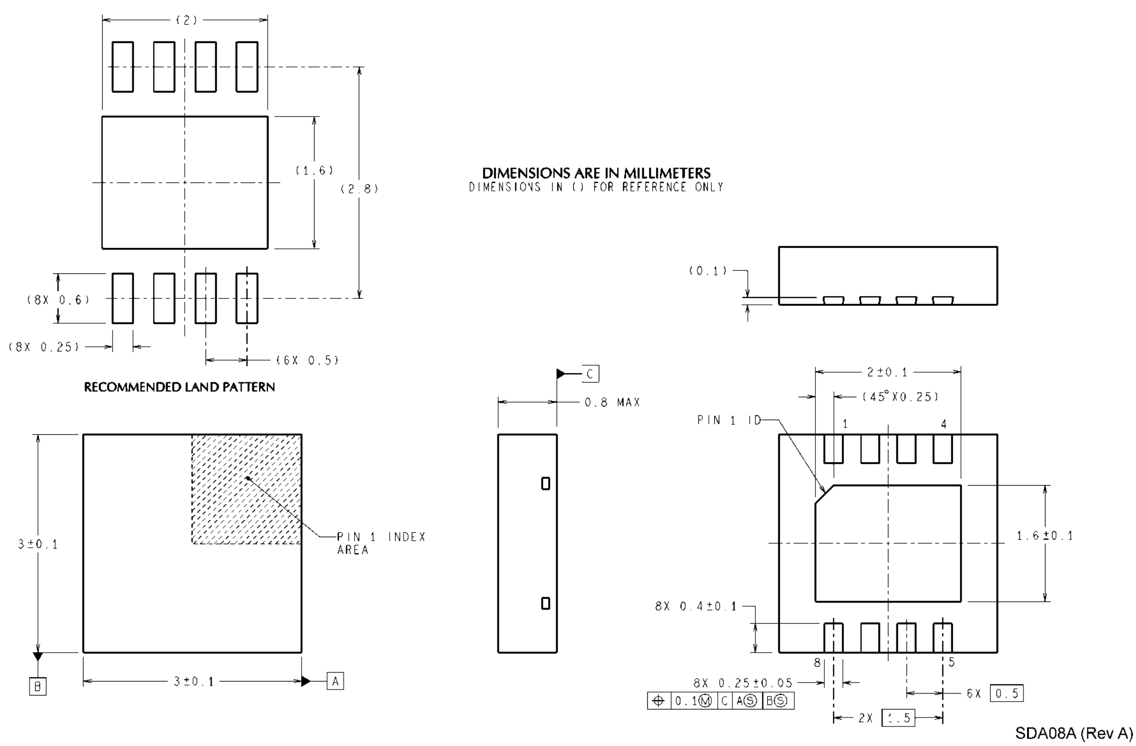
To ensure a clean supply voltage it is best to place decoupling capacitors close to the LMH2180, between V_{DD} and V_{SS}.

Another important issue is the value of the components, because this also determines the sensitivity to disturbances. Resistor values have to be low enough to avoid a significant noise contribution and large enough to avoid a significant increase in power consumption while loading inputs or outputs to heavily.

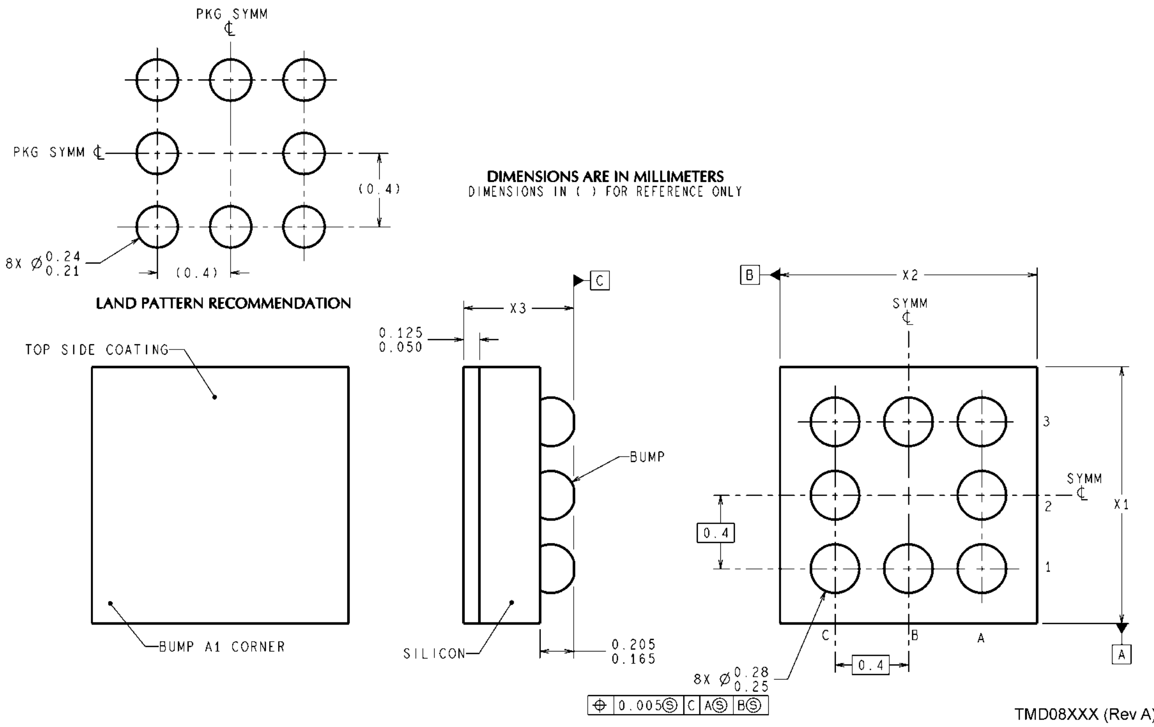
Physical Dimensions inches (millimeters) unless otherwise noted



8-Pin LLP
NS Package Number YDA08A



8-Pin LLP
NS Package Number SDA08A



8-Bump micro SMD
NS Package Number TMD08AAA
X1 = 1.215 ± 0.030 mm, X2 = 1.215 ± 0.030 mm, X3 = 0.600 ± 0.075 mm

Notes

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