

# 100390

## Low Power Single Supply Hex ECL-to-TTL Translator

### General Description

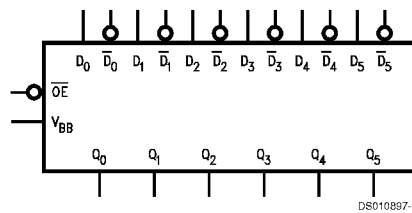
The 100390 is a hex translator for converting F100K logic levels to TTL logic levels. Unlike other level translators, the 100390 operates using only one +5V supply. Differential inputs allow each circuit to be used as an inverting, noninverting, or differential receiver. An internal reference generator provides  $V_{BB}$  for single-ended operation. The standard FAST® 3-STATE outputs are enabled by a common active low TTL compatible  $\overline{OE}$  input. Partitioned  $V_{CC}$ s on chip are brought out on separate power pins, allowing the noisy TTL

$V_{CC}$  power plane to be isolated from the relatively quiet ECL  $V_{CC}$ . The 100390 is ideal for applications limited to a single +5V supply, allowing for easy ECL to TTL interfacing.

### Features

- Operates from a single +5V supply
- 3-STATE outputs
- 2000V ESD protection
- $V_{BB}$  supplied for single-ended operation

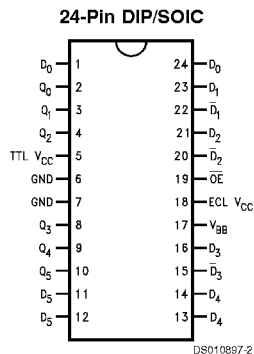
### Logic Symbol



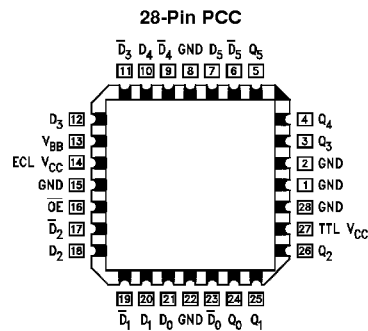
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Pin Names	Description
$D_0$ – $D_5$	Data Inputs (PECL)
$\overline{D}_0$ – $\overline{D}_5$	Inverting Data Inputs (PECL)
$Q_0$ – $Q_5$	Data Outputs (TTL)
$\overline{OE}$	Output Enable (TTL)
$V_{BB}$	Reference Voltage (PECL)

### Connection Diagrams



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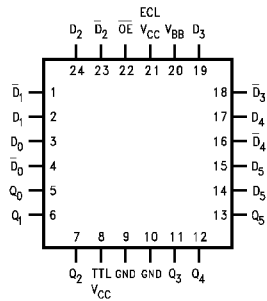


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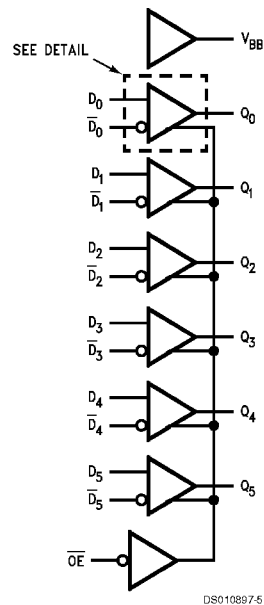
## Connection Diagrams (Continued)

### 24-Pin Quad Cerpak



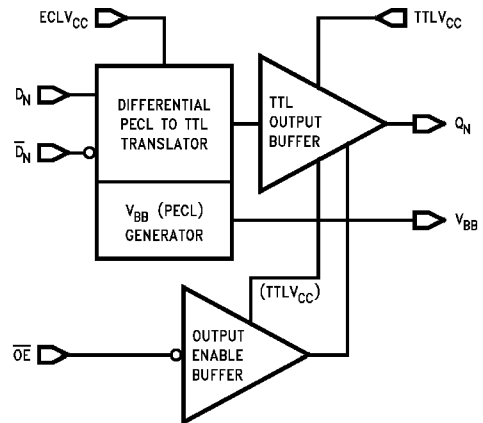
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### Logic Diagram



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### Detail



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## Truth Table

Data Inputs (PECL)		Control Input (TTL)	TTL Outputs	Comments
$D_n$	$\overline{D}_n$	$\overline{OE}$	$Q_n$	
X	X	H	Z	Outputs Disable
L	H	L	L	Differential Operation
H	L	L	H	Differential Operation
L	L	L	U	Invalid Input States
H	H	L	U	Invalid Input States
OPEN	OPEN	L	U	Invalid Input States
L	$V_{BB}$	L	L	Single Ended Operation
H	$V_{BB}$	L	H	Single Ended Operation
$V_{BB}$	L	L	H	Single Ended Operation
$V_{BB}$	H	L	L	Single Ended Operation
$V_{BB}$	OPEN	L	H	Single Ended Operation
OPEN	$V_{BB}$	L	L	Single Ended Operation

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 Z = HIGH Impedance  
 U = Undefined

## Absolute Maximum Ratings (Note 1)

Storage Temperature	-65°C to +150°C
Maximum Junction Temperature	
Ceramic	+175°C
Plastic	+150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
TTL Input Voltage (Note 2)	-0.5V to +7.0V
TTL Input Current (Note 2)	-30 mA to +5.0 mA
V <sub>BB</sub> Output Current	-5.0 mA to +1.0 mA
ECL Input Potential	GND to ECL V <sub>CC</sub> + 0.5V
V <sub>CC</sub> Differential ECL V <sub>CC</sub> to TTL V <sub>CC</sub>	-1.0V to +1.0V
Voltage Applied to Output	

in High State (with V <sub>CC</sub> = 0V)	
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in Low State (Max)	Twice the Rated I <sub>OL</sub> (mA)
ESD Last Passing Voltage (Min)	2000V

## Recommended Operating Conditions

Case Temperature	0°C to +85°C
Supply Voltage	+4.75V to +5.25V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## DC Electrical Characteristics

ECL V<sub>CC</sub> = +5.0V ±5%, TTL V<sub>CC</sub> = +5.0V ±5%, GND = 0V

Symbol	Parameter		Min	Max	Units	Conditions
V <sub>IH</sub>	Input HIGH Voltage	Data	ECL V <sub>CC</sub> - 1.165	ECL V <sub>CC</sub> - 0.870	V	Guaranteed HIGH Signal for ALL Inputs (with One Input Tied to V <sub>BB</sub> )
		$\overline{OE}$	2.0		V	Guaranteed HIGH Signal (TTL)
V <sub>IL</sub>	Input LOW Voltage	Data	ECL V <sub>CC</sub> - 1.830	ECL V <sub>CC</sub> - 1.475	V	Guaranteed LOW Signal for ALL Inputs (with One Input Tied to V <sub>BB</sub> )
		$\overline{OE}$		0.8	V	Guaranteed LOW Signal (TTL)
V <sub>BB</sub>	Output Reference Voltage		ECL V <sub>CC</sub> - 1.38	ECL V <sub>CC</sub> - 1.26	V	I <sub>BB</sub> = 0.0 mA or -1.0 mA
V <sub>OH</sub>	Output HIGH Voltage (TTL)		2.7		V	I <sub>OH</sub> = -3 mA
V <sub>OL</sub>	Output LOW Voltage (TTL)			0.5	V	I <sub>OL</sub> = 24 mA
I <sub>IH</sub>	Input HIGH Current	Data		50	μA	V <sub>IN</sub> = V <sub>IH</sub> (Max), D <sub>0</sub> -D <sub>5</sub> = V <sub>BB</sub> , $\overline{D_0}-\overline{D_5}$ = V <sub>IL</sub> (Min)
		$\overline{OE}$		20	μA	V <sub>IN</sub> = 2.7V (TTL)
I <sub>IL</sub>	Input LOW Current	$\overline{OE}$		-200	μA	V <sub>IN</sub> = 0.5V (TTL)
I <sub>BVI</sub>	Input Breakdown Current	$\overline{OE}$		10	μA	V <sub>IN</sub> = 7.0V (TTL)
I <sub>CBO</sub>	Input Leakage Current		-10		μA	V <sub>IN</sub> = GND, D <sub>0</sub> -D <sub>5</sub> = V <sub>BB</sub> , $\overline{D_0}-\overline{D_5}$ = V <sub>IL</sub> (Min)
I <sub>OZH</sub>	3-STATE Current Output HIGH			50	μA	V <sub>OUT</sub> = +2.7V
I <sub>OZL</sub>	3-STATE Current Output LOW			-50	μA	V <sub>OUT</sub> = +0.5V
I <sub>CC</sub>	ECL Supply Current		13	30	mA	
I <sub>CCZ</sub>	TTL Supply Current		10	20	mA	3-STATE
I <sub>CCL</sub>	TTL Supply Current		8	17	mA	Low State
I <sub>CCH</sub>	TTL Supply Current HIGH		0.4	2.0	mA	HIGH State
I <sub>OS</sub>	Output Short-Circuit Current		-150	-60	mA	V <sub>OUT</sub> = 0.0V, V <sub>CC</sub> = +5.25
V <sub>Diff</sub>	Differential Input Voltage		150		mV	Required for Full Output Swing
V <sub>CM</sub>	Common Mode Voltage		ECL V <sub>CC</sub> - 2.0	ECL V <sub>CC</sub> - 0.5	V	
V <sub>CD</sub>	Clamp Diode Voltage			-1.2	V	I <sub>IN</sub> = -18 mA

## DIP AC Electrical Characteristics

$V_{CC} = 5.0V \pm 5\%$ ;  $T_C = 0^\circ C$  to  $+85^\circ C$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
$F_{MAX}$	Maximum Clock Frequency	100		100		100		MHz	
$t_{PLH}$	Propagation Delay	3.5	7.2	3.5	6.8	3.5	6.7	ns	Figure 1
$t_{PHL}$	Data to Output								
$t_{PZH}$	Output Enable Time	2.7	4.8	2.7	4.8	3.0	5.1	ns	Figure 2
$t_{PZL}$	Output Disable Time	2.4	4.0	2.4	4.0	2.6	4.2	ns	Figure 2
$t_{PHZ}$	Output Disable Time	2.9	5.8	2.9	5.4	2.7	5.1	ns	Figure 2
$t_{PLZ}$	Output Disable Time	2.3	3.9	2.2	3.9	2.2	3.9	ns	

## SOIC, Cerpak and PCC Package AC Electrical Characteristics

$V_{CC} = 5.0V \pm 5\%$ ;  $T_C = 0^\circ C$  to  $+85^\circ C$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Fig. No.
		Min	Max	Min	Max	Min	Max		
$F_{MAX}$	Maximum Clock Frequency	100		100		100		MHz	
$t_{PLH}$	Propagation Delay	3.5	7.0	3.5	6.6	3.5	6.5	ns	Figure 1
$t_{PHL}$	Data to Output								
$t_{PZH}$	Output Enable Time	2.7	4.6	2.7	4.6	3.0	4.9	ns	Figure 2
$t_{PZL}$	Output Disable Time	2.4	3.8	2.4	3.8	2.6	4.0	ns	Figure 2
$t_{PHZ}$	Output Disable Time	2.9	5.6	2.9	5.2	2.7	4.9	ns	Figure 2
$t_{PLZ}$	Output Disable Time	2.3	3.7	2.2	3.7	2.2	3.7	ns	

## Switching Waveforms

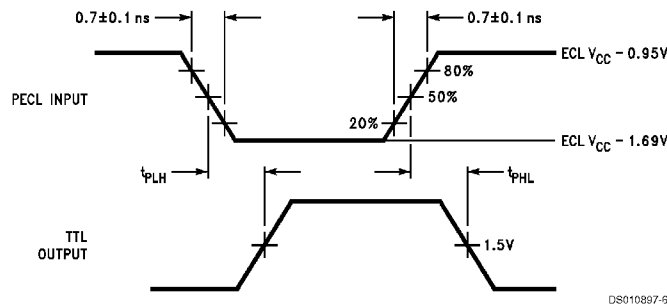


FIGURE 1. Data to Output Propagation Delay

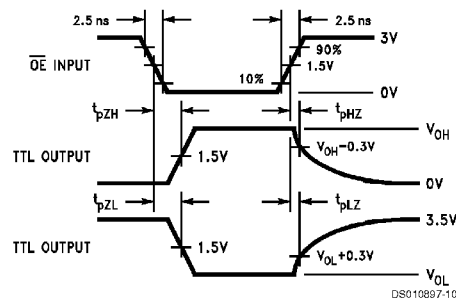
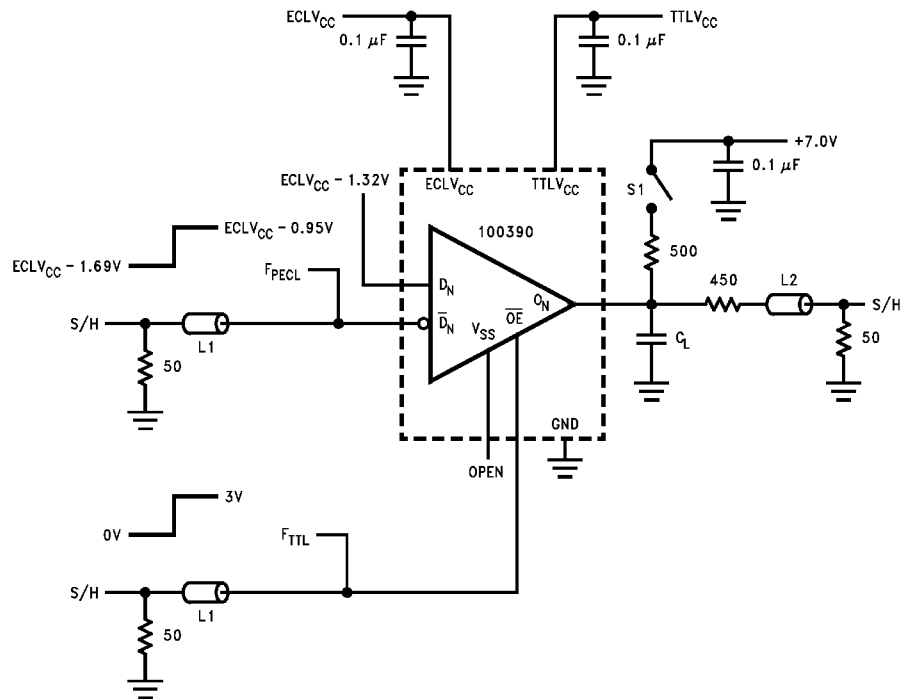


FIGURE 2. Enable/Disable Propagation Delay

## Test Circuit



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### Notes:

- GND = 0V, ECL V<sub>CC</sub> = +5V, TTL V<sub>CC</sub> = +5V
- L1 and L2 = equal length 50Ω impedance lines
- 50Ω terminators are internal to S/H measurement unit
- Decoupling 0.1 μF from GND to ECL V<sub>CC</sub> and TTL V<sub>CC</sub>
- All unused outputs are loaded with 500Ω to GND
- C<sub>L</sub> = Fixture and stray capacitance = 50 pF
- Switch S1 is open for t<sub>PLH</sub>, t<sub>PHL</sub>, t<sub>PHZ</sub> and t<sub>PZH</sub> tests
- Switch S1 is closed only for t<sub>PLZ</sub> and t<sub>PZL</sub> tests

FIGURE 3. AC Test Circuit

## Application Notes

1. Device performance will be enhanced by the use of dual V<sub>CC</sub> power planes as illustrated in the Application Figures 4, 5. This will minimize the coupling of TTL switching noise into the primary reference to the ECL circuitry and take full advantage of the 100390's on chip V<sub>CC</sub> partitioning.
2. The device's partitioned V<sub>CC</sub> may be operated from two 5V, 5% tolerance, supplies provided that they are ramped up/down together so that the max differential is 1V. This is to prevent overstress to internal ESD diodes. If the ECL driver to the F390 is powered from a separate supply, it must obey this sequence rule also.
3. Glitch-free power up, independent of Data input levels, is achieved if TTL logic HIGH is held on the Output Enable pin during ramping up/down of the V<sub>CC</sub> supply.
4. Undefined output states can occur for some invalid combinations. See Truth Table. This should be avoided to prevent possible oscillation or increased power consumption due to TTL outputs biased into a quasi state with both pullup and pulldown stages partially on. 3-STATEing the outputs will counteract the effects of invalid input states.
5. Pins 8, 15, and 22 on the 28-pin PCC package are tied to the chip's substrate and are named GNDs. These pins are electrically common to the ground pins 1, 2, and 28. For best thermal performance, tie the GND pins to the circuit ground plane. They may be tied to an electrically isolated thermal dissipation plane or may float.
6. Figure 4 illustrates typical differential input operation.
7. Figure 5 illustrates typical single-ended input operation.

**Application Notes** (Continued)

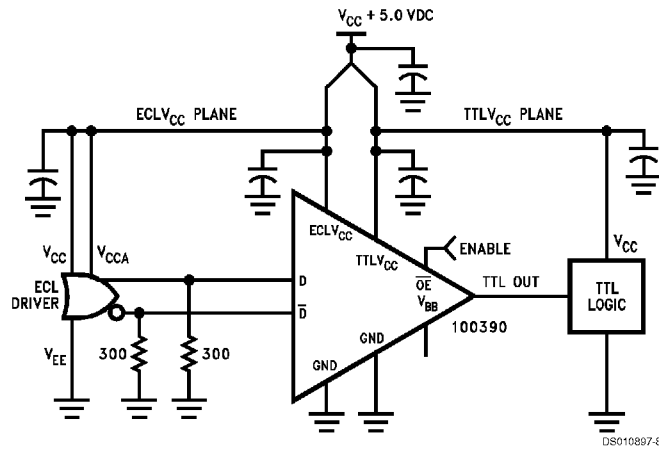


FIGURE 4.

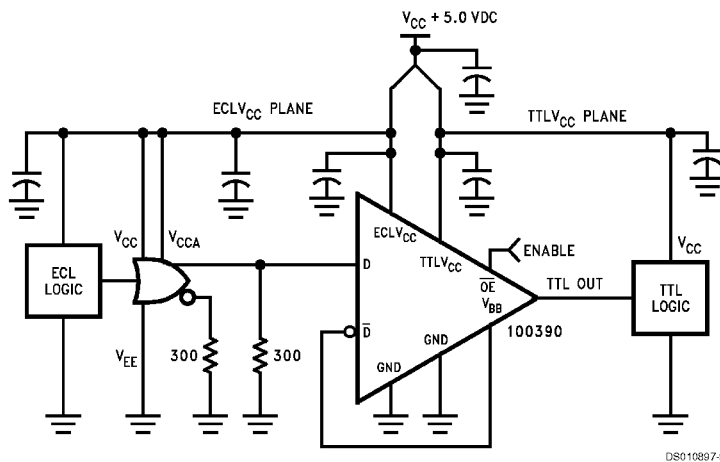
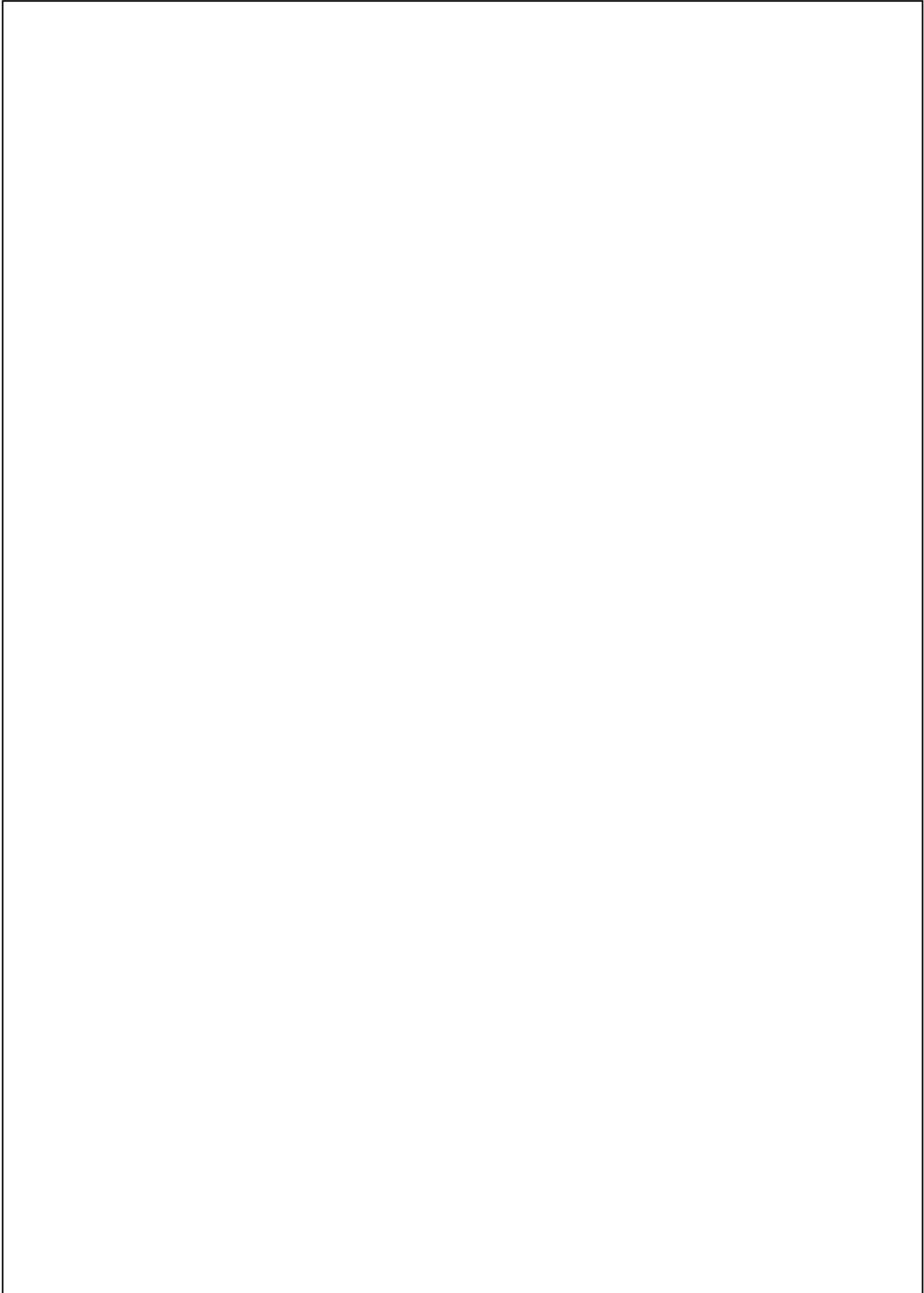


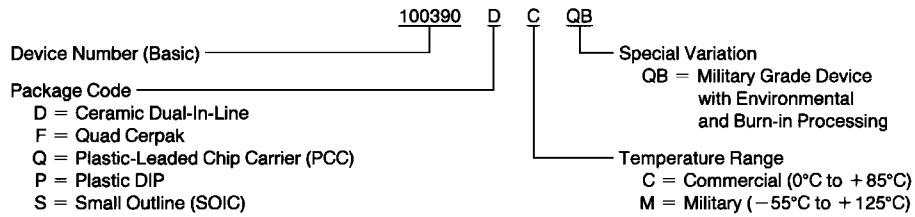
FIGURE 5.





## Ordering Information

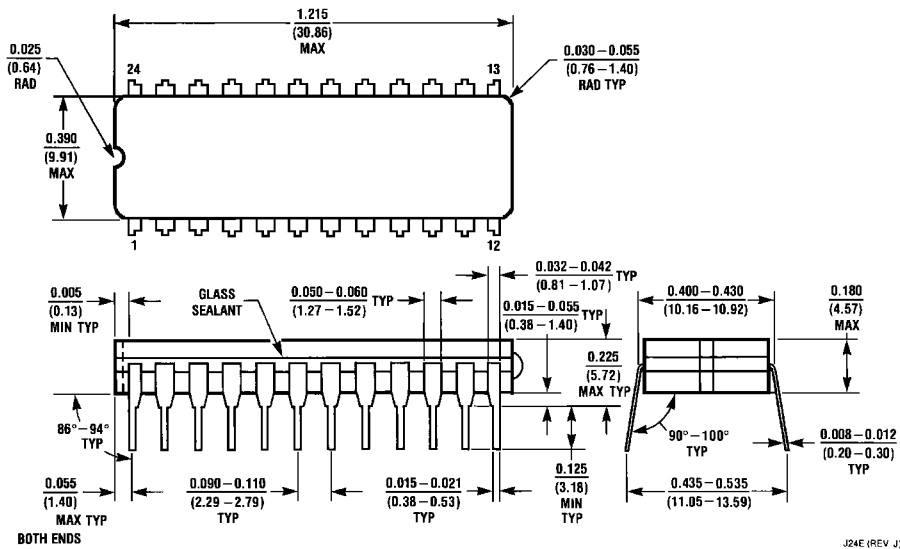
The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:



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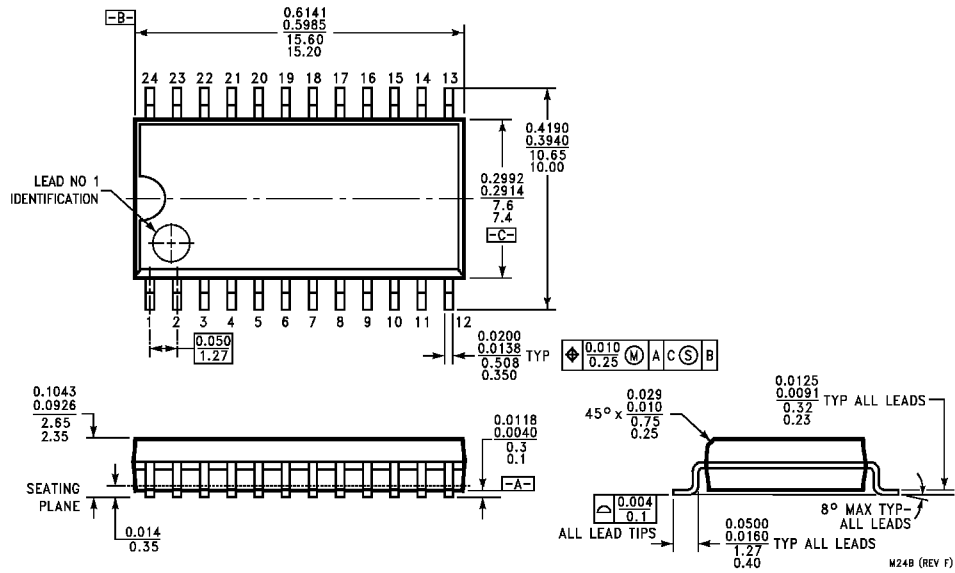
## Physical Dimensions

inches (millimeters) unless otherwise noted

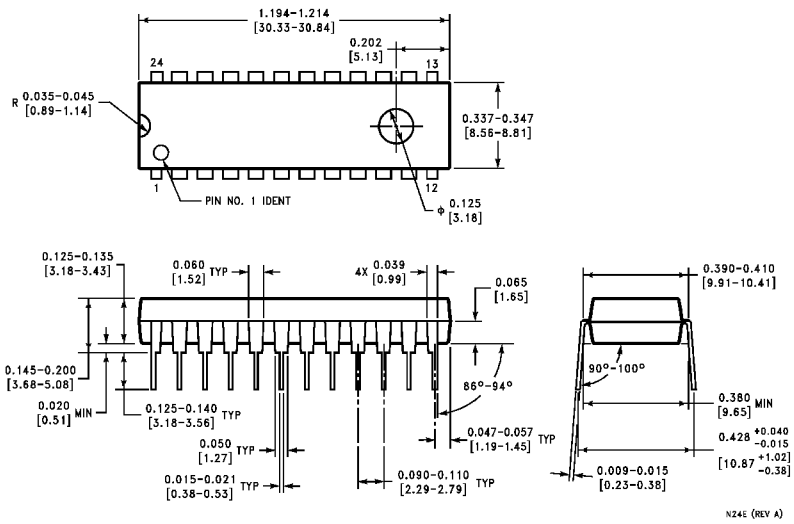


24-Lead Ceramic Dual-In-Line Package  
(0.400" Wide) (D)  
Package Number J24E

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)

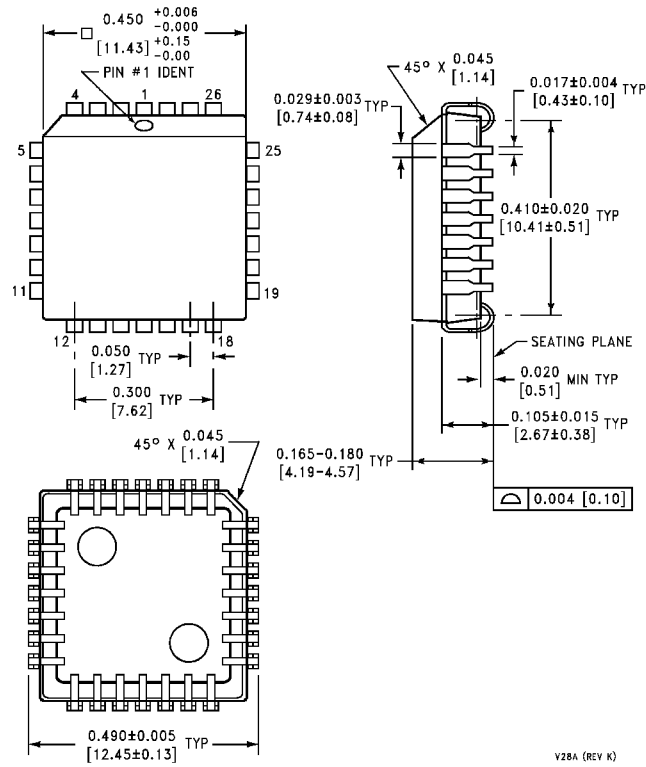


**24-Lead Molded Package  
(0.300" Wide) (S)  
Package Number M24B**



**24-Lead Plastic Dual-In-Line Package (P)  
Package Number N24E**

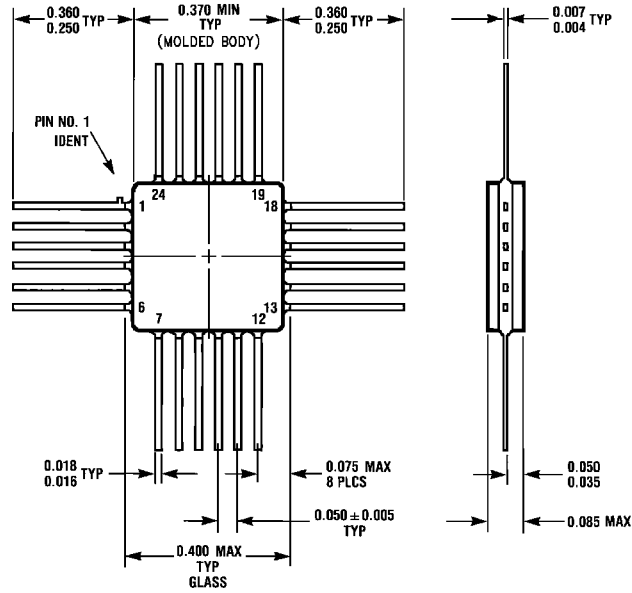
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**28-Lead Plastic Chip Carrier (Q)**  
**Package Number V28A**

V28A (REV K)

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



W24B (REV D)

**24-Lead Quad Cerpak (F)  
Package Number W24B**

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