

1、General Description

GN1629C is a 3-line serial interface common cathode 15 seg 8 grid LED controller/driver. It has keyboard scan ports, MCU digital ports, data latches, LED drivers and other circuits. Used in all kind of LED panels, such as microwave ovens, induction cookers, water heaters and other home appliances.

Features:

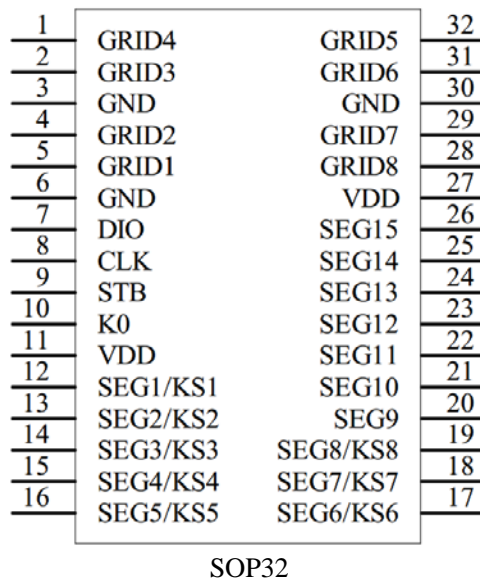
- Display Modes (15 segment * 8 grid)
- Built-in display RAM
- Key Scanning (8 × 1bit)
- Software adjustable display brightness
- 3-line serial interface (CLK, STB, DIO)
- Built-in RC oscillator

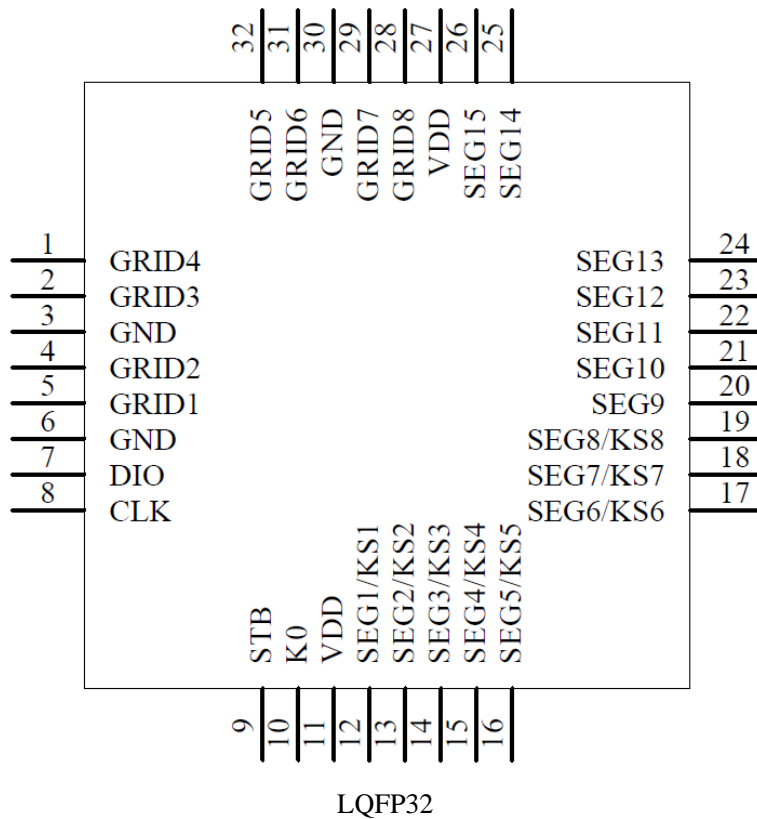
Package form

GN1629C SOP-32 20PCS/tube 1600PCS/box 16000PCS/box

2、Block Diagram And Pin Description

2.1、Pin Arrangement Diagram





2.2、Pin Description

Pin No.	Pin Name	I/O	Description
1	GRID4	O	Grid Output Pins (N-Channel, open drain)
2	GRID3	O	Grid Output Pins (N-Channel, open drain)
3	GND	-	Ground Pin
4	GRID2	O	Grid Output Pins (N-Channel, open drain)
5	GRID1	O	Grid Output Pins (N-Channel, open drain)
6	GND	-	Ground Pin
7	DIO	IO	Data Input Output Pin (N-Channel, open drain) This pin inputs serial data at the rising edge of the shift clock (starting from the lower bit); This pin outputs serial data at the falling edge of the shift clock(starting from the lower bit).
8	CLK	I	Clock input Pin . This pin reads serial data at the rising edge and outputs data at the falling edge.
9	STB	I	Serial Interface Strobe Pin The data input after the STB has fallen is processed as a command. When this pin is "HIGH", CLK is ignored.

10	K0	I	Key Data Input Pins The data sent to these pins are latched at the end of the display cycle.(Internal Pull-Low Resistor)
11	VDD	-	Power Supply
12	SEG1/KS1	O	Segment Output Pins(P-Channel, open drain) Also acts as the Key Source.
13	SEG2/KS2	O	Segment Output Pins(P-Channel, open drain) Also acts as the Key Source.
14	SEG3/KS3	O	Segment Output Pins(P-Channel, open drain) Also acts as the Key Source.
15	SEG4/KS4	O	Segment Output Pins(P-Channel, open drain) Also acts as the Key Source.
16	SEG5/KS5	O	Segment Output Pins(P-Channel, open drain) Also acts as the Key Source.
17	SEG6/KS6	O	Segment Output Pins(P-Channel, open drain) Also acts as the Key Source.
18	SEG7/KS7	O	Segment Output Pins(P-Channel, open drain) Also acts as the Key Source.
19	SEG8/KS8	O	Segment Output Pins(P-Channel, open drain) Also acts as the Key Source.
20	SEG9	O	Segment Output Pins(P-Channel, open drain)
21	SEG10	O	Segment Output Pins(P-Channel, open drain)
22	SEG11	O	Segment Output Pins(P-Channel, open drain)
23	SEG12	O	Segment Output Pins(P-Channel, open drain)
24	SEG13	O	Segment Output Pins(P-Channel, open drain)
25	SEG14	O	Segment Output Pins(P-Channel, open drain)
26	SEG15	O	Segment Output Pins(P-Channel, open drain)
27	VDD	-	Power Supply
28	GRID8	O	Grid Output Pins (N-Channel, open drain)
29	GRID7	O	Grid Output Pins (N-Channel, open drain)
30	GND	-	Ground Pin
31	GRID6	O	Grid Output Pins (N-Channel, open drain)
32	GRID5	O	Grid Output Pins (N-Channel, open drain)

3、Electrical Parameter

3.1、Absolute Maximum Ratings ($T_{amb}=25^{\circ}C$, All voltage referenced to GND, unless otherwise specified.)

Characteristic	Symbol	Conditions	Value	Unit	
Supply Voltage	VDD	-	-0.5~7.0	V	
Input Voltage	V_{IN}	-	-0.5~VDD+0.5	V	
Drive Output Current	I_{O1}	-	-50	mA	
	I_{O2}	-	+150	mA	
Ambient Temperature	T_{amb}	-	-40~+85	$^{\circ}C$	
Storage Temperature	T_{stg}	-	-65~+150	$^{\circ}C$	
Soldering Temperature	T_L	10s	SOP32	250	$^{\circ}C$
		LQFP32	260	$^{\circ}C$	

3.2、Recommended Operating Range

Parameter	Symbol	Min.	Typ.	Max.	Unit
Logic Supply Voltage	VDD	3	5	5.5	V
High-level Input Voltage	V_{IH}	0.7VDD	-	VDD	V
Low-level Input Voltage	V_{IL}	0	-	0.2VDD	V

3.3、Electrical Characteristics

3.3.1、DC Characteristics ($V_{DD}=5V$, $GND=0V$, unless otherwise specified.)

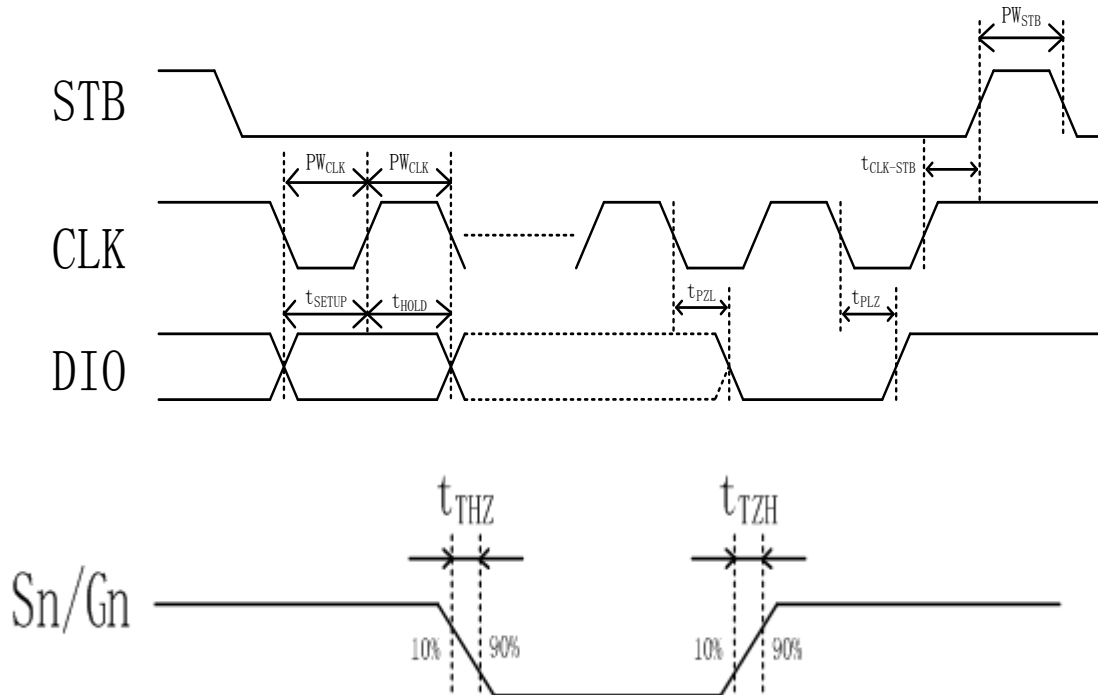
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
High-level Output Current	I_{OH1}	SEG1~SEG15, $V_O = V_{DD} - 2V$	-20	-25	-40	mA
	I_{OH2}	SEG1~SEG15, $V_O = V_{DD} - 3V$	-20	-30	-50	mA
Low-level Output Current	I_{OL1}	GRID1~GRID8, $V_O = 0.3V$	80	100	-	mA
	I_{DO}	$V_O = 0.4V$, DIO	4	8	-	mA
Segment High-level Output Current Tolerance	I_{TOLSG}	$V_O = V_{DD} - 3V$, SEG1~SEG15	-	-	5	%
High-level Input Voltage	V_{IH}	CLK, DIO, STB	0.7VDD	-	-	V
Low-level Input Voltage	V_{IL}	CLK, DIO, STB	-	-	0.2VDD	V
Hysteresis Voltage	V_H	CLK, DIO, STB	-	0.35	-	V
Input Leakage Current	I_I	$V_{IN} = V_{DD}/GND$, CLK, DIO, STB	-	-	± 1	μA
Supply Current	I_{DD}	No load, $V_{IN} = V_{DD}$	120	150	180	μA
Input resistance	R_L	K0	-	3	-	K Ω

3.3.2、AC Characteristics (VDD=4.5~5.5V, GND=0V, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	
Oscillation Frequency	f_{OSC}	-	-	400	-	KHz	
Propagation Delay	t_{PLZ}	CLK→DIO $C_L=15pF, R_L=10K\Omega$	-	-	300	ns	
	t_{PZL}		-	-	100	ns	
Rise Time	t_{TZH1}	$C_L=300pF$	SEG1~SEG15		2	us	
	t_{TZH2}		GRID1~GRID8		0.5	us	
Fall Time	t_{THZ}	$C_L=300pF, SEGn, GRIDn$		-	-	120	us
Maximum Clock Frequency	f_{max}	Duty=50%	1	-	-	MHz	

3.3.3、Timing Characteristics (VDD=4.5~5.5V, GND=0V, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Clock Pulse Width	PW_{CLK}	-	400	-	-	ns
STB Pulse Width	PW_{STB}	-	1	-	-	us
Set-up Time For Data	t_{SETUP}	-	100	-	-	ns
Hold Time For Data	t_{HOLD}	-	100	-	-	ns
Propagation Delay CLK to STB	$t_{CLK-STB}$	CLK↑→STB↑	1	-	-	us
Wait Time	t_{WAIT}	CLK↑→CLK↓	1	-	-	us



4、Function Description

4.1、Display Mode And RAM Address

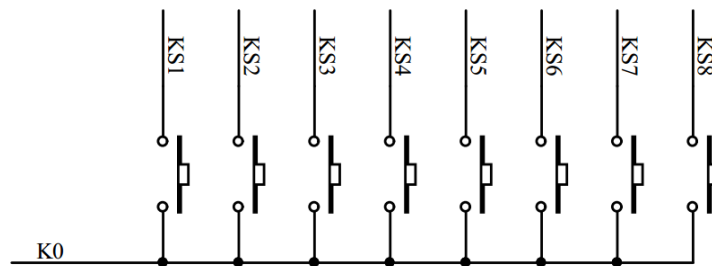
Data transmitted from an external device to GN1629C via the serial interface are stored in the Display register. The allocation of the register addresses is as follows:

SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	X	
xxHL(low 4 bits)				xxHU(high 4 bits)				xxHL(low 4 bits)				xxHU(high 4 bits)				
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	
00HL				00HU				01HL				01HU				GRID1
02HL				02HU				03HL				03HU				GRID2
04HL				04HU				05HL				05HU				GRID3
06HL				06HU				07HL				07HU				GRID4
08HL				08HU				09HL				09HU				GRID5
0AHL				0AHU				0BHL				0BHU				GRID6
0CHL				0CHU				0DHL				0DHU				GRID7
0EHL				0EHU				0FHL				0FHU				GRID8

Note: When power up, first transfer data to RAM, and then setup display on.

4.2、Key Scanning And Key Scanning Data Registers

Key scanning matrix is 8×1 bit, as follows:



The Key scanning data storage address is as follows. After issuing the key reading command, read the key data BYTE1~BYTE4 and output the data from low-level. When the key corresponding to the pins K and KS is pressed, the BIT bit in the corresponding byte is 1.

B0	B1	B2	B3	B4	B5	B6	B7	
X	X	X	K0	X	X	X	K0	
KS1				KS2				BYTE1
KS3				KS4				BYTE2
KS5				KS6				BYTE3
KS7				KS8				BYTE4

4.3、Commands Description

Commands are used to set the display mode and the state of the LED driver.

The first byte entered by DIO after the falling edge of STB is used as an instruction. After decoding, the highest B7 and B6 bits are taken to distinguish different instructions.

B7	B6	Commands
0	1	Data Command Settings
1	0	Display Control Command Settings
1	1	Address Command Settings

If the STB is set to a high level at the time of instruction or data transmission, the serial communication is initialized and the instruction or data being transmitted is invalid (the previously transmitted instruction or data remains valid).

4.3.1、Data Command Settings

This instruction is used to set data write and read, B1 and B0 bits are not allowed to set 01 or 11.

MSB				LSB				Function	Description
B7	B6	B5	B4	B3	B2	B1	B0		
0	1	Irrelevant terms, set 0		-	-	0	0	Data Read-Write Mode Settings	Write Data to Display Register
0	1			-	-	1	0		Read Key Scan Data
0	1			-	0	-	-	Address Addition Mode Settings	Automatic Address Increase
0	1			-	1	-	-		Fixed Address
0	1			0	-	-	-	Test Mode Settings	Common Mode
0	1			1	-	-	-		Test Mode (Internal Use)

4.3.2、Address Command Settings

This instruction is used to set the address of the display register. If the address is set to 10H or higher, the data is ignored until the effective address is set. When power on, the address is set to 00H by default.

MSB				LSB				Display Address
B7	B6	B5	B4	B3	B2	B1	B0	
1	1	Irrelevant terms, set 0		0	0	0	0	00H
1	1			0	0	0	1	01H
1	1			0	0	1	0	02H
1	1			0	0	1	1	03H
1	1			0	1	0	0	04H
1	1			0	1	0	1	05H
1	1			0	1	1	0	06H
1	1			0	1	1	1	07H

1	1		1	0	0	0	08H
1	1		1	0	0	1	09H
1	1		1	0	1	0	0AH
1	1		1	0	1	1	0BH
1	1		1	1	0	0	0CH
1	1		1	1	0	1	0DH
1	1		1	1	1	0	0EH
1	1		1	1	1	1	0FH

4.3.3、Display Control MSB

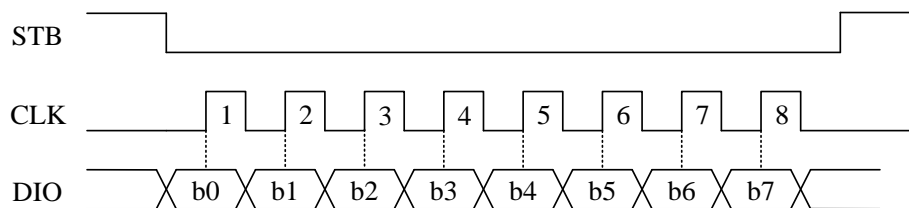
LSB

B7	B6	B5	B4	B3	B2	B1	B0	Function	Description
1	0	Irrelevant terms, set 0		-	0	0	0	Extinction Number Settings	Set the pulse width to 1/16
1	0			-	0	0	1		Set the pulse width to 2/16
1	0			-	0	1	0		Set the pulse width to 4/16
1	0			-	0	1	1		Set the pulse width to 10/16
1	0			-	1	0	0		Set the pulse width to 11/16
1	0			-	1	0	1		Set the pulse width to 12/16
1	0			-	1	1	0		Set the pulse width to 13/16
1	0			-	1	1	1		Set the pulse width to 14/16
1	0				0	-	-	-	Display Switch Settings
1	0			1	-	-	-	Display ON	

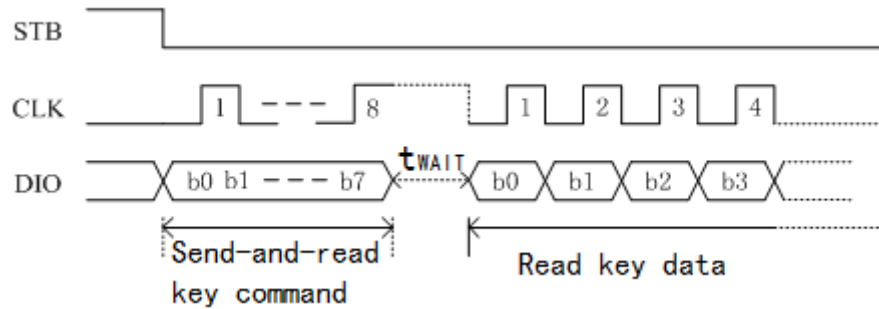
4.4、Serial Data Transfer Format

Reading and receiving a BIT are performed at the rising edge of the clock.

4.4.1、Data Receiving (Writing)



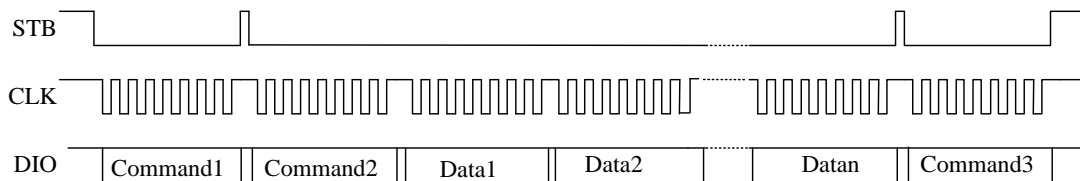
4.4.2、Data Reading (Reading)



Note: When reading data, there is a waiting time t_{WAIT} (minimum 1us) between setting instructions from the 8th rising edge of serial clock CLK to the falling edge of CLK.

4.5、Transmission Of Serial Data In Application

4.5.1、Address Addition Mode



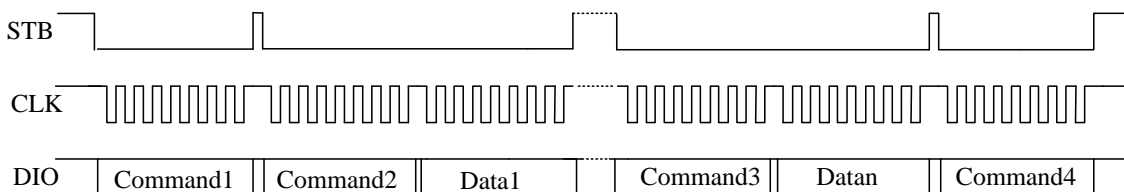
Command1: Setting data command

Command2: Setting display address

Data1 ~ n: Transfer display data

Command3: Display control command

4.5.2、Fixed Address Mode



Command1: Setting data command

Command2: Setting display Address 1

Data1: Transfer display data to Command2 Address

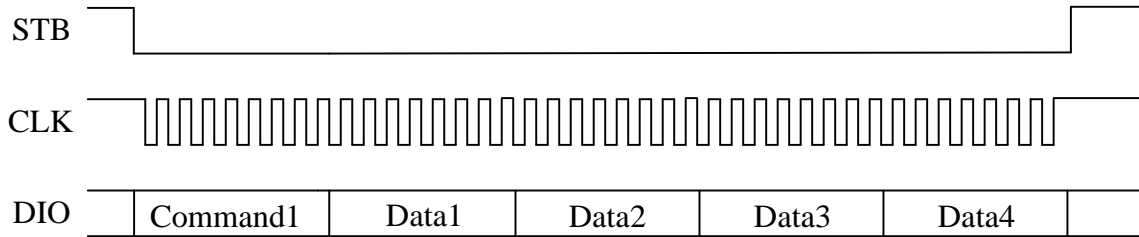
⋮

Command3: Setting display address N

Datan: Transfer display data to Command3 address

Command4: Display control command

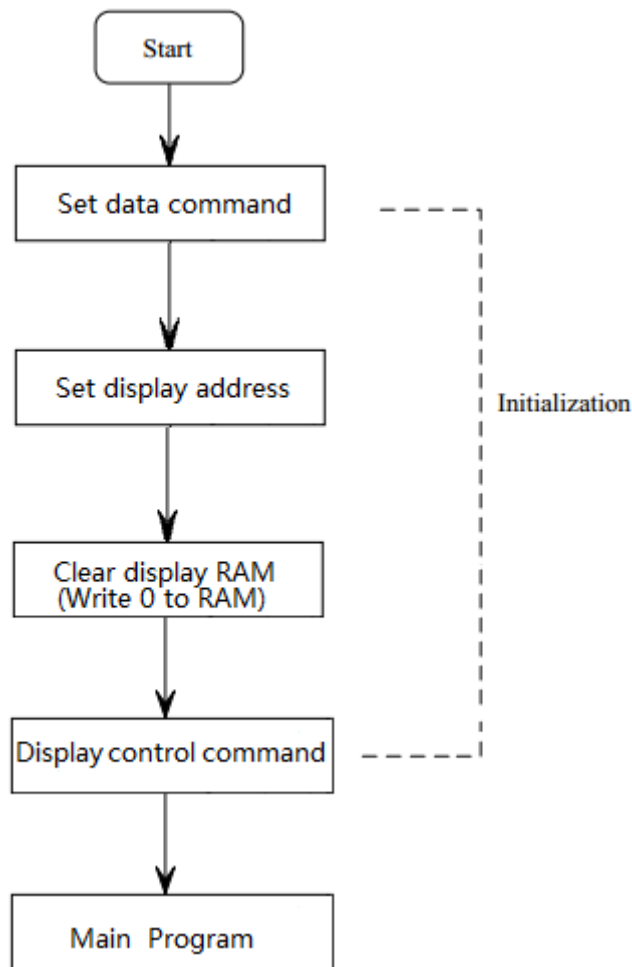
4.5.3、Reading Key Timing



Command1: Setting reading key data command

Data1 ~ 4: Read Key Data

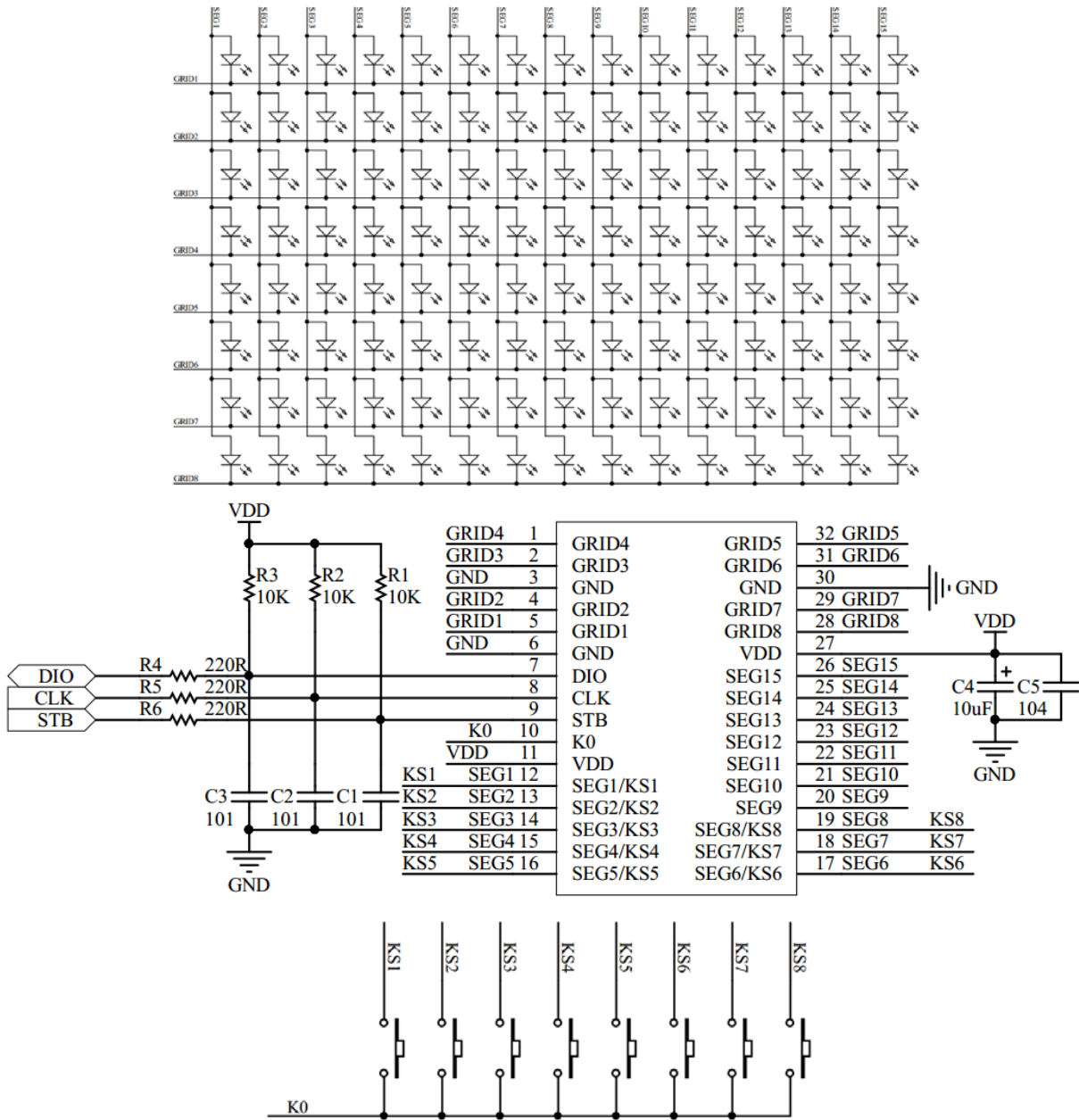
4.6、Initialization Flow Chart



Note:1. The data command is used to select whether to write display data for the RAM area(divided into two types:fixed address and address self-addition)or read key values.

2.When the IC is powered on, the content of RAM is not fixed. In order to prevent the display from appearing randomly when the display is turned on first. It is recommended to clear the RAM and then turn on the display.

5、Typical Application Circuit And Application Note

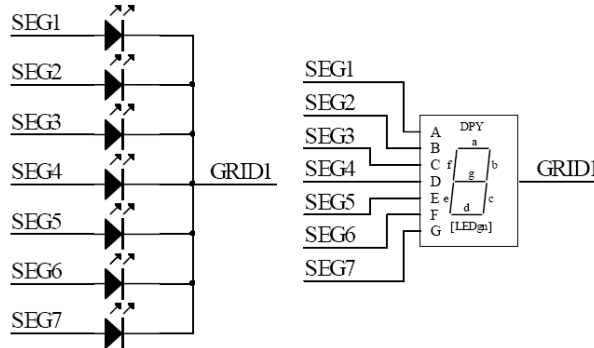


Note:1. The circuit between filter capacitor and VDD, GND is as short as possible to enhance the filter effect.

2. In order to improve the anti-interference ability of the circuit, the communication port is recommended to be connected according to the above figure. The specific parameter values can be adjusted according to actual needs.

5.1、Drive Common Cathode Digital Tube

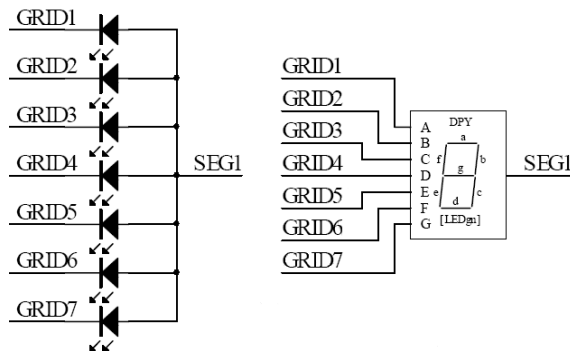
If the digital tube displays “0”, then you need to make SEG1, SEG2, SEG3, SEG4, SEG5, SEG6 high and SEG7 low when GRID1 is low. Just write the data 3FH in the 00H address to make the digital tube display “0”. The connection diagram of the common cathode digital tube shows below:



SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	Address
B7	B6	B5	B4	B3	B2	B1	B0	
0	0	1	1	1	1	1	1	00H

5.2、Drive Common Anode Digital Tube

If the digital tube shows “0”, then you need to make SEG1 high when GRID1, GRID2, GRID3, GRID4, GRID5 and GRID6 are low, and SEG1 low when GRID7 is low. Write data 01H to address units 00H, 02H, 04H, 06H, 08H, 0AH, respectively, the rest of the address units all write data 00H. The connection diagram of the common anode digital tube shows below:

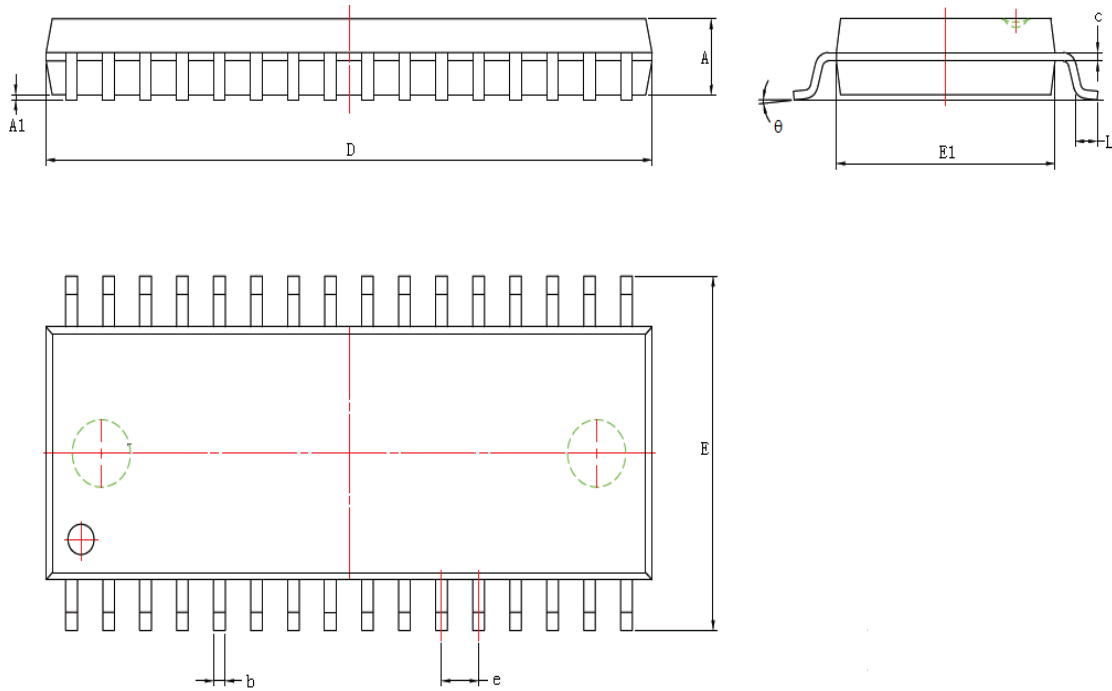


SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	Address
B7	B6	B5	B4	B3	B2	B1	B0	
0	0	0	0	0	0	0	1	00H
0	0	0	0	0	0	0	1	02H
0	0	0	0	0	0	0	1	04H
0	0	0	0	0	0	0	1	06H
0	0	0	0	0	0	0	1	08H
0	0	0	0	0	0	0	1	0AH
0	0	0	0	0	0	0	0	0CH

Note: SEGn is the P channel open drain output, GRIDn is the N channel open drain output. When using, SEGn can only connect the anode of LED, GRIDn can only connect the cathode of LED, no reverse connection.

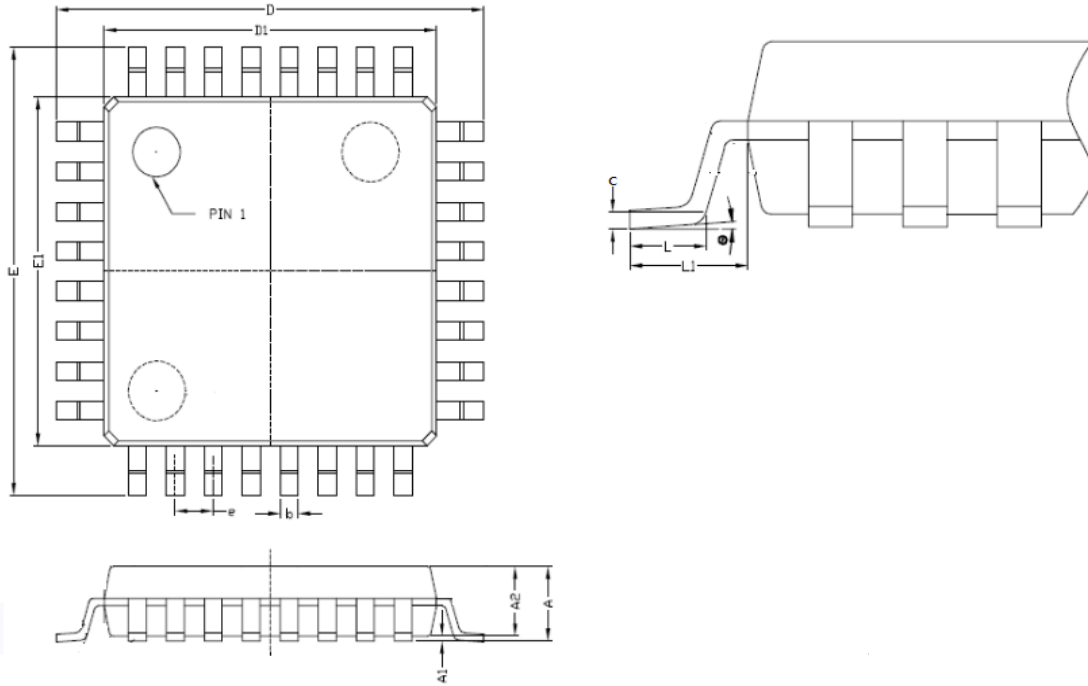
6、Package Dimensions and Outline Drawings

6.1、SOP-32 Outline Drawings and Package Dimensions



2023/12/A	Dimensions In Millimeters	
Symbol	Min.	Max.
A	2.24	2.59
A1	0.05	0.25
E	10.20	10.60
E1	7.40	7.62
D	20.68	21.08
L	0.55	0.95
e	1.27	
b	0.30	0.50
c	0.25	
θ	0°	8°

6.2、LQFP-32 Outline Drawings and Package Dimensions



2023/12/A	Dimensions In Millimeters	
Symbol	Min	Max
A	—	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.32	0.43
c	0.13	0.18
D	8.80	9.20
D1	6.90	7.10
E	8.80	9.20
E1	6.90	7.10
e	0.80	
L	0.45	0.75
L1	1.00	
θ	0°	7°

7、StatementsAnd Notes

7.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
Explanation	○: Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006standard. ×: Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

7.2、Notes

We Recommend you to read this chapter carefully before using this product.

The information in this chapter is provided for reference only and i-Core disclaims any express or implied warranties, including but not limited to applicability, special application or non-infringement of third party rights.

This product is not suitable for critical equipment such as life-saving, life-sustaining or safety equipment. It is also not suitable for applications that may result in personal injury, death, or serious property or environmental damage due to product malfunction or failure. I-Core will not be liable for any damages incurred by the customers at their own risk for such applications.

The customer is responsible for conducting all necessary tests i-Core 's application to avoid failure in the application or the application of the customer 's third party users. I-Core does not accept any liability.

The Company reserves the right to change or improve the information published in this chapter at any time. The information in this chapter are subject to change without notice. We recommend the customer to consult our sales staff before purchasing.

Please obtain related materials form i-Core 's regular channels and we are not responsible for its content if it is provided by sources other than our company.

In case of any conflict between the Chinese and English version, the version is subject to the Chinese one.