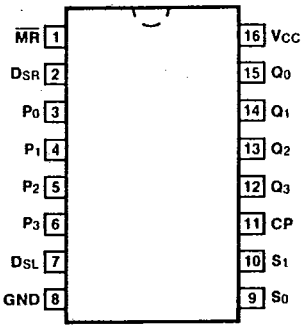
54/74194
54S/74S194
54LS/74LS194A

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

DESCRIPTION — The '194 is a high speed 4-bit bidirectional universal shift register. As a high speed multifunctional sequential building block, it is useful in a wide variety of applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers. The '194 is similar in operation to the '195 universal shift register, with added features of shift left without external connections and hold (do nothing) modes of operation.

- **GUARANTEED SHIFT FREQUENCY OF 30 MHz ('LS194A) OR 70 MHz ('S194)**
- **ASYNCHRONOUS MASTER RESET**
- **HOLD (DO NOTHING) MODE**
- **FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS**

CONNECTION DIAGRAM
PINOUT A



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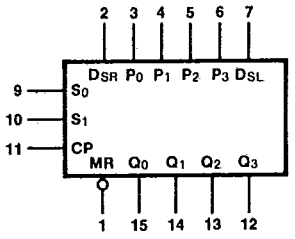
LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74194PC 74S194PC, 74LS194APC		9B
Ceramic DIP (D)	A	74194DC, 74S194DC, 74LS194ADC	54194DM 54S194DM, 54LS194ADM	6B
Flatpak (F)	A	74194FC, 74S194FC, 74LS194AFC	54194FM 54S194FM, 54LS194AFM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
S_0, S_1	Mode Control Inputs	1.0/1.0	1.25/1.25	0.5/0.25
$P_0 - P_3$	Parallel Data Inputs	1.0/1.0	1.0/1.0	0.5/0.25
D_{SR}	Serial Data Input (Shift Right)	1.0/1.0	1.0/1.0	0.5/0.25
D_{SL}	Serial Data Input (Shift Left)	1.0/1.0	1.0/1.0	0.5/0.25
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	1.25/1.25	0.5/0.25
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	1.25/1.25	0.5/0.25
$Q_0 - Q_3$	Parallel Outputs	20/10	25/12.5	10/5.0 (2.5)

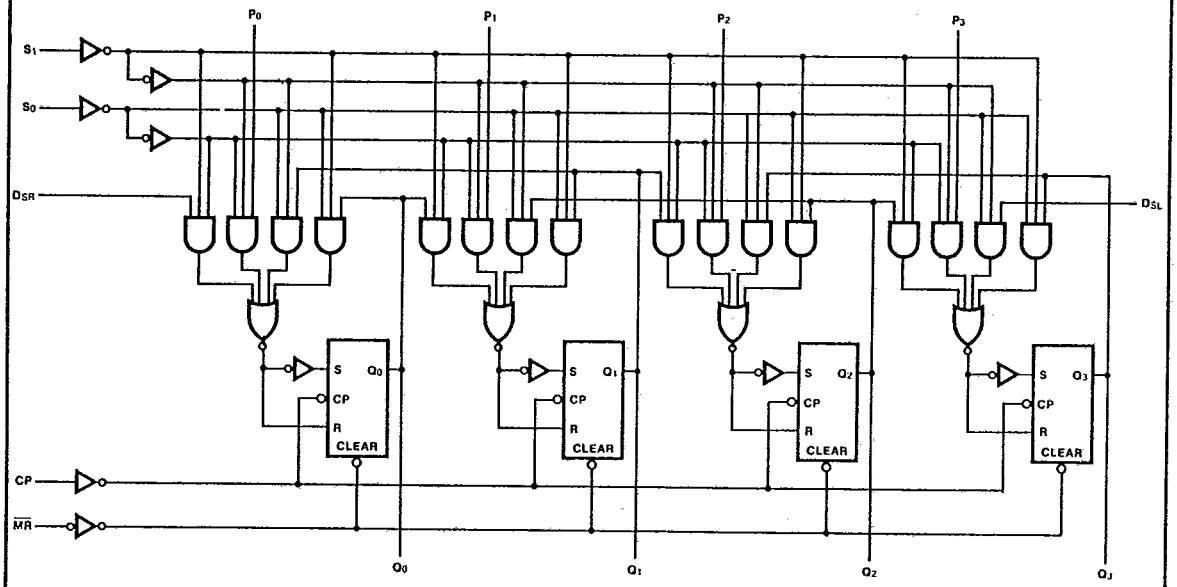
FUNCTIONAL DESCRIPTION — The '194 contains four edge-triggered D flip-flops and the necessary interstage logic to synchronously perform shift right, shift left, parallel load and hold operations. Signals applied to the Select (S_0, S_1) inputs determine the type of operation, as shown in the Mode Select Table. Signals on the Select, Parallel data (P_0 — P_3) and Serial data (D_{SR}, D_{SL}) inputs can change when the clock is in either state, provided only that the recommended setup and hold times, with respect to the clock rising edge, are observed. Synchronous state changes occur within 8.0 ns (typical, '194) or 15 ns (typical, 'LS194A), making the devices especially useful for implementing high speed memory or CPU buffer registers. A LOW signal on Master Reset ($\overline{MR}$) overrides all other inputs and forces the outputs LOW.

MODE SELECT TABLE

OPERATING MODE	INPUTS						OUTPUTS			
	$\overline{MR}$	S_1	S_0	D_{SR}	D_{SL}	P_n	Q_0	Q_1	Q_2	Q_3
Reset	L	X	X	X	X	X	L	L	L	L
Hold	H	l	l	X	X	X	q_0	q_1	q_2	q_3
Shift Left	H	h	l	X	l	X	q_1	q_2	q_3	L
	H	h	l	X	h	X	q_1	q_2	q_3	H
Shift Right	H	l	h	l	X	X	L	q_0	q_1	q_2
	H	l	h	h	X	X	H	q_0	q_1	q_2
Parallel Load	H	h	h	X	X	p_n	p_0	p_1	p_2	p_3

l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
p_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
I_{CC}	Power Supply Current		63		135		23	mA	V_{CC} = Max S_n, $\overline{MR}$, D_{SR}, D_{SL} = 4.5 V P_n = Gnd CP = ⎍

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configuration)

SYMBOL	PARAMETER	54/74		54/74S		54/74LS		UNITS	CONDITIONS
		C_L = 15 pF R_L = 400 Ω		C_L = 15 pF R_L = 280 Ω		C_L = 15 pF			
		Min	Max	Min	Max	Min	Max		
f_{max}	Maximum Shift Frequency	25		70		30		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		22 26		8.0 12		21 24	ns	
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n		30		23		26	ns	Figs. 3-1, 3-16

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74		54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW P_n or D_{SR} or D_{SL} to CP	20 20		6.0 6.0		16 16		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW P_n or D_{SR} or D_{SL} to CP	0 0		0 0		0 0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW S_n to CP	30 30		9.0 9.0		25 25		ns	
t_h (H) t_h (L)	Hold Time HIGH or LOW S_n to CP	0 0		0 0		0 0		ns	
t_w (H)	CP Pulse Width HIGH	20		7.0		17		ns	Fig. 3-8
t_w (L)	$\overline{MR}$ Pulse Width LOW	20		12		12		ns	Fig. 3-16
t_{rec}	Recovery Time $\overline{MR}$ to CP	25		5.0		18		ns	

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