DIODE-TRANSISTOR MICROLOGIC®

INTEGRATED CIRCUITS

A FAIRCHILD *COMPATIBLE CURRENT SINKING LOGIC* PRODUCT

MILITARY TEMPERATURE RANGE: −55°C to +125°C

GENERAL DESCRIPTION

The Fairchild 9930 series of Diode Transistor Micrologic is a member of the Compatible Current Sinking Logic (CCSL) family designed for use in systems where good noise immunity, medium speed, medium power, and good fan-out are required. DTμL is available in CERPAK and hermetically sealed Dual In-Line packages over the full military temperature range. Basic members of the family are active low level output AND gates commonly called NAND gates.

Noise immunity is typically 1 volt. Worst case noise immunity over the military temperature range is 400 mV. Power dissipation is typically 8.5 mW per gate function at a 50% duty cycle. The average propagation delay is 30 ns per gate function. A single 5 volt ±10% supply is used.

A variety of gate combinations is available which provides the system designer the utmost in logic flexibility and helps to reduce package requirements to a minimum. Gate outputs may be tied together to perform the wired-OR function. Some gates are provided with 2K pull-up resistors which offer improved propagation delay times. An extender is provided to increase the fan-in for some of the gates.

The 9932 buffer has active pull-up to provide increased capacitive drive and higher fan-out. The 9944 has a bare collector output to allow for wired-OR or driving of low-power lamps. Fan-in for the buffers can be extended with the use of the 9933.

The binary products are direct coupled master-slave flip-flops making operation independent of the clock pulse rise and fall times. The binary products incorporate direct clear, direct set, and buffered outputs to provide output isolation from the slave circuitry.

The V_{CC} and ground terminals of all devices are located on diagonal corners of the package which allow two degrees of freedom in routing of power and ground lines on the P/C boards. Simple loading rules are incorporated so that the fan-in and fan-out capability of each device can be quickly established.

The DTμL 9930 series is compatible with the CCSL devices which include LPDTμL, TTμL, MμL, Medium Scale Integration (MSI), and Micromatrix™ array products.

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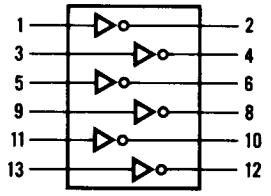
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

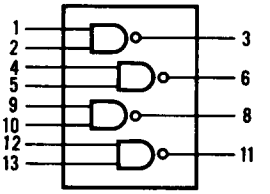
FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

9300 SERIES DTμL INTEGRATED CIRCUITS

HEX INVERTERS

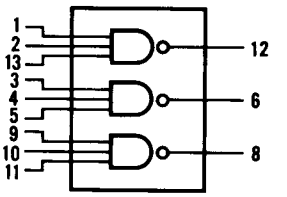


9936, 9937

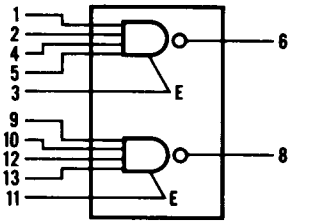


9946, 9949

NAND GATES

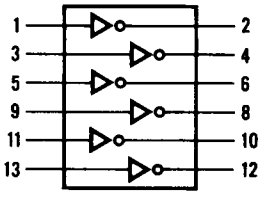


9962, 9963



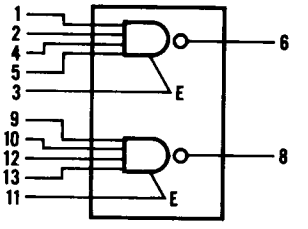
9930, 9961

EXTENDABLE HEX INVERTER



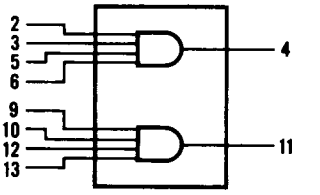
9935

BUFFERS



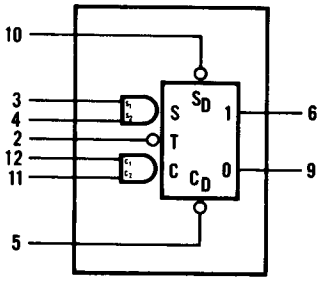
9932, 9944

EXTENDER

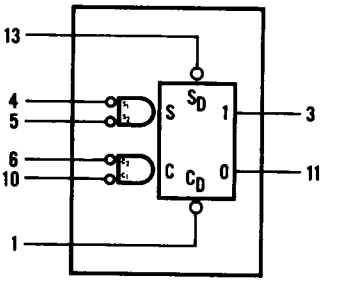


9933

BINARY ELEMENTS



9945, 9948



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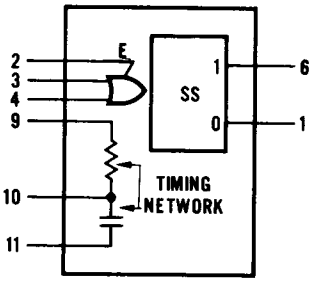
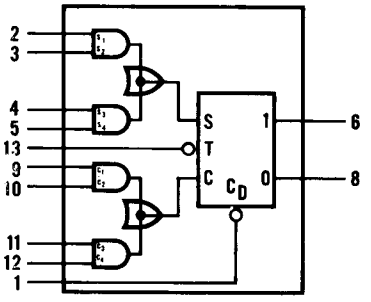
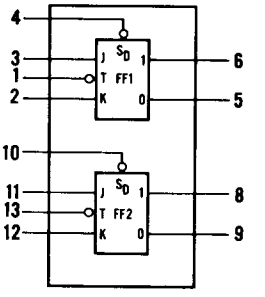


9941, 9951

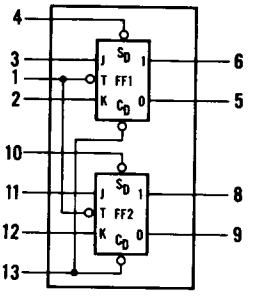


9111



9093, 9094

V_{CC} = 14
GND = 7



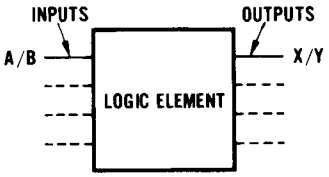
9097, 9099

ABSOLUTE MAXIMUM RATINGS (Above which useful life may be impaired)

Storage Temperature	−65°C to 150°C
Temperature (Ambient) under bias	−55°C to 125°C
V_{CC} pin potential to ground	−0.5 V to +8.0 V
V_{CC}, pulsed 1 second	12 V
Input voltage, applied to input	−1.5 V to 5.5 V
Voltage applied to output when output is high	$+V_{CC}$
Input current, into inputs	1.0 mA
Current into output when output is low (except 9932 & 9944)	30 mA
Current into output when output is low (9932 & 9944)	100 mA
Lead temperature (soldering, 60 seconds)	300°C

LOADING RULES

In this data sheet the following notation has been chosen to indicate the input loading and output drive for all logic elements.



Where
A = high logic level input load factor
B = low logic level input load factor
X = high logic level output drive factor
Y = low logic level output drive factor

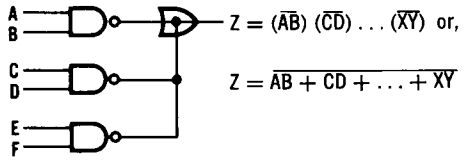
When checking for loading violations it is only necessary to insure that the sum of the high logic level input load factors at any node does not exceed the high logic level output drive factor at that node. The same is true for low logic level load and drive factors. These rules apply only within the DTμL 9930 series. For loading rules to other Fairchild logic elements refer to the CCSL Composite Data Sheet.

Multiplying the factor with the appropriate current per unit load gives the input loading or output drive in terms of current. For the DTμL circuits of this data sheet, current per unit load is -1.5 mA maximum at low logic level and is 5 μA maximum at high logic level.

In the case where unused inputs of an AND gate are shorted to a driven input, the high logic level input load factor for inputs will be the number of inputs shorted together times the high logic level input load factor for one input. The low logic level input load factor for the inputs will be the same as that for a single input.

FANOUT REDUCTION RULES FOR WIRED-OR APPLICATIONS

Each DTμL output has a pull-up resistor connected to the output (except 9932 and 9944 and 9950). In wired-OR applications, any gate must be able to sink the current from all pull-up resistors in addition to the loads connected to the common wired "AND" point. A 6K pull-up resistor represents 0.82 unit loads (U.L.) and a 2K pull-up resistor represents 2.3 U.L. To calculate the load driving capability of a wired-OR configuration simply find the total U.L. contribution of excess pull-up resistors. The FAN-OUT of the wired AND is then the fan-out of the lowest rated fan-out gate in the wired-OR combination minus the excess pull-up resistor contribution.



NAND GATES—9930, 9946, 9949, 9961, 9962, 9963
HEX INVERTERS—9936, 9937

DESCRIPTION

The 9930, 9946 and 9962 are active low NAND gates. The 9936 is a hex inverter with input and output characteristics identical to the NAND gates. The variety of gate combinations provides the system designer the utmost in logic flexibility and reduces package count.

The 9961, 9949, 9937 and 9963 are versions of the 9930, 9946, 9936 and 9962 with 2K collector pullup resistors in place of 6K pullup resistors. These gates have increased speeds and greater high level drive factors over their 6K counterparts.

Fig. 1—LOGIC SYMBOL AND PIN CONFIGURATIONS

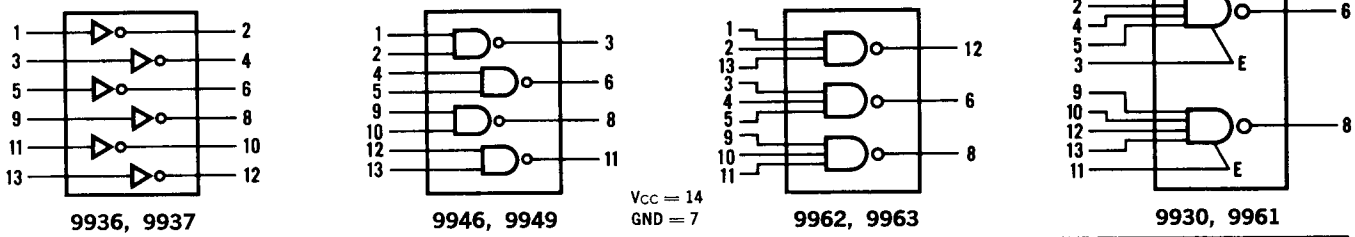
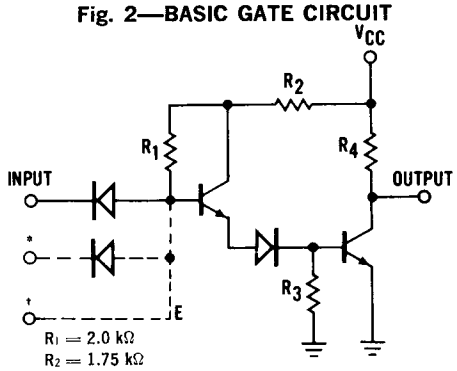


Fig. 2—BASIC GATE CIRCUIT



$R_1 = 2.0$ kΩ
$R_2 = 1.75$ kΩ
$R_3 = 5.0$ kΩ
$R_4 = 6.0$ kΩ (9930, 9936, 9946, 9962)
$R_4 = 2.0$ kΩ (9937, 9949, 9961, 9963)

* Number of inputs depends on the gate.
† 9930 and 9961 only.

Fig. 3—LOADING FACTORS (9930, 9936, 9946, 9962)

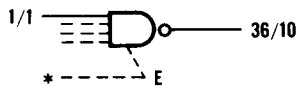
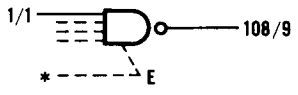


Fig. 4—LOADING FACTORS (9937, 9949, 9961, 9963)



*Extender pin on 9930, 9963 allows increased number of inputs by addition of discrete diodes or extender element DTμL9933.

TABLE I

ELECTRICAL CHARACTERISTICS OF 6K GATES — 9930, 9936, 9946 AND 9962 ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.5		2.6	3.5		2.5		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -0.18\ mA$ Inputs at V_{IL} (See Below)
V_{OL}	Output Low Voltage		0.4		0.25	0.4		0.4	Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 12\ mA$ $V_{CC} = 5.5\ V$, $I_{OL} = 15\ mA$ Inputs at V_{IH} (See Below)
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current		−1.5		−1.2	−1.5		−1.4	mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$
			−1.16		−0.93	−1.16		−1.08	mA	$V_{CC} = 4.5\ V$ 4.0 V on other inputs
I_R	Input Leakage Current					2.0		5.0	μA	$V_{CC} = 5.5\ V$, $V_R = 4.0\ V$ Ground on other inputs
I_{PD} (per gate)	V_{CC} Current "Gate On"				2.41	3.25			mA	Inputs Open $V_{CC} = 5.0\ V$
	V_{CC} Current "Gate Off"				1.15	1.47			mA	Inputs Grounded
t_{pd+}	Turn Off Delay			25	45	80			ns	$V_{CC} = 5.0\ V$, See Page 6, Fig. 7
t_{pd-}	Turn On Delay			10	20	30			ns	

TABLE II

ELECTRICAL CHARACTERISTICS OF 2K GATES — 9937, 9949, 9961 AND 9963 ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.5		2.6	3.5		2.5		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -0.54\ mA$ Inputs at V_{IL} (See Below)
V_{OL}	Output Low Voltage		0.4		0.27	0.4		0.4	Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 10.8\ mA$ $V_{CC} = 5.5\ V$, $I_{OL} = 13.5\ mA$ Inputs at V_{IH} (See Below)
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current		−1.5		−1.2	−1.5		−1.4	mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$
			−1.16		−0.93	−1.16		−1.08	mA	$V_{CC} = 4.5\ V$ 4.0 V on other inputs
I_R	Input Leakage Current					2.0		5.0	μA	$V_{CC} = 5.5\ V$, $V_R = 4.0\ V$ Ground on other inputs
I_{PD} (per gate)	V_{CC} Current "Gate On"				4.05	5.45			mA	Inputs Open $V_{CC} = 5.0\ V$
	V_{CC} Current "Gate Off"				1.15	1.47			mA	Inputs Grounded
t_{pd+}	Turn Off Delay			10	35	50			ns	$V_{CC} = 5.0\ V$, See Page 6, Fig. 7
t_{pd-}	Turn On Delay			10	20	30			ns	

ELECTRICAL CHARACTERISTICS

Fig. 5a
WORST CASE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE

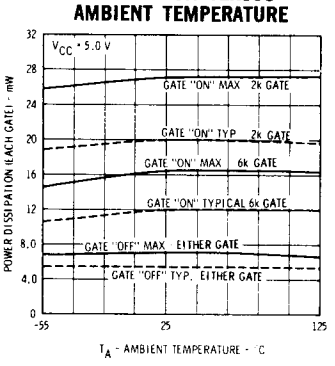


Fig. 5b
WORST CASE LOGIC LEVELS VERSUS AMBIENT TEMPERATURE

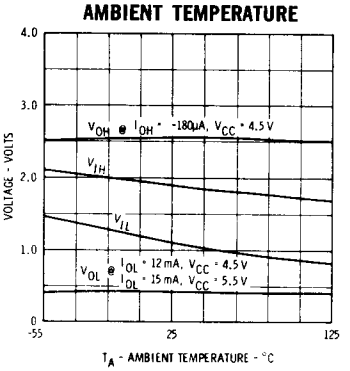


Fig. 5c
WORST CASE HIGH LEVEL NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE

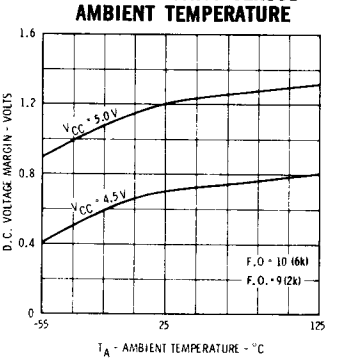


Fig. 5d
WORST CASE LOW LEVEL NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE

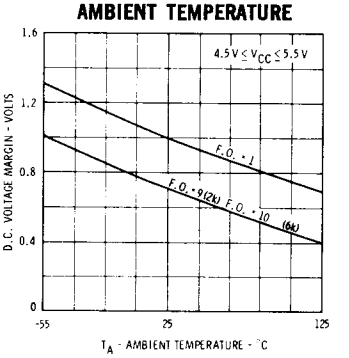


Fig. 5e
WORST CASE TURN ON DELAY VERSUS AMBIENT TEMPERATURE (6k Gates)

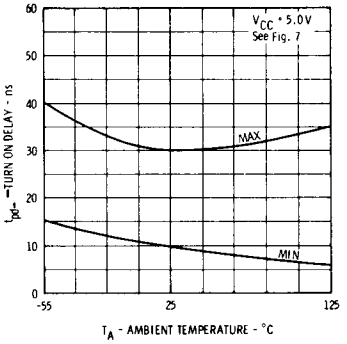


Fig. 5f
WORST CASE TURN OFF DELAY VERSUS AMBIENT TEMPERATURE (6k Gates)

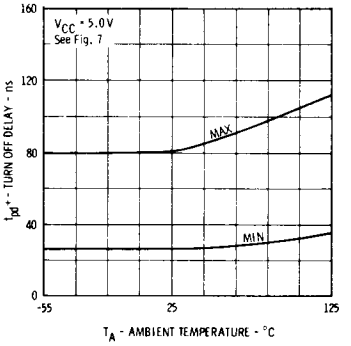


Fig. 5g
INCREASE OF PROPAGATION DELAY VERSUS CAPACITANCE (6k Gates)

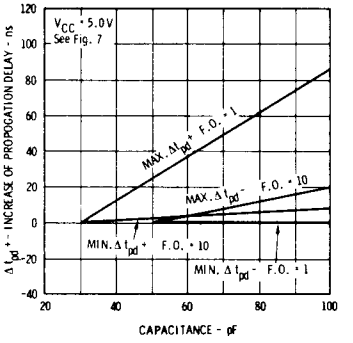


Fig. 5h
DECREASE OF TURN OFF DELAY VERSUS FANOUT (6k Gates)

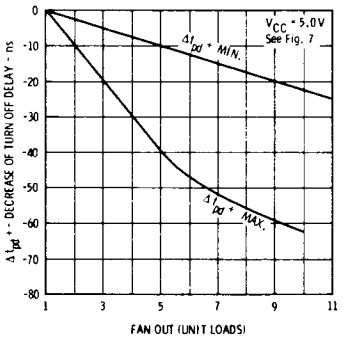


Fig. 5i
WORST CASE TURN ON DELAY VERSUS AMBIENT TEMPERATURE (2k Gates)

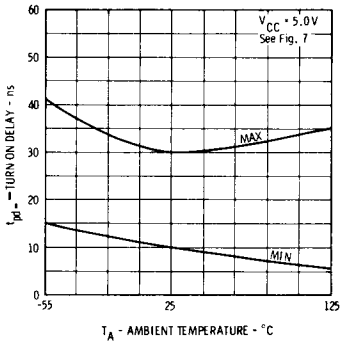


Fig. 5j
WORST CASE TURN OFF DELAY VERSUS AMBIENT TEMPERATURE (2k Gates)

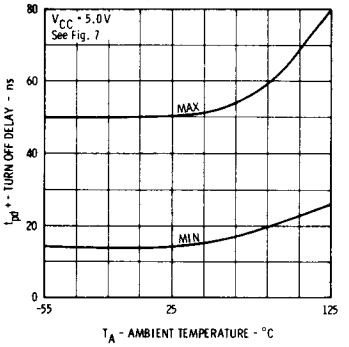


Fig. 5k
INCREASE OF PROPAGATION DELAY VERSUS CAPACITANCE (2k Gates)

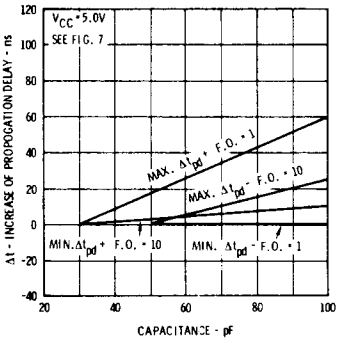
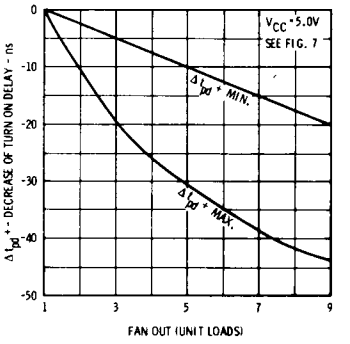


Fig. 5l
DECREASE OF TURN ON DELAY VERSUS FANOUT (2k Gates)



INPUT AND OUTPUT CHARACTERISTICS

Fig. 6a
TYPICAL INPUT CURRENT VERSUS INPUT VOLTAGE (6k & 2k Gates)

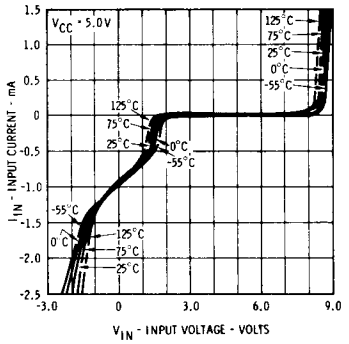


Fig. 6b
TYPICAL OUTPUT VOLTAGE VERSUS INPUT VOLTAGE (6k & 2k Gates)

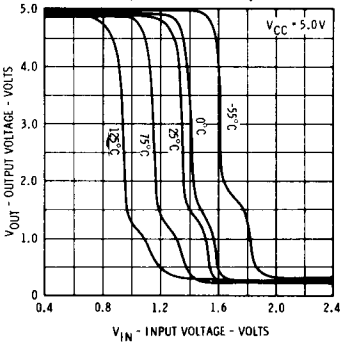


Fig. 6c
TYPICAL OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (6k & 2k Gates)

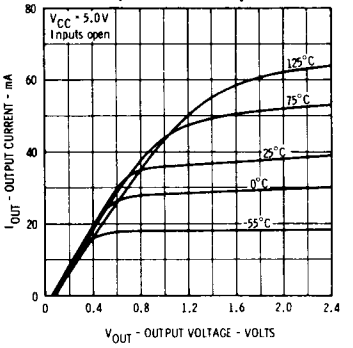


Fig. 6d
TYPICAL OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (2k Gates)

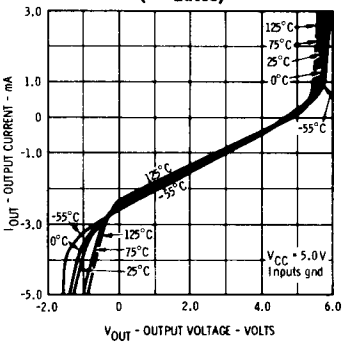


Fig. 6e
TYPICAL OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (6k Gates)

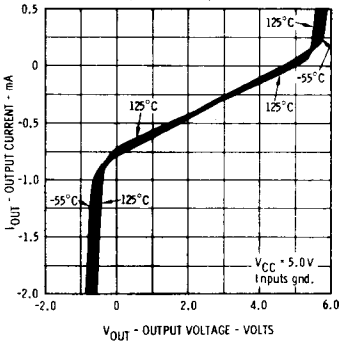
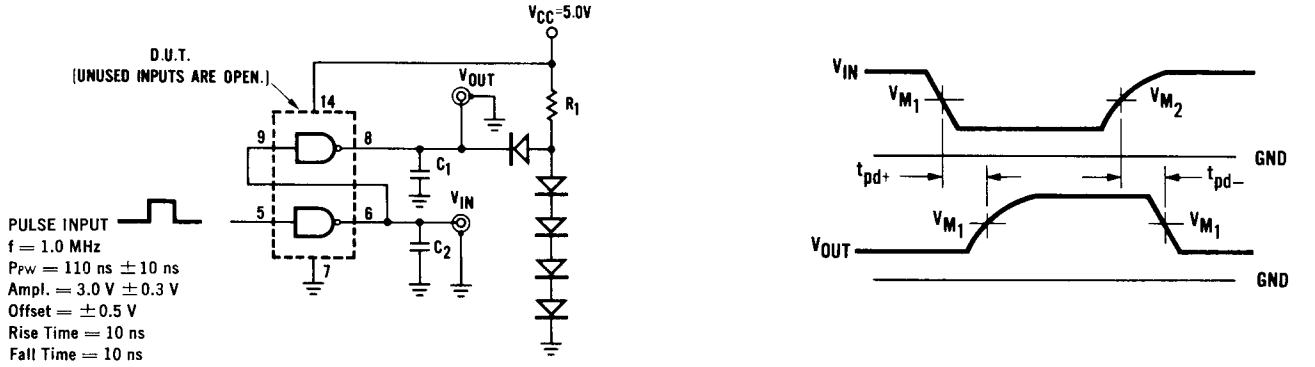


Fig. 7—t_{pd} TEST CIRCUIT AND WAVEFORMS



	t_{pd+}	t_{pd-}
R_1	3.9 kΩ	400 Ω
C_1	30 pF	50 pF
C_2	20 pF	20 pF

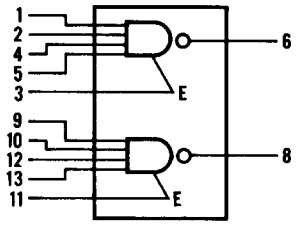
Diodes are FD600.
C_1 and C_2 include all jig and probe capacitance

Temp.	V_{m1} (Volts)	V_{m2} (Volts)
−55°C	1.7	1.5
25°C	1.5	1.3
125°C	1.2	1.0

BUFFER ELEMENTS—9932 AND 9944

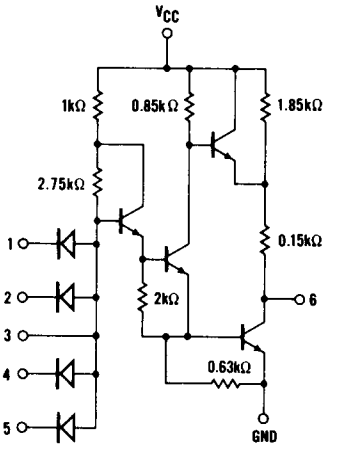
The DTμL 9932 and DTμL 9944 are dual "NAND" power gates capable of driving and sinking large currents for high fan-out applications. The DTμL 9932 features an emitter-follower output pull-up, which provides a high fan-out device with superior capacitance-driving capability. The DTμL 9944 is intended as a high fan-out gate interface driver, or low power lamp driver.

Fig. 1—LOGIC DIAGRAM AND PIN CONFIGURATION 9932, 9944



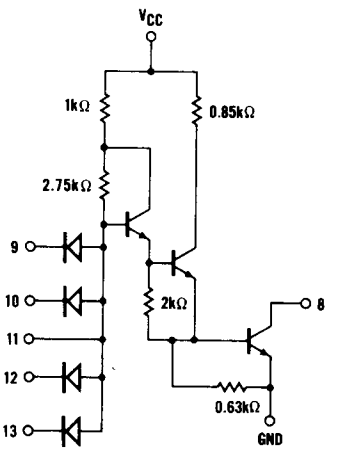
V_{CC} = 14
GND = 7

Fig. 2—SCHEMATIC DIAGRAM OF THE DTμL 9932 ELEMENT (ONE GATE)



V_{CC} = 14
GND = 7

Fig. 3—SCHEMATIC DIAGRAM OF THE DTμL 9944 ELEMENT (ONE GATE)



V_{CC} = 14
GND = 7

Fig. 4—LOADING FACTORS (9932)

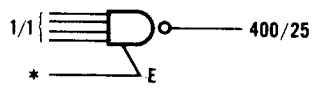
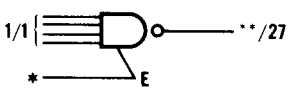


Fig. 5—LOADING FACTORS (9944)



NOTES:

1. Extender pin (*) allows increased number of inputs by addition of discrete diodes or extender element DTμL9933.
2. (**) denotes the need for an external resistor to provide high level drive capability. The use of an external resistor will then detract from the low level drive factor as follows: subtract one (1) fan-out for every 3.4 kΩ path from V_{CC} to output.
3. 9932 outputs cannot be wired-OR.

TABLE I

ELECTRICAL CHARACTERISTICS — 9932 ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.5		2.6	2.8		2.5		Volts	$V_{CC} = 4.5\ V$ Inputs at V_{IL} (See Below) | $I_{OH} = -2.0$ mA at −55°C; $= -2.5$ mA at 25°C; $= -4.0$ mA at 125°C
V_{OL}	Output Low Voltage		0.4		0.27	0.4		0.4	Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 36$ mA; $V_{CC} = 5.5\ V$, $I_{OL} = 37.5$ mA; Inputs at V_{IH} (See Below)
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed Input High Threshold For All Inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	Volts	Guaranteed Input Low Threshold For All Inputs
I_F	Input Load Current		−1.5		−1.2	−1.5		−1.4	mA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$
			−1.16		−0.93	−1.16		−1.08	mA	$V_{CC} = 4.5\ V$, $V_F = 0.4\ V$
I_R	Input Leakage Current					2.0		5.0	μA	$V_R = 4.0\ V$ Other inputs grounded
I_{PD}	V_{CC} Current "Gate On"				10	13.3			mA	$V_{CC} = 5.0\ V$, Inputs Open
(per gate)	V_{CC} Current "Gate Off"				1.15	1.47			mA	$V_{CC} = 5.0\ V$, Inputs Grounded
t_{pd+}	Turn Off Delay			25	50	80			ns	$V_{CC} = 5.0\ V$, See Page 8, Fig. 7
t_{pd-}	Turn On Delay			15	25	40			ns	

TABLE II

ELECTRICAL CHARACTERISTICS — 9944 ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OL}	Output Low Voltage		0.4		0.27	0.4		0.4	Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 36$ mA; $V_{CC} = 5.5\ V$, $I_{OL} = 37.5$ mA; Inputs at V_{IH} (see below)
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	Volts	Guaranteed input low threshold for all inputs
I_{CEX}	Output Leakage		50			100		200	μA	$V_{CEX} = 4.5\ V$ Inputs at V_{IL} (see above)
I_F	Input Load Current		−1.5		−1.3	−1.5		−1.4	mA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$
			−1.16		−1.0	−1.16		−1.08	mA	$V_{CC} = 4.5\ V$, $V_F = 0.4\ V$
I_R	Input Leakage Current				0.02	2.0		5.0	μA	$V_R = 4.0\ V$ Other inputs grounded
I_{PD}	V_{CC} Current "Gate On"				7.6	10			mA	$V_{CC} = 5.0\ V$, Inputs Open
(per gate)	V_{CC} Current "Gate Off"				1.15	1.47			mA	$V_{CC} = 5.0\ V$, Inputs Grounded
t_{pd+}	Turn Off Delay			15	35	50			ns	$V_{CC} = 5.0\ V$, See Page 8, Fig. 8
t_{pd-}	Turn On Delay			10	20	35			ns	

9932 AND 9944 ELECTRICAL CHARACTERISTICS

Fig. 6a
WORST CASE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE

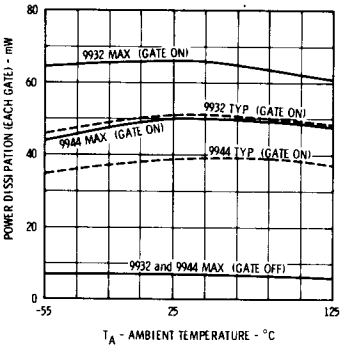


Fig. 6b
WORST CASE LOGIC LEVELS VERSUS AMBIENT TEMPERATURE

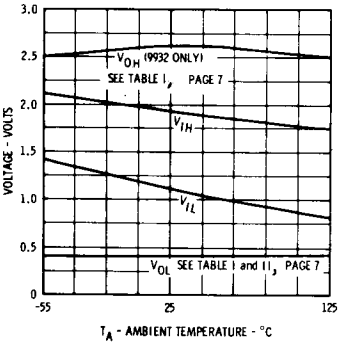


Fig. 6c
WORST CASE HIGH LEVEL NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE (9932 ONLY)

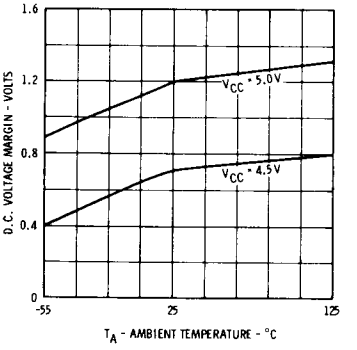


Fig. 6d
WORST CASE LOW LEVEL NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE

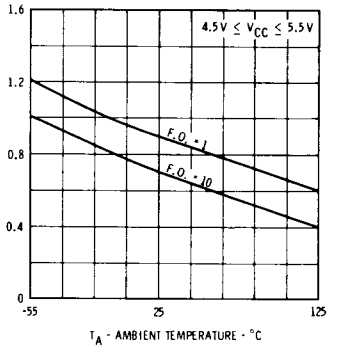


Fig. 6e
TYPICAL INPUT CURRENT VERSUS INPUT VOLTAGE

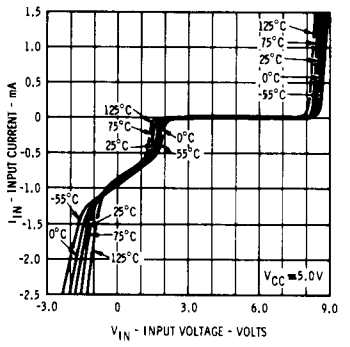


Fig. 6f
TYPICAL OUTPUT VOLTAGE VERSUS INPUT VOLTAGE (9932 ONLY)

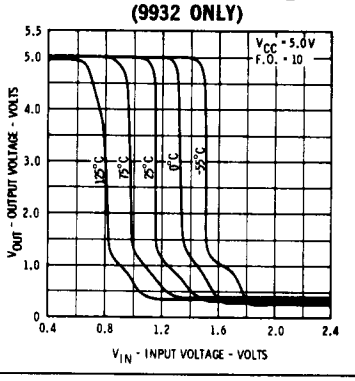


Fig. 6g
TYPICAL OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (9932 ONLY)

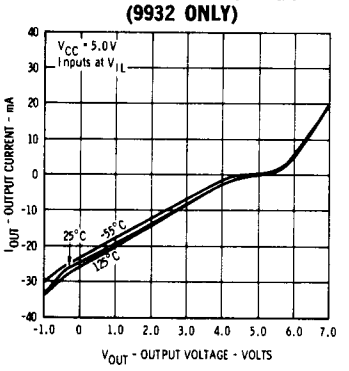
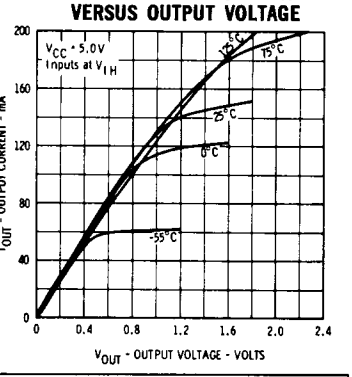
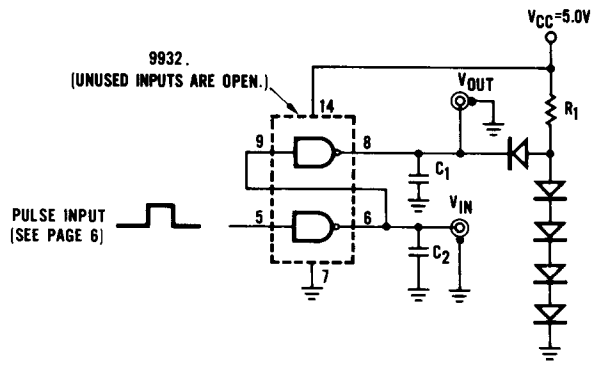


Fig. 6h
TYPICAL OUTPUT CURRENT VERSUS OUTPUT VOLTAGE



SWITCHING CHARACTERISTICS

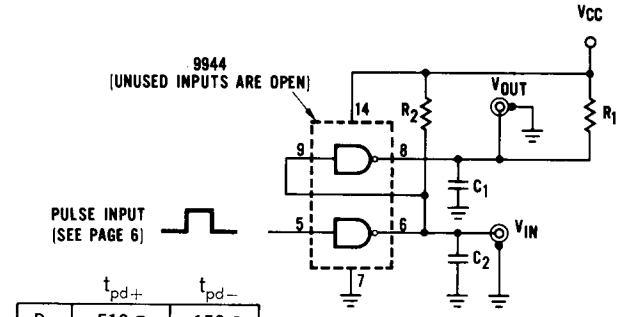
Fig. 7—t_{pd} TEST CIRCUIT FOR DTμL 9932 ELEMENT



	t_{pd+}	t_{pd-}
R_1	510 Ω	150 Ω
C_1	500 pF	500 pF
C_2	20 pF	20 pF

All Diodes are FD600 or Equivalent
C_1 and C_2 include Probe and Jig Capacitance

Fig. 8—t_{pd} TEST CIRCUIT FOR DTμL 9944 ELEMENT



	t_{pd+}	t_{pd-}
R_1	510 Ω	150 Ω
R_2	2 kΩ	2 kΩ
C_1	20 pF	100 pF
C_2	20 pF	20 pF

Fig. 9—WAVEFORMS FOR 9932 AND 9944

Temp.	V_M (Volts)
−55°C	1.7
25°C	1.5
125°C	1.2

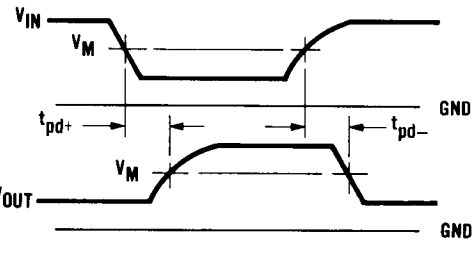


Fig. 10a
WORST CASE TURN ON DELAY VERSUS AMBIENT TEMPERATURE

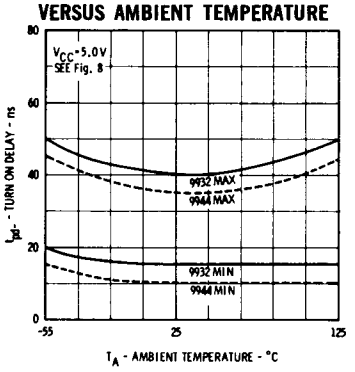


Fig. 10b
WORST CASE TURN OFF DELAY VERSUS AMBIENT TEMPERATURE

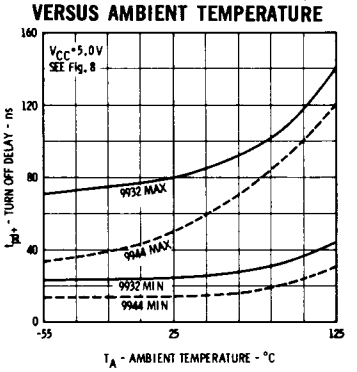
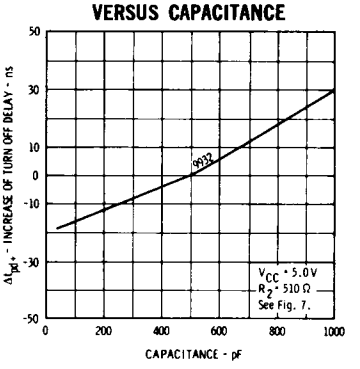


Fig. 10c
INCREASE OF TURN OFF DELAY VERSUS CAPACITANCE



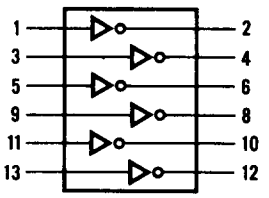
EXTENDABLE HEX INVERTER — 9935

A 9935 inverter is intended for use with discrete diode expansion of the input. Input load and drive factors can be calculated with the aid of the curves on Page 11 and the forward/reverse characteristics of the diode used.

A single 9935 inverter can be driven directly by the outputs of other DTμL elements, with the exception of 9932 and 9950, providing no more than 5 mA is allowed to flow into the input of the 9935. Commoning 9935 inputs is not a recommended configuration.

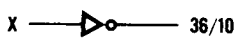
When extending inputs with diodes, care should be taken to minimize capacitance on the input node as turn on delay will be increased by 2 ns per picofarad of stray capacitance at this node.

Fig. 1—LOGIC DIAGRAM AND PIN CONFIGURATION



V_{CC} = 14
GND = 7

Fig. 3—LOADING FACTORS



X = input to be used with 9933 or discrete diode.

Fig. 2—SCHEMATIC DIAGRAM (ONE INVERTER ONLY)

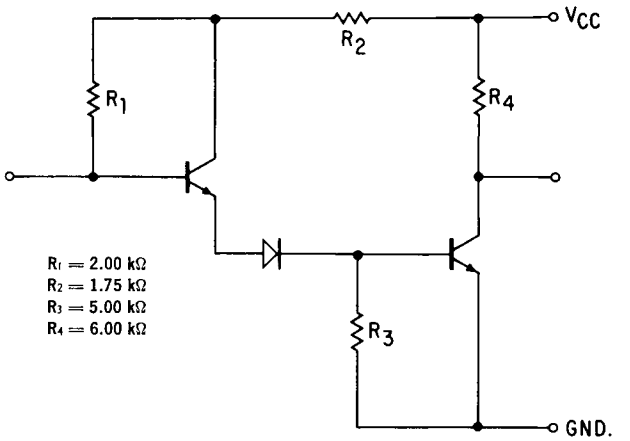


TABLE I

ELECTRICAL CHARACTERISTICS — 9935 (T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10%)

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	−55°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+125°C MIN.	+125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage		2.5		3.5	2.6		2.5	Volts	V_{CC} = 4.5 V, I_{OH} = −0.18 mA Inputs at V_{IL}
V_{OL}	Output Low Voltage		0.4		0.25	0.4		0.4	Volts	V_{CC} = 4.5 V, I_{OL} = 12 mA V_{CC} = 5.5 V, I_{OL} = 15 mA Inputs at V_{IH}
V_{IH}	Input High Voltage	2.3		2.0			1.8		Volts	Guaranteed input high threshold with FD600 diode
V_{IL}	Input Low Voltage		1.4			1.1		0.8	Volts	Guaranteed input low threshold with FD600 diode
I_F	Input Load Current		−1.5		−1.2	−1.5		−1.5	mA	V_{CC} = 5.5 V, V_F = 0.4 V — FD600 Diode
			−1.2		−0.93	−1.2		−1.2	mA	V_{CC} = 4.5 V, V_F = 0.4 V — on input
I_{PD} (per gate)	V_{CC} Current "Gate On"				2.41	3.1			mA	V_{CC} = 5.0 V, Inputs open
	V_{CC} Current "Gate Off"				1.33	1.7			mA	V_{CC} = 5.0 V, Inputs gnd.
t_{pd+}	Turn Off Delay			25	65	80			ns	V_{CC} = 5.0 V, See Page 10, Fig. 5
t_{pd-}	Turn On Delay			10	30	40			ns	

9935 ELECTRICAL CHARACTERISTICS

Fig. 4a
WORST CASE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE (EACH INVERTER)

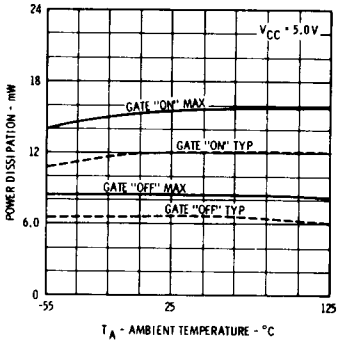


Fig. 4b
WORST CASE LOGIC LEVELS VERSUS AMBIENT TEMPERATURE

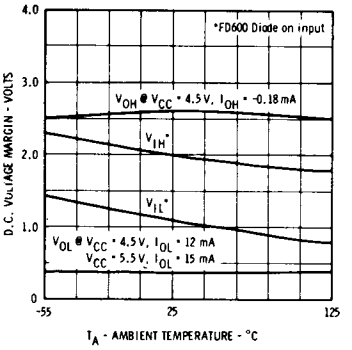


Fig. 4c
HIGH INPUT THRESHOLD VOLTAGE VERSUS FORWARD EXTENDER DIODE VOLTAGE

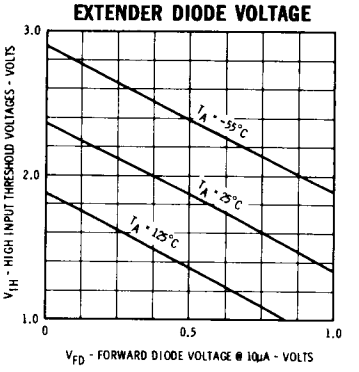


Fig. 4d
WORST CASE HIGH LEVEL NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE

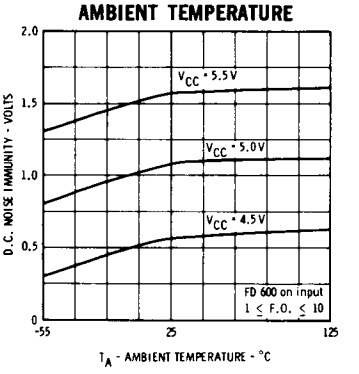


Fig. 4e
WORST CASE LOW LEVEL NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE

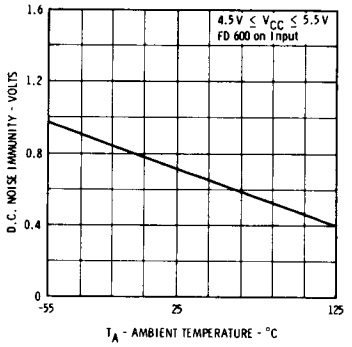


Fig. 4f
LOW INPUT THRESHOLD VOLTAGE VERSUS FORWARD DIODE VOLTAGE

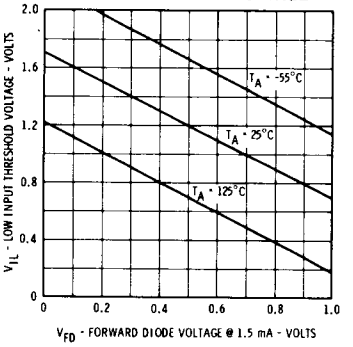


Fig. 4g
WORST CASE TURN OFF DELAY VERSUS AMBIENT TEMPERATURE

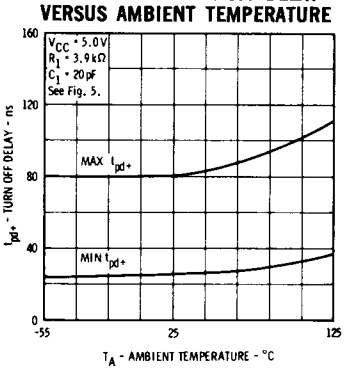


Fig. 4h
WORST CASE TURN ON DELAY VERSUS AMBIENT TEMPERATURE

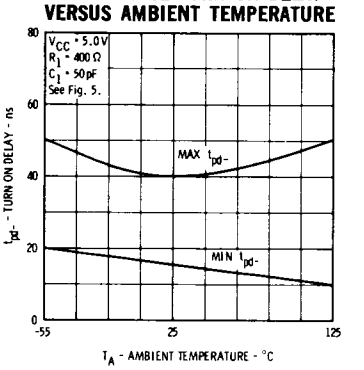
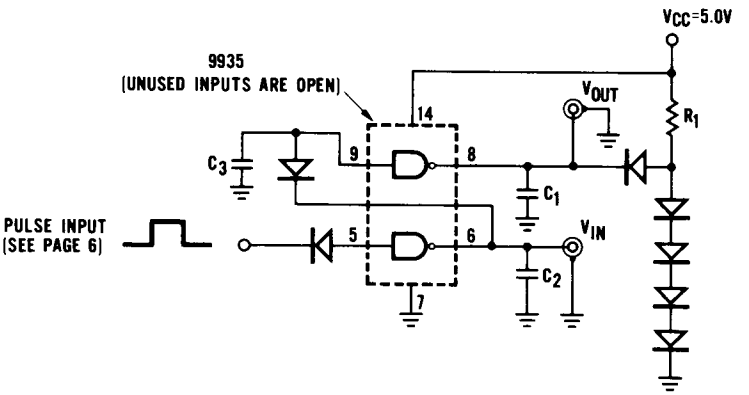


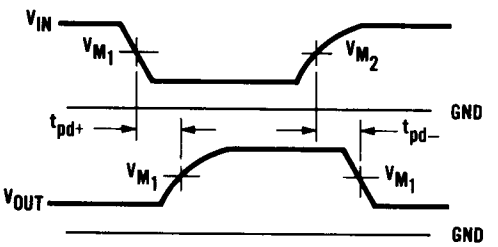
Fig. 5—SWITCHING TIME TEST CIRCUIT



	t_{pd+}	t_{pd-}
R_1	3.9 k	400 Ω
C_1	30 pF	50 pF
C_2	20 pF	20 pF
C_3	5 pF	5 pF

Diodes are FD600 or equivalent

C_1 and C_2 include Jig and Probe Capacitance



Temp.	V_{m1} (Volts)	V_{m2} (Volts)
−55°C	1.7	1.5
+25°C	1.5	1.3
+125°C	1.2	1.0

DTμL EXTENDER ELEMENT—9933

The DTμL 9933 is a dual four-input extender element. DTμL 9933 elements may be used to extend fan-in capability to more than 20 without adversely affecting the noise immunity or load driving capability of the element to which they are connected.
Typical input capacitance of DTμL 9933 is 2.0 pF and output capacitance is 5.0 pF.

Fig. 1—LOGIC DIAGRAM AND PIN CONFIGURATION

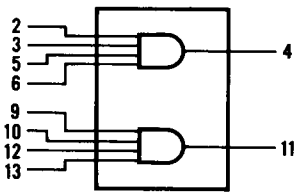
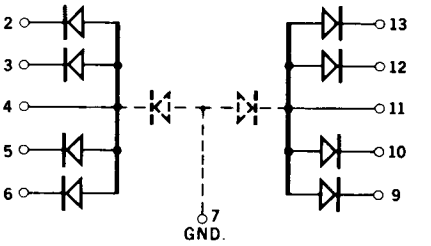


Fig. 2—SCHEMATIC DIAGRAM



9933 ELECTRICAL CHARACTERISTICS

Fig. 3a TYPICAL FORWARD AND REVERSE CHARACTERISTICS (WITH 9933)

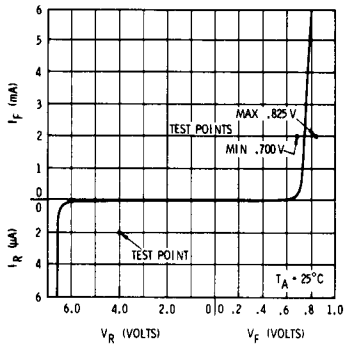


Fig. 4a WORST CASE PROPAGATION DELAY VERSUS EXTENDER PIN CAPACITANCE (WITH 9930, 9935, 9963)

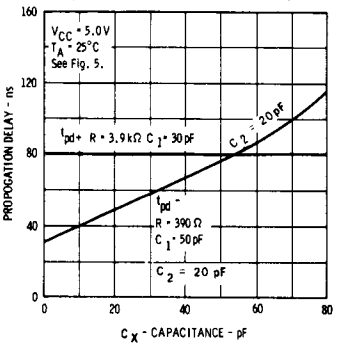


Fig. 4b WORST CASE PROPAGATION DELAY VERSUS EXTENDER PIN CAPACITANCE (WITH 9932)

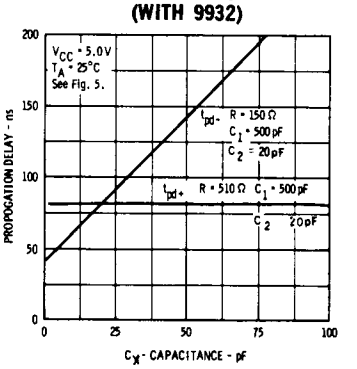
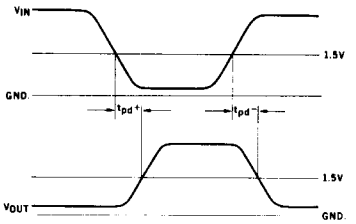
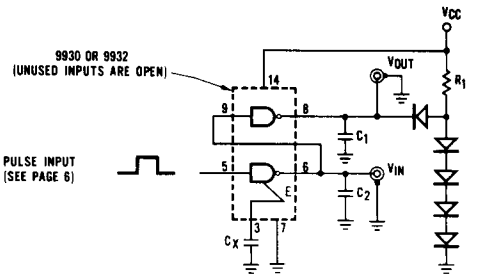


Fig. 5—WAVEFORMS AND TEST CIRCUIT





Diodes are FD600

C_X represents the summation of the DTμL 9933 Dual Extender Element output capacitances (~5.0 pF per output) and associated board, connector and wiring capacitances.

Typical Curves to Show the Effects of Extender Pin Capacitance on Noise Threshold of DTμL9930 Dual Gate

Fig. 6a PULSED GROUND NOISE THRESHOLD AS A FUNCTION OF EXTENDER PIN CAPACITANCE

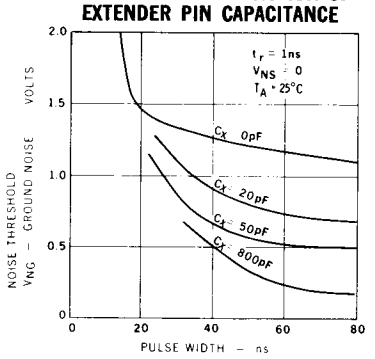


Fig. 6b PULSED SIGNAL LINE NOISE THRESHOLD AS A FUNCTION OF EXTENDER PIN CAPACITANCE

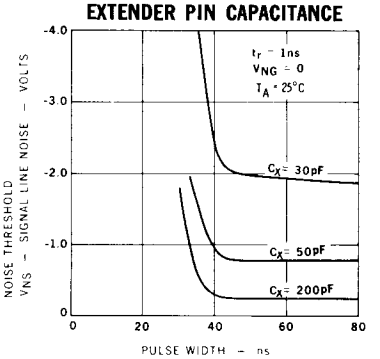
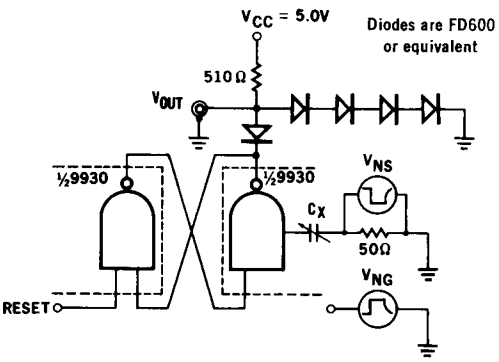


Fig. 6c TEST CONDITIONS



R-S FLIP-FLOPS 9945, 9948 AND 9111
DUAL J-K FLIP-FLOPS 9093, 9094, 9097 AND 9099

GENERAL DESCRIPTION

The DTμL 9930 series has seven flip-flops to satisfy the storage requirements of a logic system. Four flip-flops are dual J-K designs with buffered outputs, allowing the wired-OR configuration to be used. The other three flip-flops operate in the R-S mode and can be converted to J-K operation with external cross-coupled connections. All flip-flops incorporate the master-slave design which offers the advantage of a D.C. threshold on the clock input initiating the transition of the outputs, so that careful control of the clock pulse rise and fall times is not required.

Data is accepted by the master flip-flop while the clock is high. Refer to truth table for definition of "one" and "zero" levels. Transfer from the master flip-flop to the slave flip-flop occurs on the high to low transition of the clock. When the clock is low, the J, K, S, and C inputs are inhibited.

The asynchronous inputs provide ability to control the state of the flip-flop independent of static conditions on the clock and synchronous inputs. Both asynchronous set and clear are provided on the 9945, 9948, 9097 and 9099. The 9093 and 9094 have only asynchronous set inputs, and the 9111 has only asynchronous clear inputs.

LOGIC DIAGRAMS AND LOADING FACTORS

Fig. 1—9945

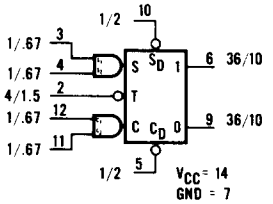


Fig. 2—9093

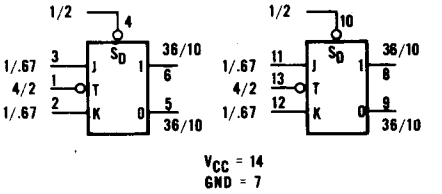


Fig. 3—9948

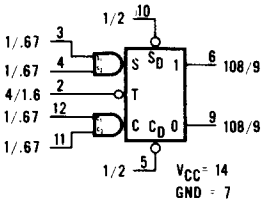


Fig. 4—9094

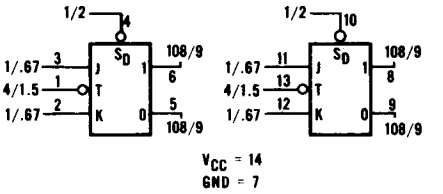


Fig. 5—9111

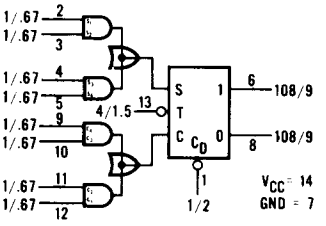


Fig. 6—9097

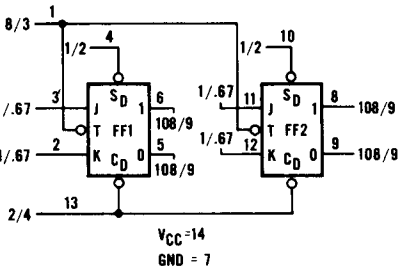


Fig. 7 9945/9948 (J-K MODE)

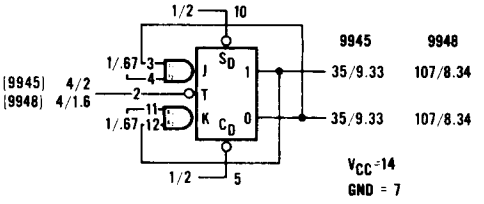
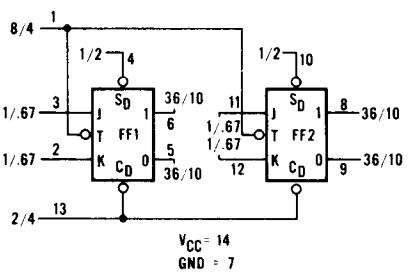


Fig. 8 9099



FUNCTIONAL LOGIC DIAGRAMS

Fig. 9—9945, 9948 AND 9111

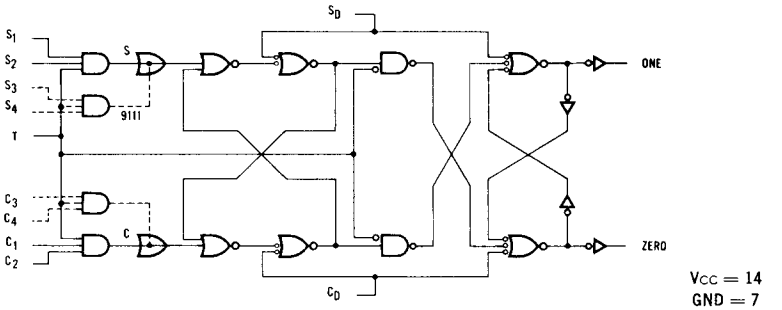
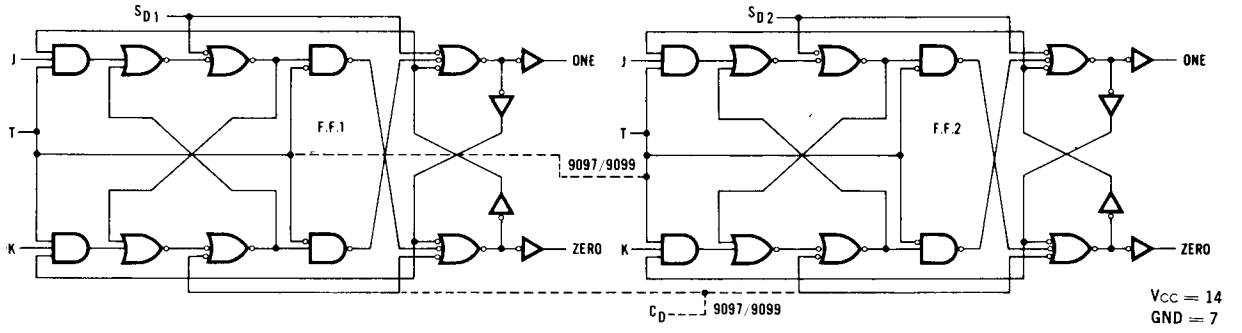


Fig. 10—9093, 9094, 9097 AND 9099



SYNCHRONOUS OPERATION

The truth table defines the next state of the flip-flop after a high to low transition of the clock pulse. The output of all flip-flops operating in the J-K mode is a function of the previous state of the flip-flop and the condition of the inputs prior to a high to low transition of the clock. The output of all flip-flops operating in the R-S mode is a function of the S and C inputs at the time of a high to low clock transition.

The S and C inputs in the table refer to the basic S and C inputs as indicated on the logic diagrams of the 9945, 9948, and 9111. These internal inputs are the result of a logic operation on the external S and C inputs. This operation is represented symbolically by "AND" gates in the logic diagram for each flip-flop. Logic diagrams are in accordance with MIL STANDARD 806B.

The L* symbol in the J, K, C, and S input columns is defined as that input does not go high at any time while the clock is high.

The H* symbol in the J, K, C, and S input columns is defined as that the input is high at some time while the clock is high.

The X symbol indicates that the condition of that input or output has no effect on the next state of the flip-flop.

The H and L symbols refer to steady state high and low voltage levels, respectively.

TABLE I
SYNCHRONOUS OPERATION
R-S FLIP-FLOP

BEFORE CLOCK				OUTPUTS AFTER CLOCK	
OUTPUTS		INPUTS			
ONE	ZERO	S	C	ONE	ZERO
L	H	L*	L*	L	H
H	L	L*	L*	H	L
X	X	L	H*	L	H
X	X	H*	L	H	L
X	X	H	H	Undetermined	

TABLE II
SYNCHRONOUS OPERATION
J-K FLIP-FLOP

BEFORE CLOCK				OUTPUTS AFTER CLOCK	
OUTPUTS		INPUTS			
ONE	ZERO	J	K	ONE	ZERO
L	H	L*	X	L	H
L	H	H*	X	H	L
H	L	X	L*	H	L
H	L	X	H*	L	H

TABLE III
ASYNCHRONOUS OPERATION

INPUTS		OUTPUTS	
S_D	C_D	ONE	ZERO
L	L	H	H
L	H	H	L
H	L	L	H
H	H	State determined by synchronous inputs and clock input	

ELECTRICAL CHARACTERISTICS—BINARY ELEMENTS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage									
	(9945, 9093, 9099)	2.5		2.5	3.3		2.5		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -180\ \mu A$
	(9948, 9094, 9097, 9111)	2.5		2.5	3.3		2.5			$V_{CC} = 4.5\ V$, $I_{OH} = -540\ \mu A$
V_{OL}	Output Low Voltage		0.4		0.25	0.4		0.4	Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 12.0\ mA$
	(9945, 9093, 9099)									$V_{CC} = 5.5\ V$, $I_{OL} = 15.0\ mA$
	(9948, 9094, 9097, 9111)		0.4		0.25	0.4		0.4		$V_{CC} = 4.5\ V$, $I_{OL} = 13.0\ mA$ (@ −55°C)
										$V_{CC} = 5.5\ V$, $I_{OL} = 13.6\ mA$
V_{IH}	Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	Volts	Guaranteed input low threshold for all inputs
I_R	Input Leakage, all J-K S, C, S_D, C_D inputs (except C_D of 9097, 9099)					2.0		5.0	μA	$V_{CC} = 5.5\ V$, $V_R = 4.0\ V$ Gnd on other inputs
	Input Leakage of C_D (9097, 9099)					4.0		10		
I_{RCP}	Input Leakage, CP inputs									
	(9945, 9948, 9093, 9094, 9111)					10		20		
	(9097, 9099)					20		40		
I_F	Input Current, all J, K, S, C inputs		−.98		−.82	−.98		−.92	mA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$, 4.0 V on other inputs
	Input Current, S_D or C_D (9093, 9094, 9111)		−2.2		−1.8	−2.2		−1.93		
	Input Current, CP inputs									
	(9945, 9093)		−2.93		−2.40	−2.93		−2.57		
	(9948, 9094)		−2.35		−1.93	−2.35		−2.03		
	(9111)		−3.76		−3.00	−3.76		−3.76		
	(9097)		−4.68		−3.84	−4.68		−4.04		
	(9099)		−5.86		−4.81	−5.86		−5.14		
I_F	Input Current, all J, K, S, C inputs		−0.76		−0.62	−0.76		−0.72	mA	$V_{CC} = 4.5\ V$, $V_F = 0.4\ V$, 4.0 V on other inputs
	Input Current, S_D or C_D inputs (9093, 9094, 9111)		−1.7		−1.39	−1.7		−1.5		
	Input Current, CP inputs									
	(9945, 9093)		−2.26		−1.85	−2.26		−2.02		
	(9948, 9094)		−1.83		−1.50	−1.83		−1.59		
	(9111)		−2.90		−2.48	−2.90		−2.88		
	(9097)		−3.66		−3.00	−3.66		−3.18		
	(9099)		−4.52		−3.70	−4.52		−4.04		
I_{FSI}	Input Current, C_D, S_D inputs		−2.93		−2.40	−2.93		−2.57	mA	$V_{CC} = 5.5\ V$; $V_F = 0.4\ V$
	(9945, 9948, 9097, 9099)		−2.26		−1.85	−2.26		−2.20		$V_{CC} = 4.5\ V$; 4.0 V on other inputs
I_{PD}	V_{CC} Current									
	(9945)				8.3	14.0			mA	$V_{CC} = 5.0\ V$, all inputs open
	(9948)				9.9	16.2				Momentary ground on S_D
	(9111)				12.1	18.0				
	(9093)				16.6	28.0				
	(9094)				19.8	32.4				
	(9097)				19.8	32.4				
	(9099)				16.6	28.0				

INPUT AND OUTPUT CHARACTERISTICS OF BINARY ELEMENTS

Fig. 11
TYPICAL OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

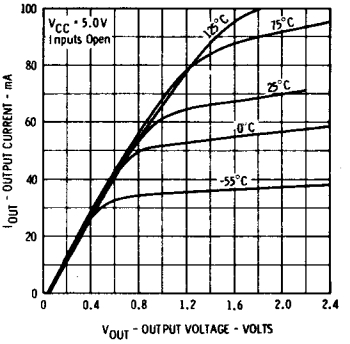


Fig. 12
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

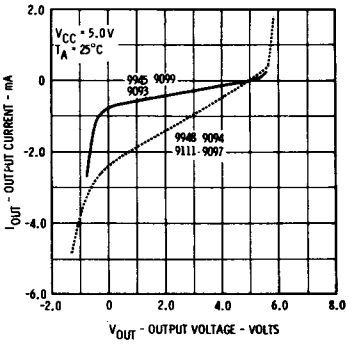


Fig. 13
CLOCK INPUT CURRENT VERSUS CLOCK INPUT VOLTAGE (9945, 9093, 9099)

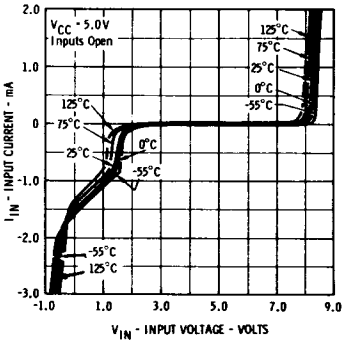


Fig. 14
INPUT CURRENT VERSUS INPUT VOLTAGE - CLOCK INPUT (9948, 9094)

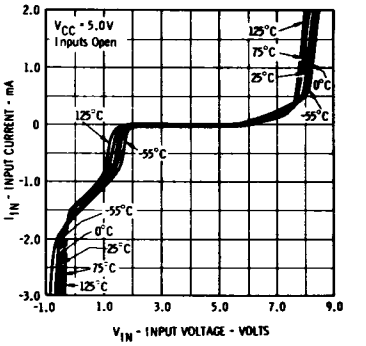


Fig. 15
INPUT CURRENT VERSUS INPUT VOLTAGE CLOCK INPUT (9111)

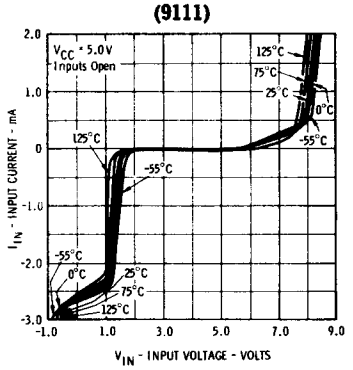


Fig. 16
INPUT CURRENT VERSUS INPUT VOLTAGE CLOCK INPUT (9097)

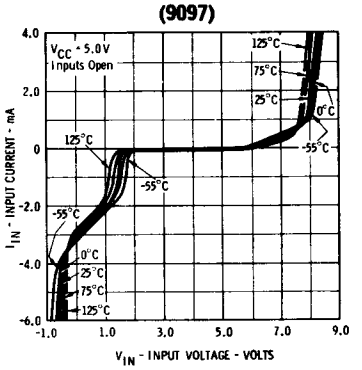


Fig. 17
CLOCK INPUT CURRENT VERSUS CLOCK INPUT VOLTAGE (9099)

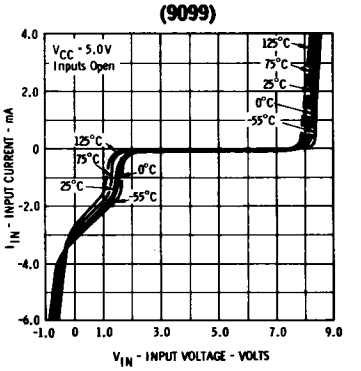


Fig. 18
INPUT CURRENT VERSUS INPUT VOLTAGE SYNCHRONOUS INPUTS

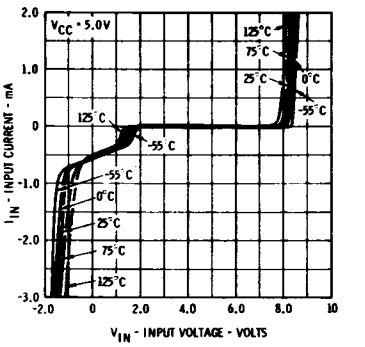


Fig. 19
INPUT CURRENT VERSUS INPUT VOLTAGE ASYNCHRONOUS INPUTS

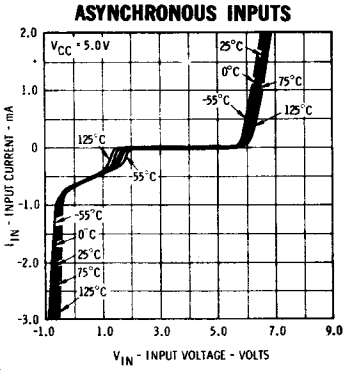


Fig. 20
OUTPUT VOLTAGE VERSUS CLOCK INPUT VOLTAGE (9945, 9093, 9099)

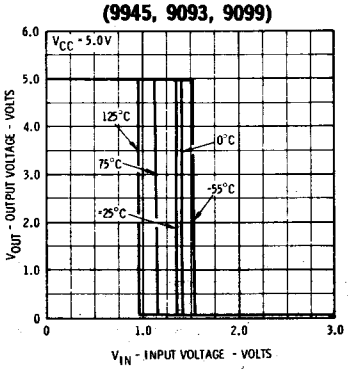


Fig. 21
OUTPUT VOLTAGE VERSUS CLOCK INPUT VOLTAGE (9948, 9094, 9097)

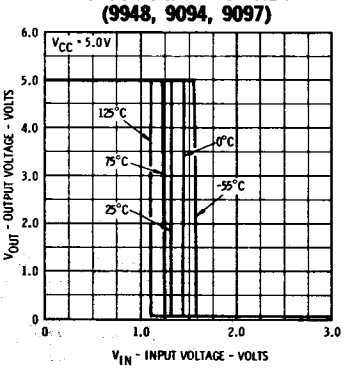
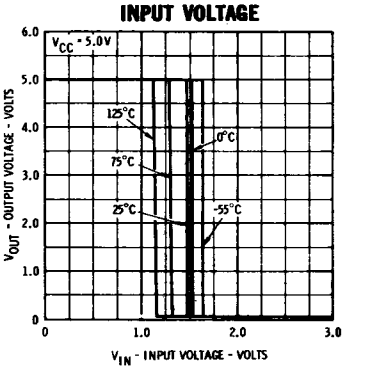


Fig. 22
OUTPUT VOLTAGE VERSUS ASYNCHRONOUS INPUT VOLTAGE



SWITCHING CHARACTERISTICS ($T_A = 25°C$, $V_{CC} = 5.0$ V)

SYMBOL	CHARACTERISTIC	9094, 9097, 9111 and 9948 MIN.	TYP.	MAX.	9093, 9099 and 9945 MIN.	TYP.	MAX.	UNITS	FIGURES
t_{pd+}	Clock to Output	30		65	35		75	ns	28, 29, 30
t_{pd-}	Clock to Output	30		75	30		75	ns	
$t_{set\text{-}up}$		35	22		35	22		ns	
$t_{release}$			14	10		14	10	ns	

Fig. 23
WORST CASE TURN OFF DELAY VERSUS AMBIENT TEMPERATURE

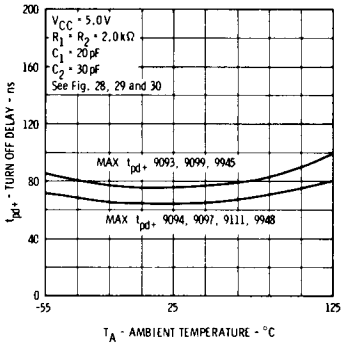


Fig. 24
WORST CASE TURN ON DELAY VERSUS AMBIENT TEMPERATURE

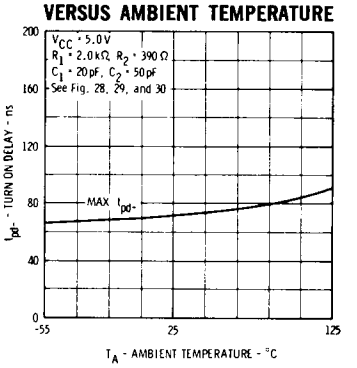


Fig. 25
WORST CASE INCREASE OF PROPAGATION DELAY VERSUS CAPACITANCE

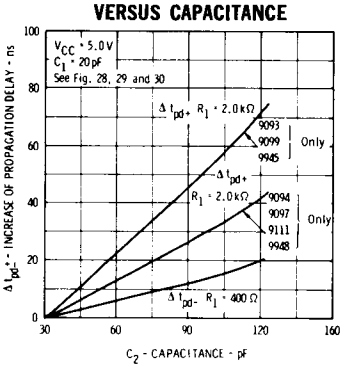


Fig. 26
DECREASE OF TURN OFF DELAY VERSUS FANOUT

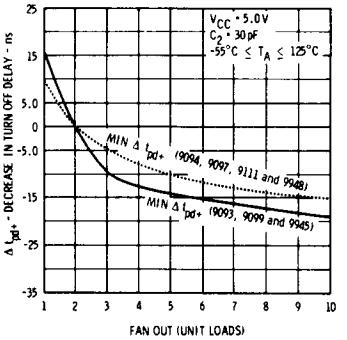
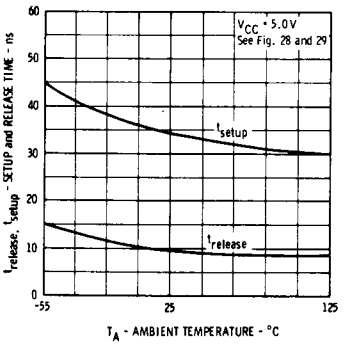


Fig. 27
WORST CASE SET UP AND RELEASE TIME VERSUS AMBIENT TEMPERATURE



SWITCHING TEST CIRCUITS, $T_A = 25°C$, $V_{CC} = 5.0$ V

Fig. 28—9945 AND 9948

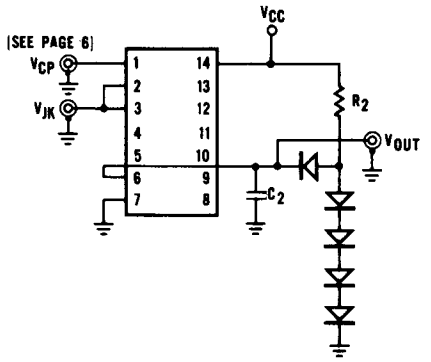


Fig. 29—9093, 9094, 9097 AND 9099

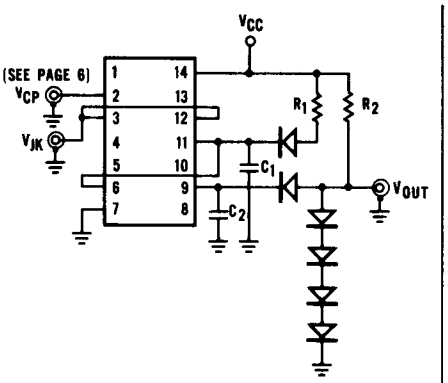


Fig. 30—9111

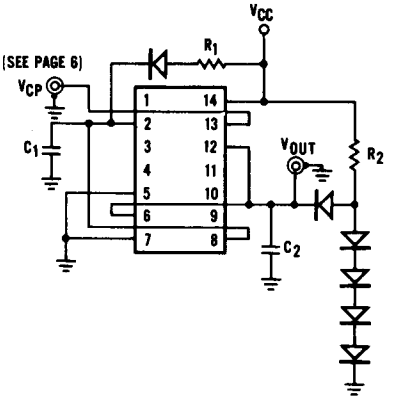


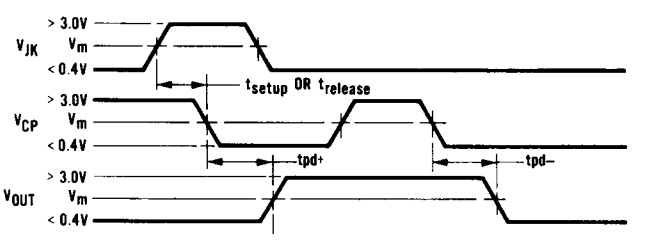
Fig. 31—WAVEFORMS

LOADS

	t_{pd+}	t_{pd-}
R_1	2.0 kΩ	2.0 kΩ
R_2	2.0 kΩ	390 Ω
C_1	20 pF	20 pF
C_2	30 pF	50 pF

MEASURING VOLTAGE THRESHOLDS (V_{in})

Temp	Vm
−55°C	1.7 V
25°C	1.5 V
125°C	1.2 V



All capacitances include probe and jig capacitance
All diodes FD600 or equivalent

SWITCHING TEST NOTES

t_{pd+} and t_{pd-}

Drive the clock pulse input with a suitable pulse source. t_{pd+} and t_{pd-} delays are defined in the waveforms Fig. 31.

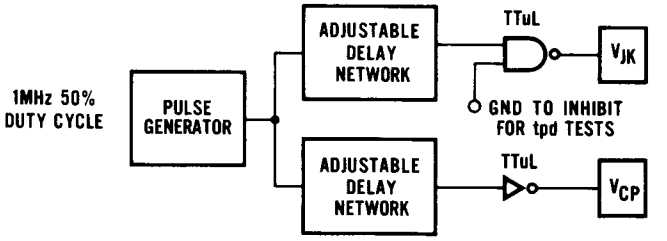
$t_{set\text{-}up}$

1. $t_{set\text{-}up}$ is defined as the minimum time required for a HIGH to be present at a synchronous logic input at any time during the high state of the clock in order for the flip-flop to respond to the data.
2. The test for $t_{set\text{-}up}$ is performed by adjusting the timing relationship between the V_{CP} and V_{JK} pulse to the $t_{set\text{-}up}$ minimum value. A device that passes the test will have the output waveform shown in Fig. 31. The output of a device that does not pass the $t_{set\text{-}up}$ test will remain at a static level (no switching will occur).

$t_{release}$

1. $t_{release}$ is defined as the maximum time allowed for a high to be present at a synchronous logic input at any time during the high state of the clock and not be recognized.
2. The test for $t_{release}$ is performed by adjusting the timing relationship between V_{CP} and V_{JK} to the $t_{release}$ maximum value. The outputs of devices that pass will remain at static logic levels. In order to check both J and K sides of the flip-flop it is necessary to perform the test with the flip-flop in each of its two possible states, i.e., set and clear. This can be accomplished by making use of the appropriate direct inputs to establish the state before a test. The outputs of devices that do not pass the $t_{release}$ test will exhibit pulses instead of static levels.

Fig. 32—RECOMMENDED INPUT PULSE SOURCES



DTμL9932 buffers with adjustable capacitors connected from extender inputs to ground make suitable delay elements.

Fig. 33—9945 AND 9948 SCHEMATIC DIAGRAM

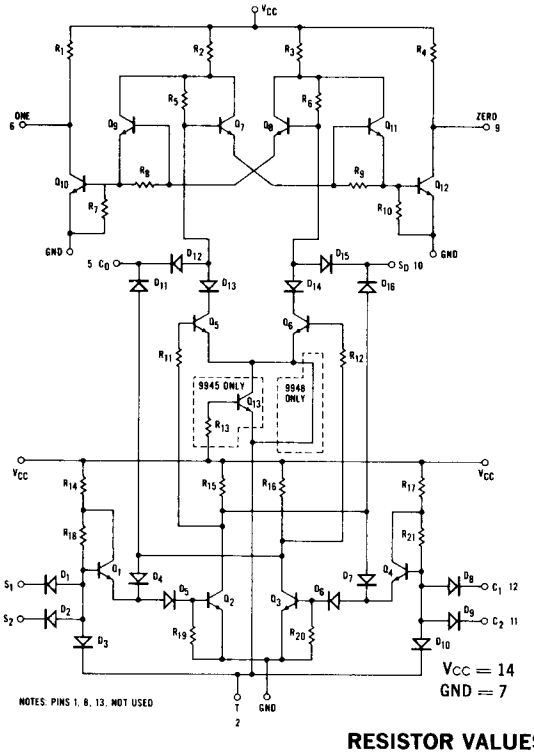
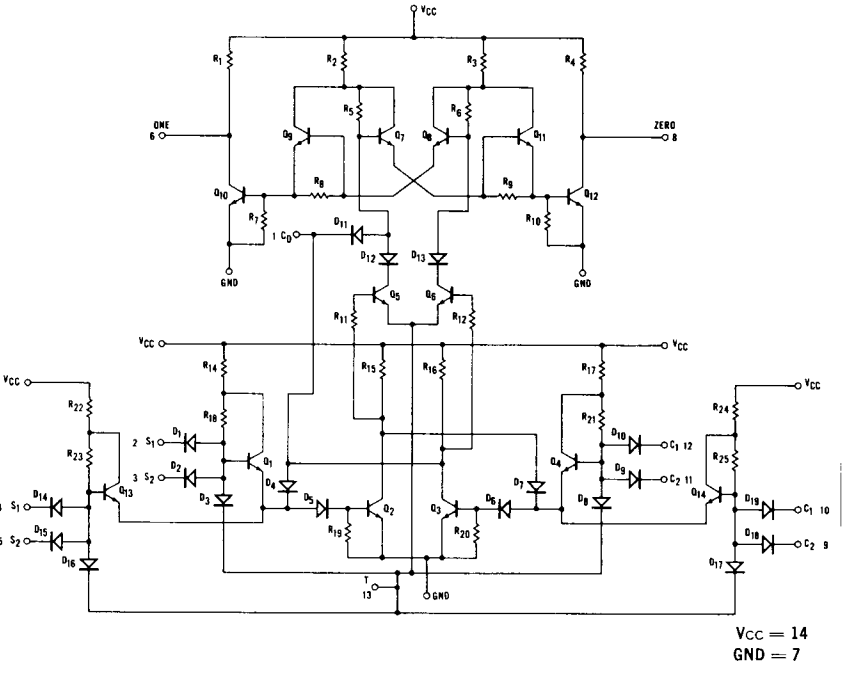


Fig. 34—9111 SCHEMATIC DIAGRAM

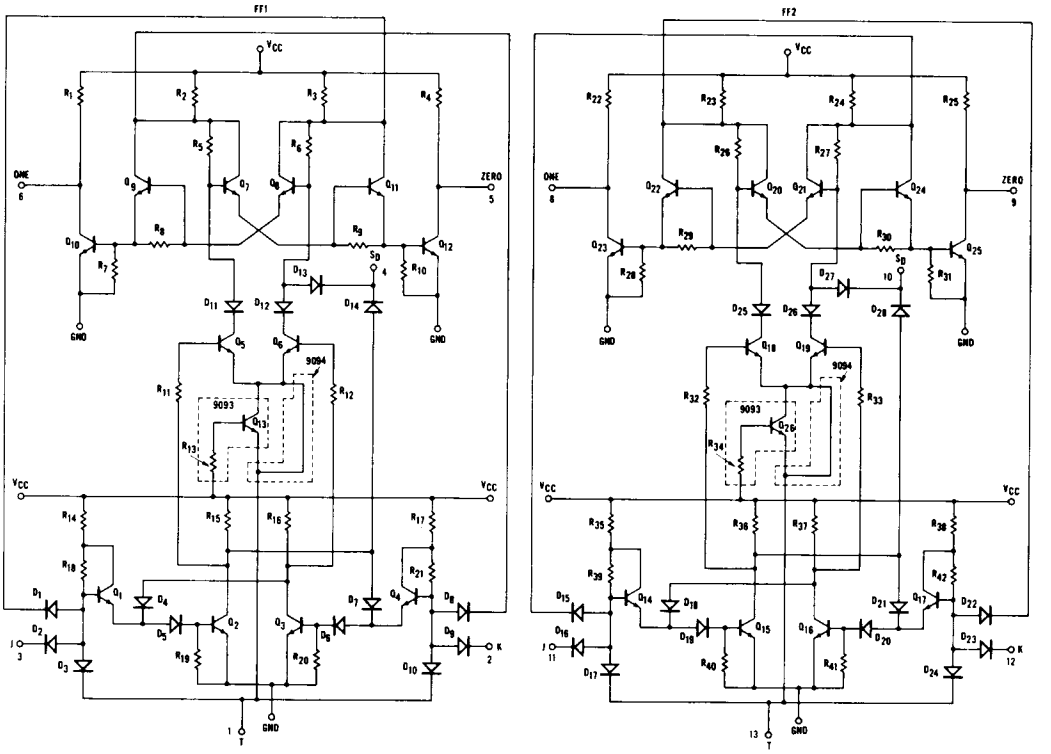


RESISTOR VALUES 9945, 9948 AND 9111

R_1, R_4 = 6.0 kΩ (9945)
= 2.0 kΩ (9948, 9111)
R_2, R_3 = 2.2 kΩ
R_5, R_6, R_{18}, R_{21}, R_{23}, R_{25} = 3.5 kΩ
R_{15}, R_{16} = 3.2 kΩ
R_7, R_{10} = 1.2 kΩ
R_8, R_9 = 3.0 kΩ
R_{11}, R_{12}, R_{19}, R_{20} = 9.0 kΩ
R_{13} = 10 kΩ
R_{14}, R_{17}, R_{22}, R_{24} = 2.5 kΩ

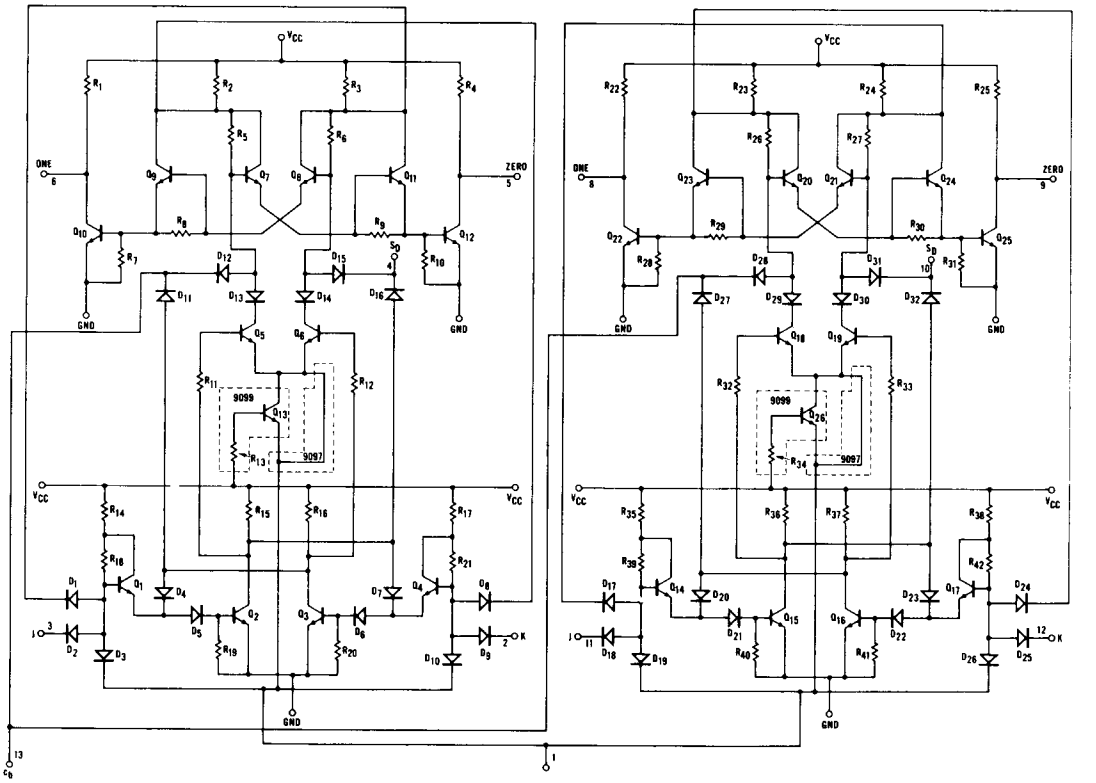
SCHEMATIC DIAGRAMS

Fig. 35—9093 AND 9094



$V_{CC} = 14$
GND = 7

Fig. 36—9097 AND 9099



$V_{CC} = 14$
GND = 7

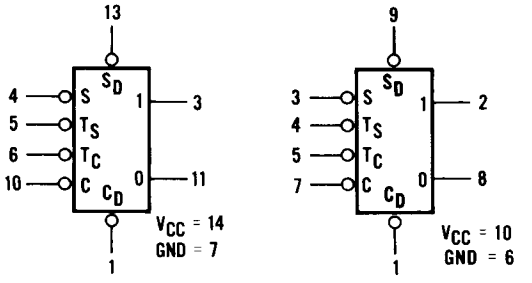
Resistor Values: 9093, 9094, 9097, 9099

R_1, R_4, R_{22}, $R_{25} = 6.0\ k\Omega$ (9093, 9099)
$= 2.0\ k\Omega$ (9094, 9097)
R_2, R_3, R_{23}, $R_{24} = 2.2\ k\Omega$
R_5, R_6, R_{18}, R_{21}, R_{26}, R_{27}, R_{39}, $R_{42} = 3.5\ k\Omega$
R_7, R_{10}, R_{28}, $R_{31} = 1.2\ k\Omega$
R_8, R_9, R_{29}, $R_{30} = 3.0\ k\Omega$
R_{11}, R_{12}, R_{19}, R_{20}, R_{32}, R_{33}, R_{40}, $R_{41} = 9.0\ k\Omega$
R_{13}, $R_{26} = 10\ k\Omega$
R_{14}, R_{17}, R_{35}, $R_{38} = 2.5\ k\Omega$
R_{15}, R_{16}, R_{36}, $R_{37} = 3.2\ k\Omega$

BINARY ELEMENT — 9950

The DTμL 9950 is an A-C coupled R-S flip-flop.

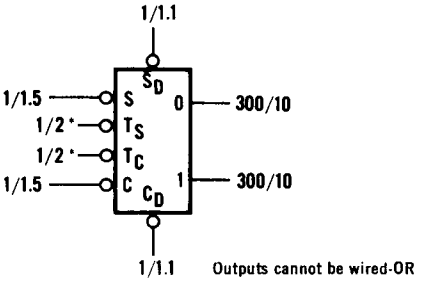
Fig. 1—LOGIC DIAGRAM AND PIN CONFIGURATION



14 PIN DIP OR FLATPACK

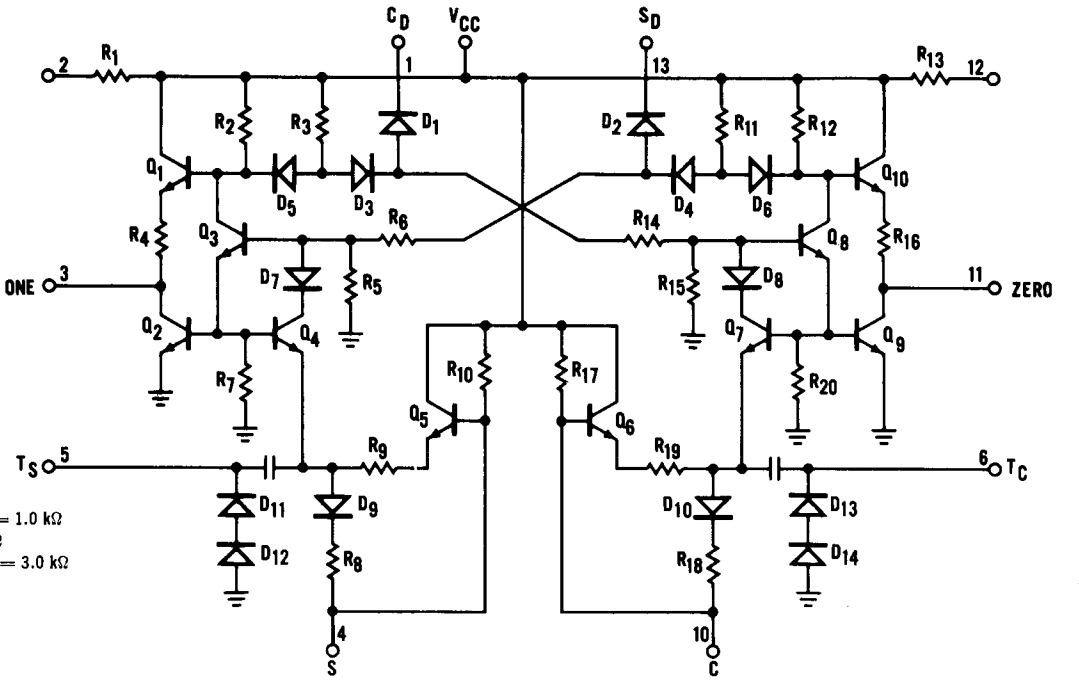
TO-100 PACKAGE

Fig. 2—LOADING RULES



* CAPACITIVE INPUTS

Fig. 3—SCHEMATIC DIAGRAM



TRUTH TABLE — TABLE I

RESPONSE TO

PULSE INPUTS						DIRECT INPUTS			
INPUTS				OUTPUTS		INPUTS		OUTPUTS	
4	5	6	10	3	11	1	13	3	11
H	X	H	X	NC	NC	H	H	NC	NC
X	H	X	H	NC	NC	L	H	L	H
L	L	X	H	H	L	H	L	H	L
L	L	H	X	H	L	L	L	H	H
H	X	L	L	L	H				
X	H	L	L	L	H				
L	L	L	L	AMBIGUOUS					

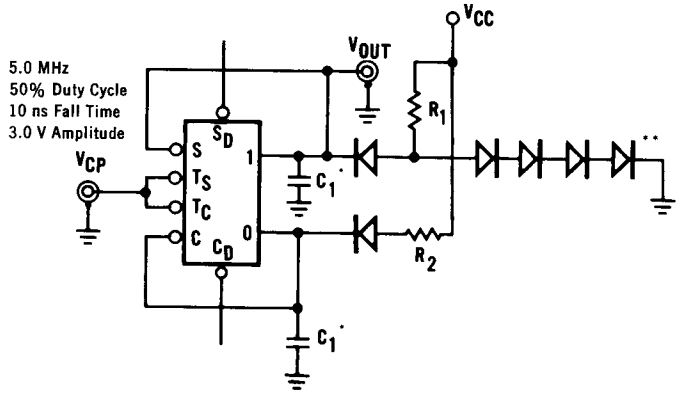
NOTES:

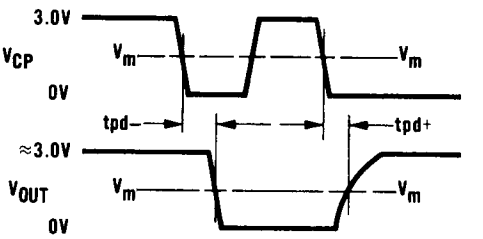
1. Abbreviations used in the body of tables:
   L = low, the more negative voltage level
   H = high, the more positive voltage level
   (in all cases, open pins have the same effect as high.)
   X = immaterial, either H or L has equal effect
   NC = no change, the trigger-pulse has no effect on outputs
2. H or L for pins 5 and 6 represent voltage transitions to the level indicated rather than the levels themselves.
3. The tables assume independent use of pulsed inputs and direct inputs. Otherwise, direct inputs will predominate.

TABLE I—
ELECTRICAL CHARACTERISTICS 9950 ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	−55°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+125°C MIN.	+125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.5		2.6			2.5		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -1.5\ mA$
V_{OL}	Output Low Voltage		0.4			0.4		0.4	Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 12\ mA$ $V_{CC} = 5.5\ V$, $I_{OL} = 15\ mA$
V_{IHS}	Asynchronous Input High Voltage	2.1		1.9			1.7		Volts	Guaranteed high threshold for asynchronous inputs
V_{ILS}	Asynchronous Input Low Voltage		.95			.80		.605	Volts	Guaranteed low threshold for asynchronous inputs
I_R	Input Leakage					2.0		5.0	μA	$V_{CC} = 5.5\ V$, $V_R = 4.0\ V$ Asynchronous inputs only
I_F	Input Load Current		−2.22			−2.22		−2.09	mA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$
I_F	Input Load Current		−1.83			−1.83		−1.71	mA	$V_{CC} = 4.5\ V$, $V_F = 0.4\ V$
I_{FSI}	Asynchronous Input Load Current		−1.64			−1.64		−1.46	mA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$
I_{FSI}	Asynchronous Input Load Current		−1.20			−1.24		−1.14	mA	$V_{CC} = 4.5\ V$, $V_F = 0.4\ V$
I_{PD}	V_{CC} Current		8.7		6.7	8.7		8.7	mA	$V_{CC} = 5.0\ V$, Input 4 gnd.
t_{pd+}	Turn Off Delay					30			ns	$V_{CC} = 5.0\ V$
t_{pd-}	Turn On Delay					30			ns	See Fig. 4
	Toggling Frequency			20					MHz	

Fig. 4—t_{pd} TEST CIRCUIT





* Includes probe and jig capacitance
** All diodes FD600 or equivalent

$V_m = 1.5\ V$ @ 25°C
$= 1.2\ V$ @ 125°C
$= 1.7\ V$ @ −55°C

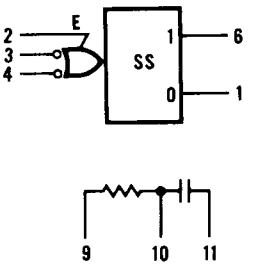
	R_1	R_2	C_1
t_{pd+}	3.9 kΩ	2.0 kΩ	100 pF
t_{pd-}	390Ω	2.0 kΩ	100 pF
20 MHz toggle	∞	∞	5.0 pF

MONOSTABLE MULTIVIBRATORS — 9941, 9951

The DTμL 9941 and 9951 are monostable multivibrators designed for use with other members of the DTμL family. They provide complementary output pulses which are typically 100 ns wide. This pulse width is adjustable by the addition of external components.

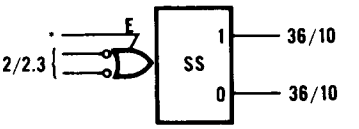
The TTμL 9601 is a retriggerable one shot having several features which are superior to the 9941 and 9951. It is therefore recommended for new system designs in preference to the 9941 or 9951.

Fig. 1—LOGIC DIAGRAM AND PIN CONFIGURATION



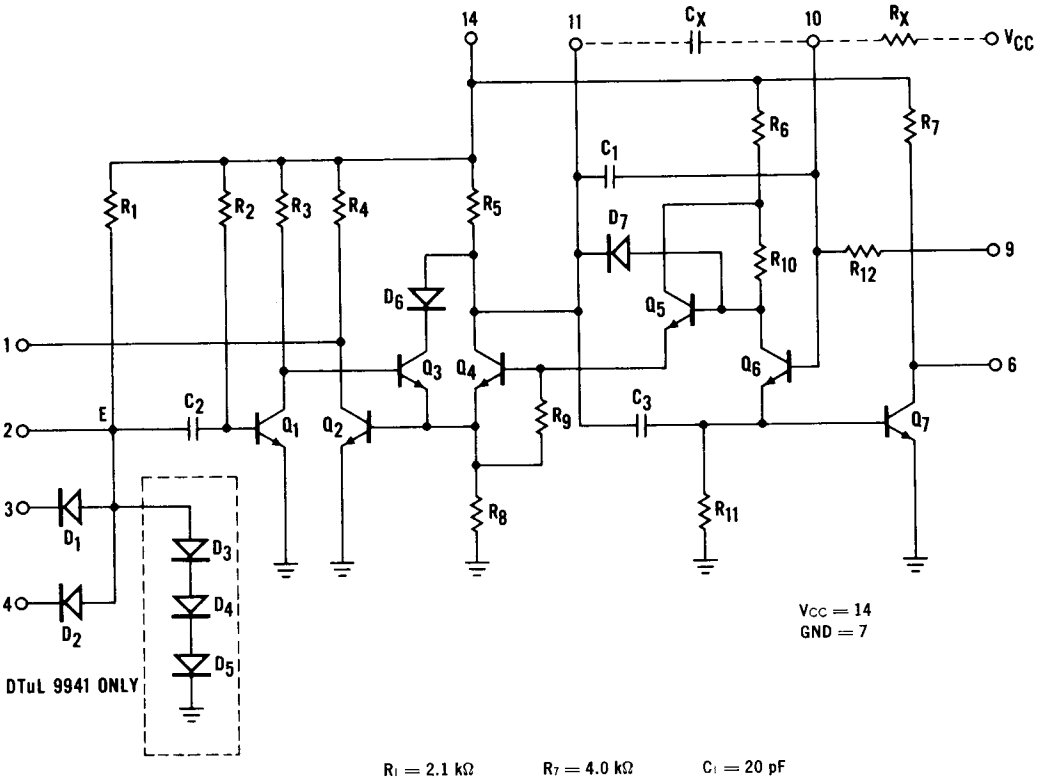
$V_{CC} = 14$
GND = 7

Fig. 2—LOADING FACTORS



1. Outputs can be wire "AND"ed
2. Extender pin allows increased number of inputs by addition of discrete diodes or extender element DTμL9933.

Fig. 3—SCHEMATIC DIAGRAM



$R_1 = 2.1\ k\Omega$
$R_2 = 7.0\ k\Omega$
$R_3 = 2.4\ k\Omega$
$R_4 = 4.0\ k\Omega$
$R_5 = 2.0\ k\Omega$
$R_6, R_{10} = 1.8\ k\Omega$
$R_7 = 4.0\ k\Omega$
$R_8 = 1.2\ k\Omega$
$R_9 = 3.6\ k\Omega$
$R_{11} = 24\ k\Omega$
$R_{12} = 9.0\ k\Omega$
$C_1 = 20$ pF
$C_2 = 25$ pF
$C_3 = 15$ pF

TABLE I

ELECTRICAL CHARACTERISTICS — 9941 AND 9951 ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

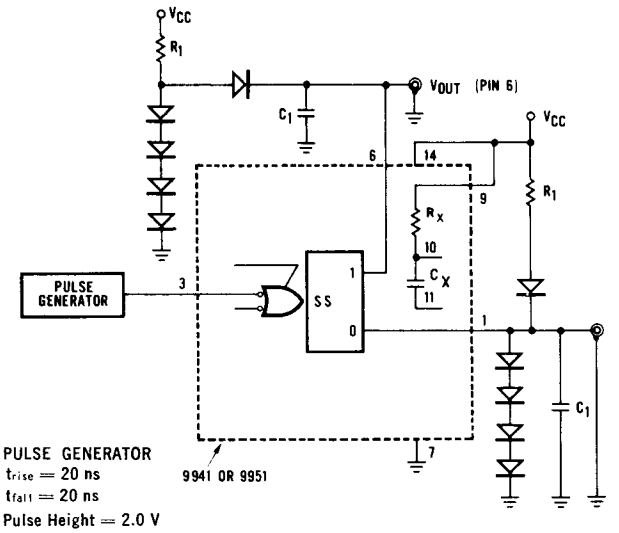
SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.5		2.5			2.5		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -0.18\ mA$
V_{OL}	Output Low Voltage		0.4			0.4		0.4	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 15\ mA$ $V_{CC} = 4.5\ V$, $I_{OL} = 15\ mA$
I_{PDL}	Power Dissipation Current with Inputs Grounded				7.2	9.0			mA	$V_{CC} = 5.0\ V$, Inputs = Gnd.
I_F	Input Load Current		−2.93			−2.93		−2.75	mA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$
			−2.26			−2.26		−2.22	mA	$V_{CC} = 4.5\ V$, $V_F = 0.4\ V$
I_R	Input Leakage Current		5.0			5.0		10.0	μA	$V_{CC} = 5.5\ V$, $V_R = 4.0\ V$, Pin 2 = Gnd.
t_{pd+}	Turn Off Delay					40			ns	Pin 6 — $V_{CC} = 5.0\ V$
t_{pd-}	Turn On Delay					40			ns	Pin 1 — See Figs. 4 & 5 on Page 23
PW	Pulse Width									
	9941			90		330				Pin 1
				70		330				Pin 6
	9951			90		220				Pin 1
				70		160				Pin 6

RULES FOR USE OF 9951

1. With Pin 9 connected to V_{CC} and no external capacitor (C_X), the output pulse width is approximately 100 ns.
2. With Pin 9 connected to V_{CC} and an external capacitor (C_X) connected between Pins 10 and 11, the output pulse width (T) is: $T \approx 4.5\ (C_X + 20)$ with C_X in pF and T in ns.
3. For improved pulse width control, Pin 9 is left open and a stable external resistor (R_X) of 9.0 kΩ minimum to 15 kΩ maximum is connected from Pin 10 to V_{CC}. The output pulse width is given by the expression: $T \approx 0.5\ R_X\ (C_X + 20)$ with R_X in kΩ, C_X in pF and T in ns.
4. The output duty cycle (pulse width/period) should not exceed 40%. It may be increased to 50% by adding a 2.0 kΩ resistor between Pin 11 and V_{CC}. Higher duty cycles are obtainable but the output pulse width and performance are less predictable.
5. The maximum input fall time to trigger: 25 ns for a 1.0 volt swing; 50 ns for a 2.0 volt swing; 100 ns for a 4.0 volt swing.
6. The minimum pulse width at output Pin 1 is approximately 100 ns. This pulse width may be decreased to 50 ns by connecting a 10 kΩ resistor between Pin 5 and V_{CC}. (not applicable to TO-100 package.)
7. For pulse widths greater than 1.0 μs, Pin 1 should be used as the output and inverted if required.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

Fig. 4

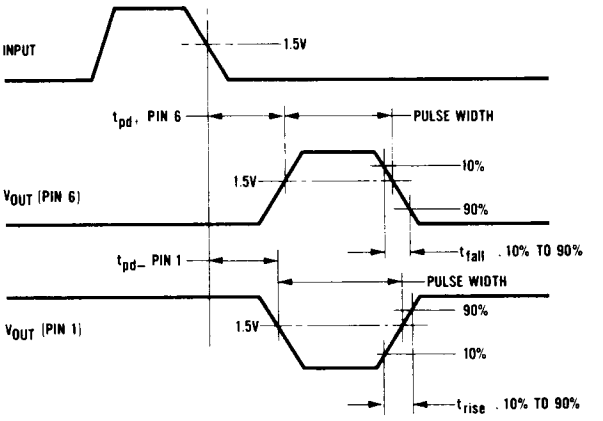


PULSE GENERATOR
t_{rise} = 20 ns
t_{fall} = 20 ns
Pulse Height = 2.0 V
Pulse Width = 200 ns
Frequency = 1.0 MHz
Capacitance includes probe and jig
All Diodes FD100

9941 OR 9951

C_l = 50 pF
R_l = 330Ω

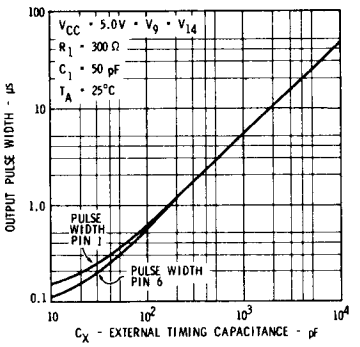
Fig. 5



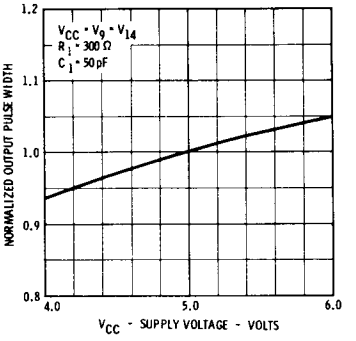
9941 AND 9951 TIMING CHARACTERISTICS

(Test circuit above is used with appropriate modifications where necessary)

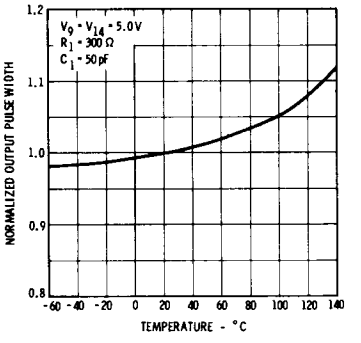
OUTPUT PULSE WIDTH VERSUS EXTERNAL TIMING CAPACITANCE C_X



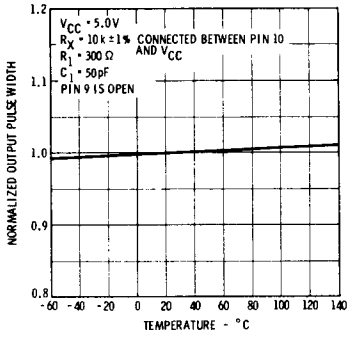
NORMALIZED OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE



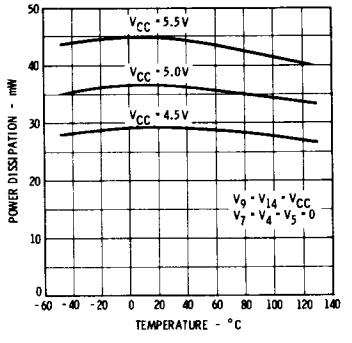
NORMALIZED OUTPUT PULSE WIDTH VERSUS TEMPERATURE



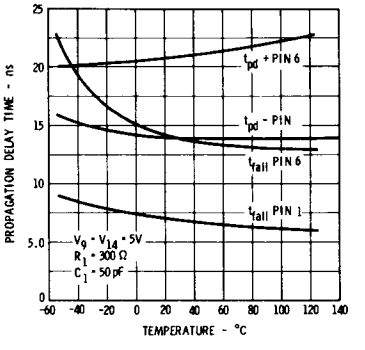
NORMALIZED OUTPUT PULSE WIDTH VERSUS TEMPERATURE USING EXTERNAL TIMING RESISTOR R_X



TYPICAL POWER DISSIPATION VERSUS TEMPERATURE

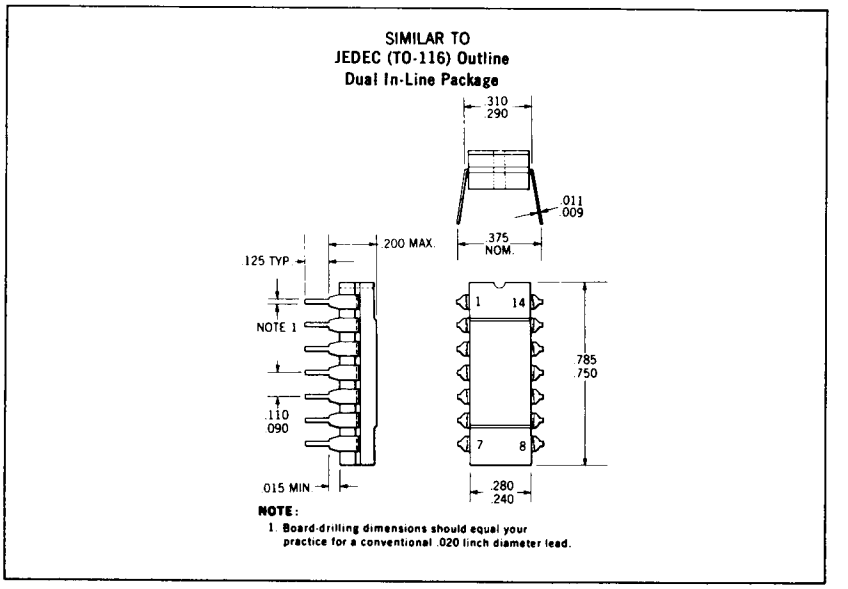


SWITCHING TIMES VERSUS TEMPERATURE

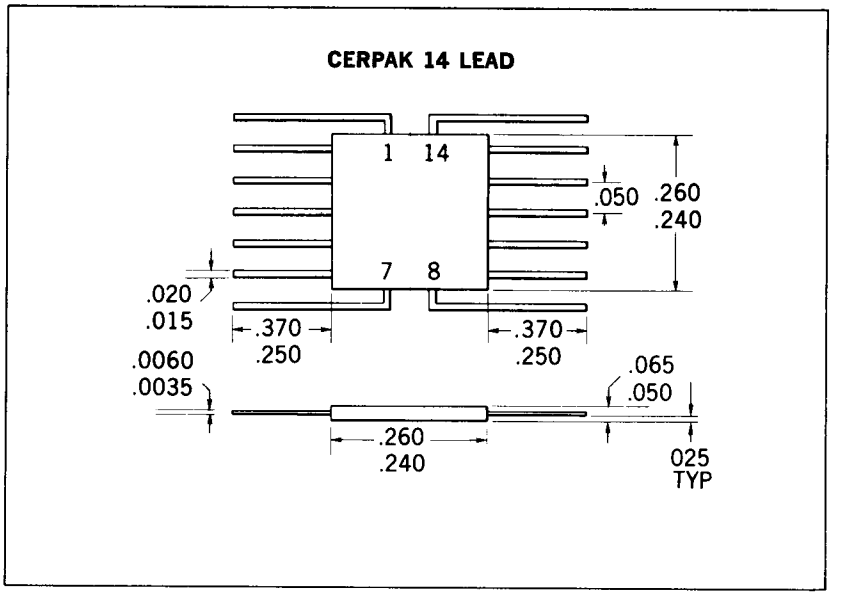


PACKAGE OUTLINES

U6A



U3I



ORDER INFORMATION

To order diode-transistor micrologic elements specify U3IXXXX51X for 14 pin Flat package; U6AXXXX51X for 14 pin Dual In-Line package where XXXX is the four-digit number denoting the specific element desired and 51X is for −55°C to + 125°C.