

### ● General Description

The AGM15P30AS combines advanced trench MOSFET technology with a low resistance package to provide extremely low  $R_{DS(ON)}$

This device is ideal for load switch and battery protection applications.

### ● Features

- Advance high cell density Trench technology
- Low  $R_{DS(ON)}$  to minimize conductive loss
- Low Gate Charge for fast switching
- Low Thermal resistance
- 100% Avalanche tested
- 100% DVDS tested

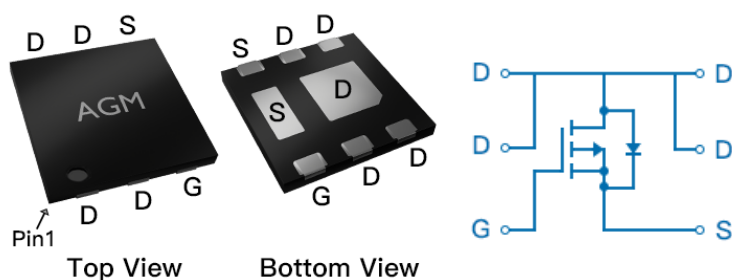
### ● Application

- MB/VGA Vcore
- SMPS 2<sup>nd</sup> Synchronous Rectifier
- POL application
- BLDC Motor driver

### Product Summary

BVDSS	RDSON	ID
-15V	29mΩ	-5A

### DFN2\*2 Pin Configuration



### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
AGM15P30	AGM15P30AS	DFN2*2	178mm	8mm	3000

Table 1. Absolute Maximum Ratings (TA=25°C)

Symbol	Parameter	Value	Unit
VDS	Drain-Source Voltage (VGS=0V)	-15	V
VGS	Gate-Source Voltage (VDS=0V)	±10	V
ID	Drain Current-Continuous(Tc=25°C) <b>(Note 1)</b>	-5.0	A
	Drain Current-Continuous(Tc=100°C)	-3.4	A
IDM (pluse)	Drain Current-Pulsed <b>(Note 2)</b>	-20	A
PD	Maximum Power Dissipation(Tc=25°C)	1.0	w
	Maximum Power Dissipation(Tc=100°C)	0.4	w
EAS	Avalanche energy <b>(Note 3)</b>	---	mJ
TJ,TSTG	Operating Junction and Storage Temperature Range	-55 To 150	°C

Table 2. Thermal Characteristic

Symbol	Parameter	Typ	Max	Unit
RθJA	Thermal Resistance Junction-ambient (Steady State) <sup>1</sup>	---	125	°C/W

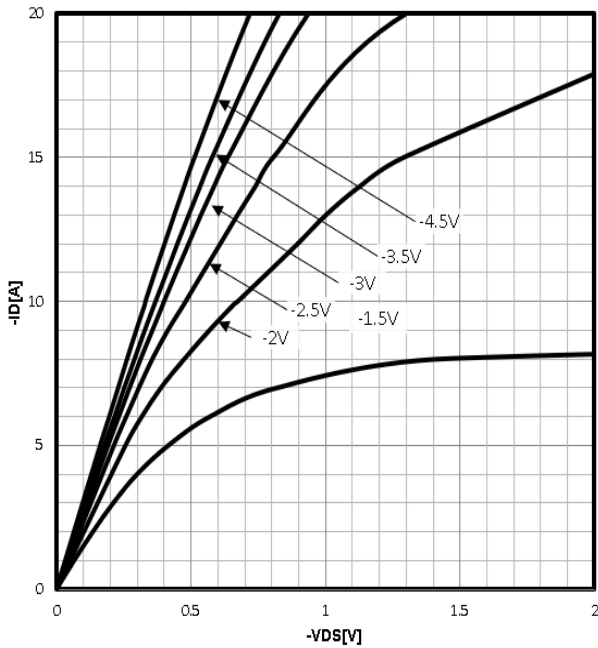
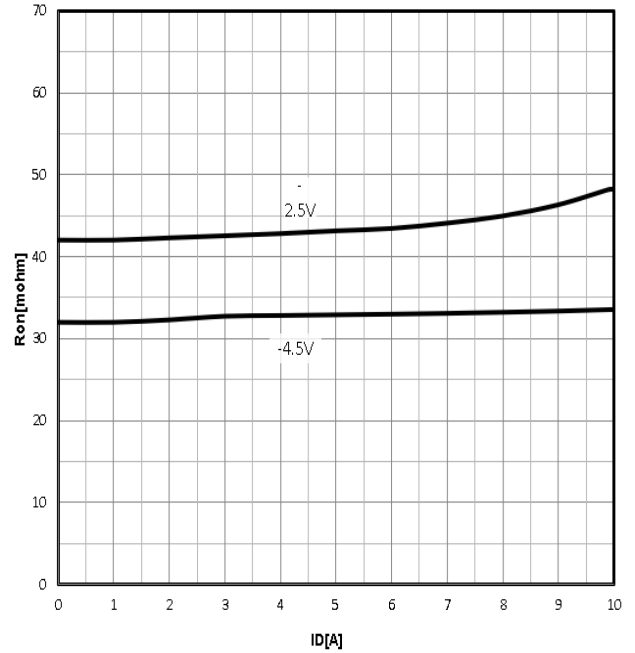
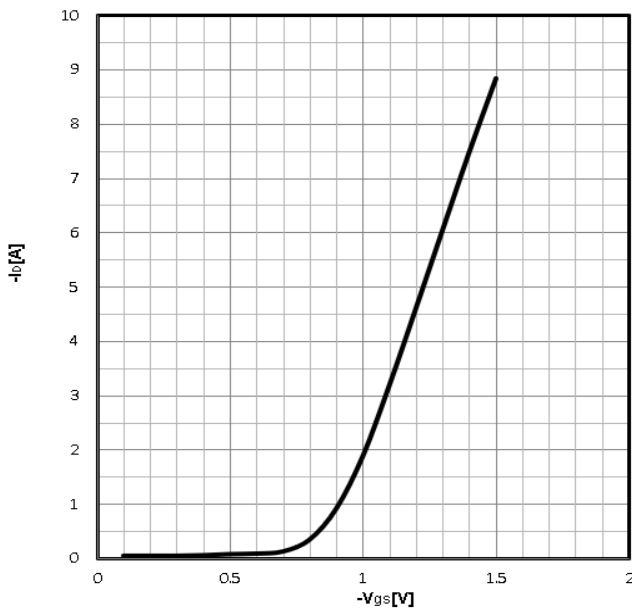
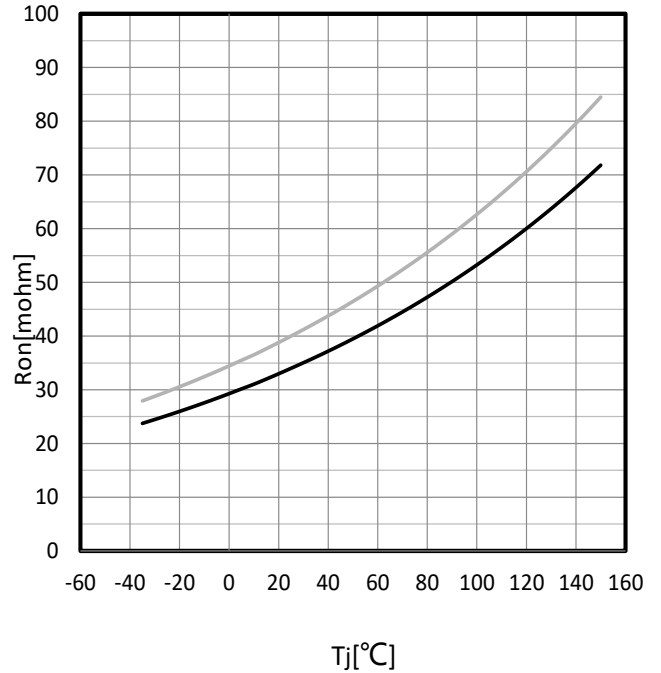
**Table 3. Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>On/Off States</b>						
BVDSS	Drain-Source Breakdown Voltage	VGS=0V ID=-250μA	-15	-18	--	V
IDSS	Zero Gate Voltage Drain Current	VDS=-15V,VGS=0V	--	--	-1	μA
IGSS	Gate-Body Leakage Current	VGS=±10V,VDS=0V	--	--	±100	nA
VGS(th)	Gate Threshold Voltage	VDS=VGS,ID=-250μA	-0.4	-0.6	-1.0	V
gFS	Forward Transconductance	VDS=-5V,ID=-3A	--	5	--	S
RDS(on)	Drain-Source On-State Resistance	VGS=-4.5V, ID=-3.5A	--	29	40	mΩ
		VGS=-2.5V, ID=-3A	--	38.5	50	mΩ
<b>Dynamic Characteristics</b>						
Ciss	Input Capacitance	VDS=-10V,VGS=0V, F=1MHZ	--	418	--	pF
Coss	Output Capacitance		--	93	--	pF
Crss	Reverse Transfer Capacitance		--	86	--	pF
Rg	Gate resistance	f=1.0MHz	--	13	--	Ω
<b>Switching Times</b>						
td(on)	Turn-on Delay Time	ID =-3.3A VDS = -10V VGS =-4.5V RG = 10Ω	--	12	--	nS
tr	Turn-on Rise Time		--	32	--	nS
td(off)	Turn-Off Delay Time		--	30	--	nS
tf	Turn-Off Fall Time		--	11	--	nS
Qg	Total Gate Charge	VGS=-10V, VDS=-10V, ID=-3.3A	--	12	--	nC
Qgs	Gate-Source Charge		--	0.7	--	nC
Qgd	Gate-Drain Charge		--	1.6	--	nC
<b>Source-Drain Diode Characteristics</b>						
ISD	Source-Drain Current(Body Diode)		--	--	-5.0	A
VSD	Forward on Voltage	VGS=0V,IS=-3.5A	--	--	-1.2	V
trr	Reverse Recovery Time	Isd=-3.5A , di/dt=100A/μs , TJ=25°C	--	--	--	ns
Qrr	Reverse Recovery Charge		--	--	--	nc

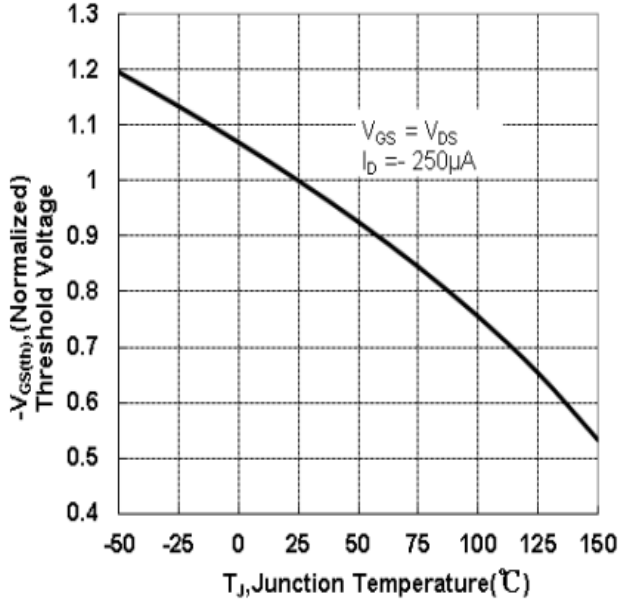
Notes 1.The maximum current rating is package limited.

Notes 2.Repetitive Rating: Pulse width limited by maximum junction temperature

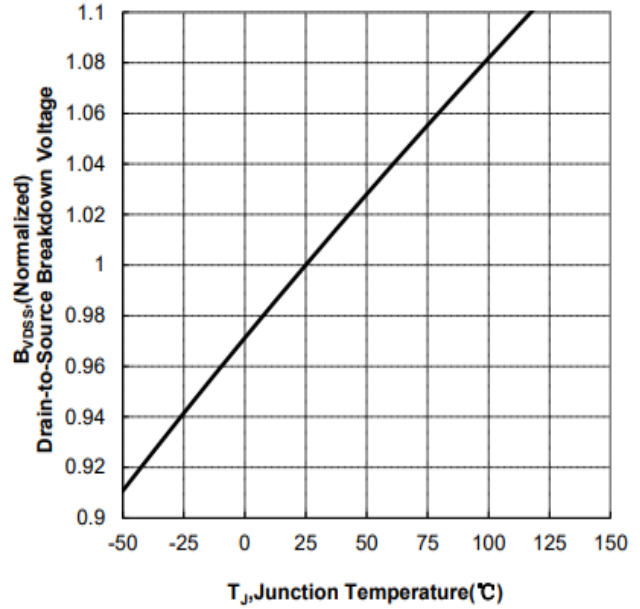
Notes 3.EAS condition: T<sub>J</sub>=25°C

**Characteristics Curve:**
**Typ. output characteristics**  
 $I_D = f(V_{DS})$ 

**Typ. drain-source on resistance**  
 $R_{DS(on)} = f(I_D)$ 

**Typ. transfer characteristics**  
 $I_D = f(V_{GS})$ 

**Drain-source on-state resistance**  
 $R_{DS(on)} = f(T_j); I_D = -3.5A$ 


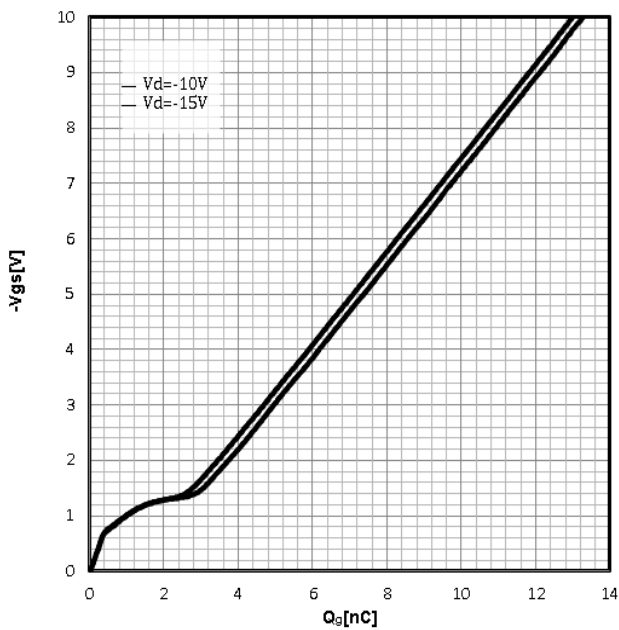
**Gate Threshold Voltage**  
 $-V_{TH}=f(T_j); I_D=-250\mu A$



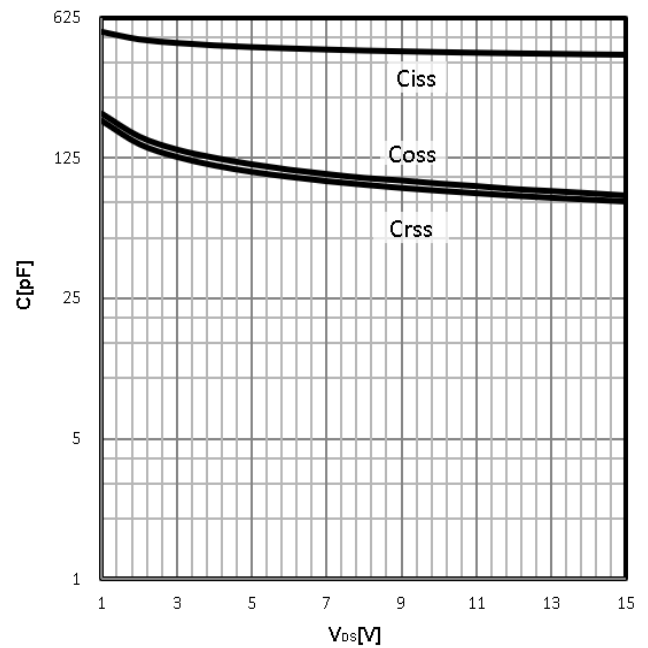
**Drain-source breakdown voltage**  
 $V_{BR(DSS)}=f(T_j); I_D=-250\mu A$



**Typ. gate charge**  
 $V_{GS}=f(Q_g); I_D=-3.3A$

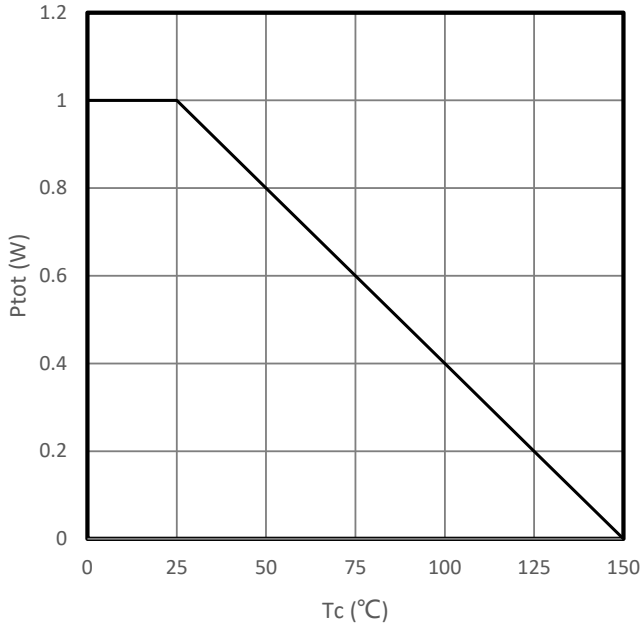


**Typ. capacitances**  
 $C=f(V_{DS}); V_{GS}=0V; f=1MHz$

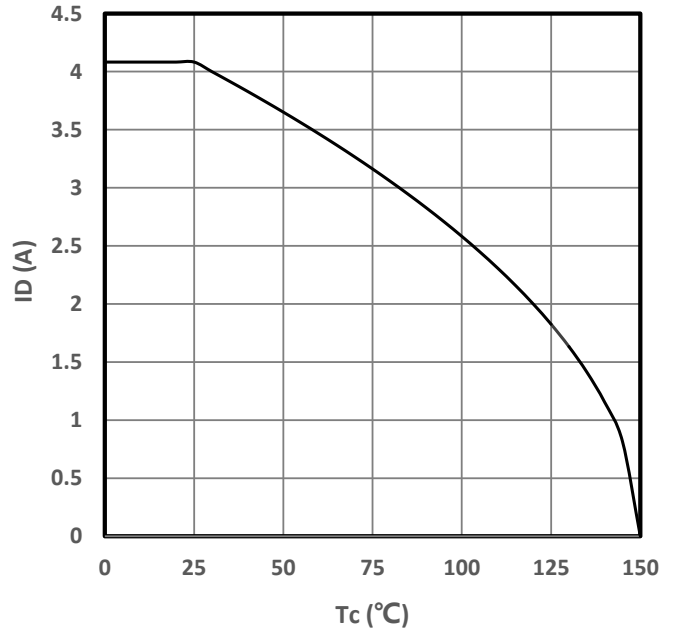


**Power Dissipation**

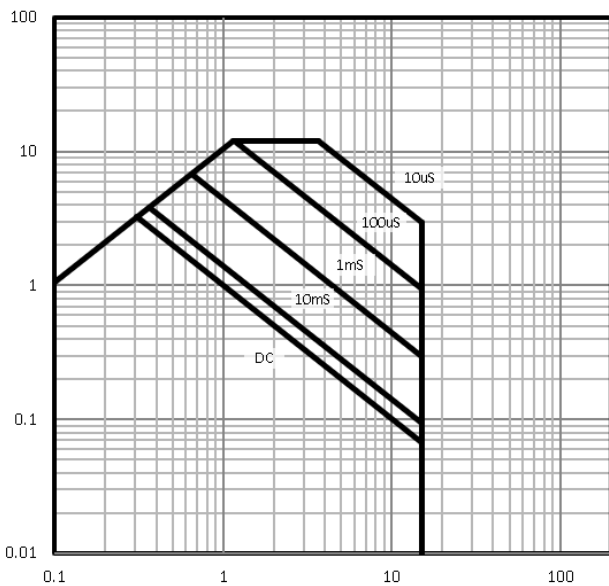
$$P_{tot}=f(T_C)$$


**Maximum Drain Current**

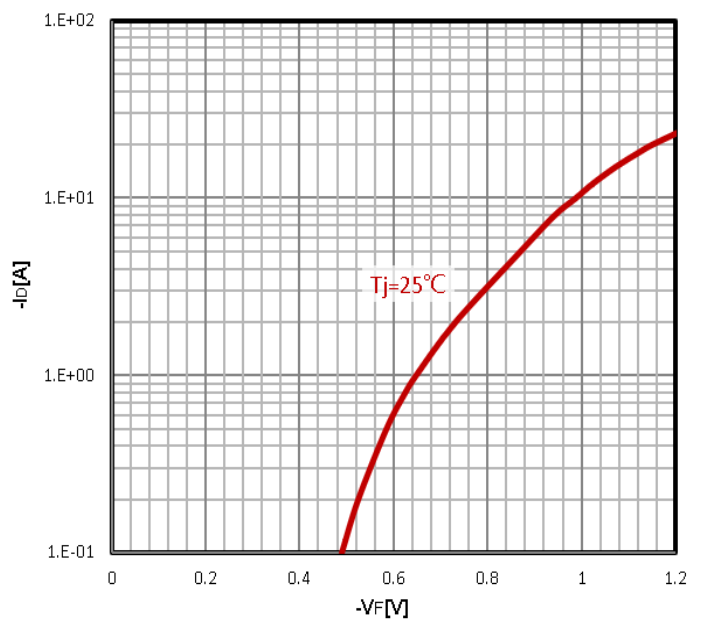
$$-I_D=f(T_C)$$


**Safe operating area**

$$-I_D=f(-V_{DS})$$

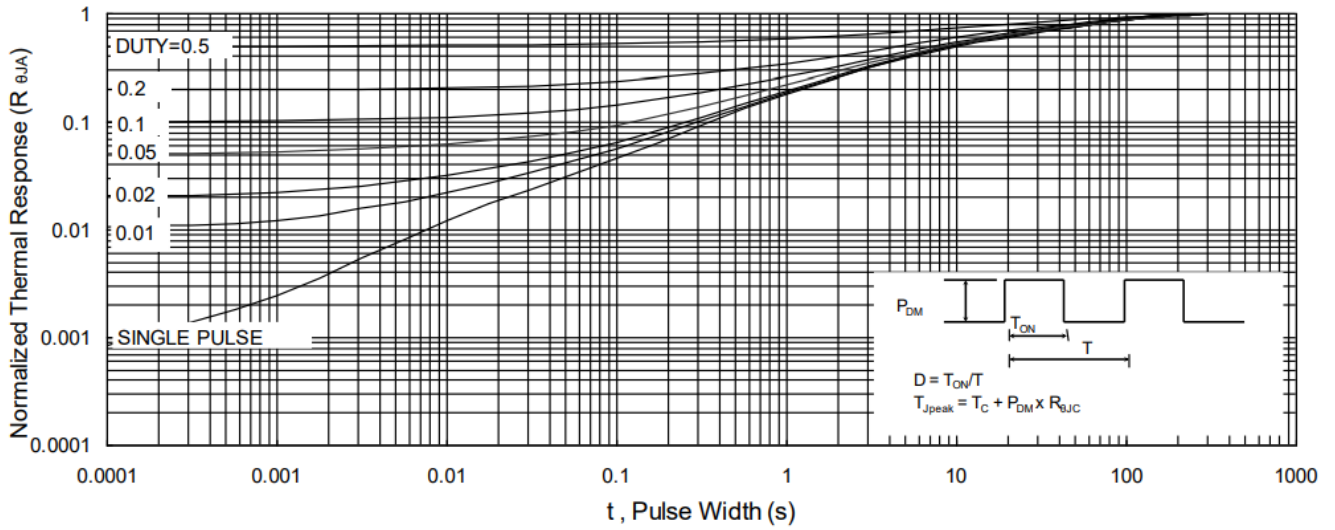

**Body Diode Forward Voltage Variation**

$$-I_F=f(-V_{GS})$$

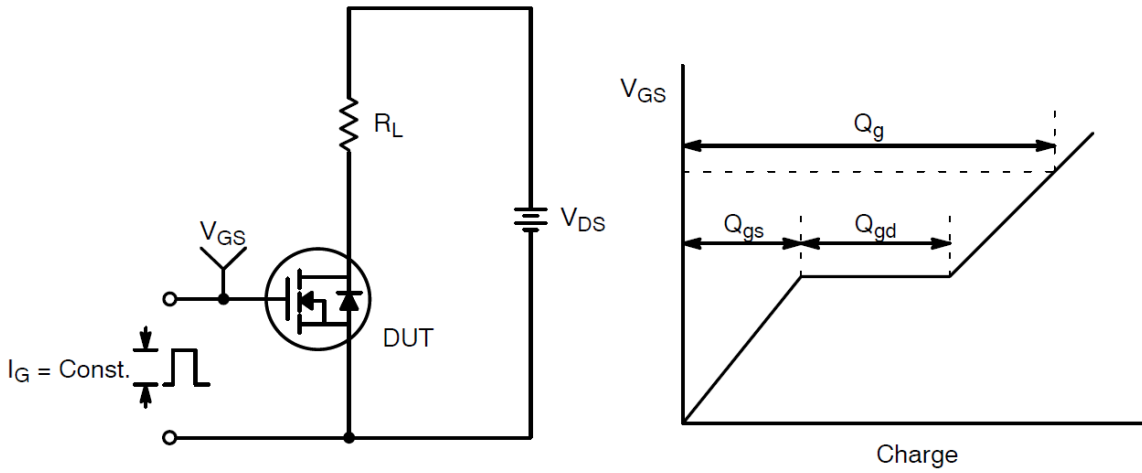


### Max. transient thermal impedance

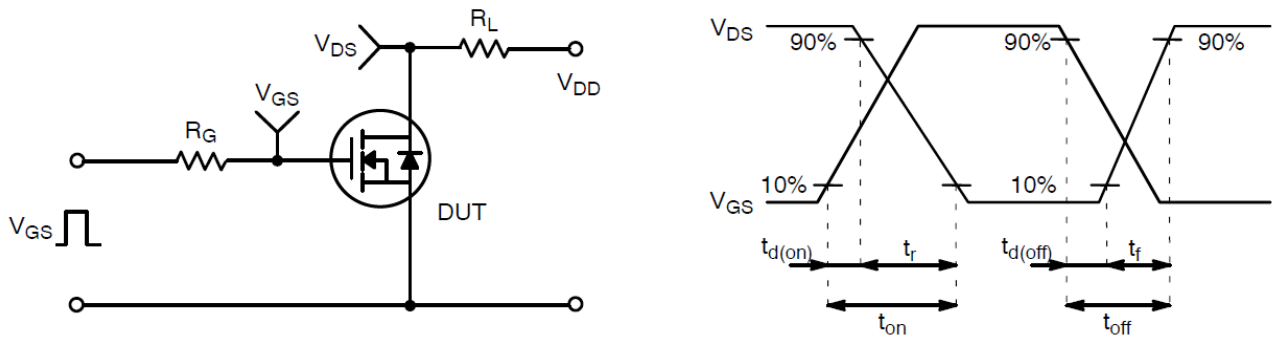
$$Z_{thJC} = f(t_p)$$



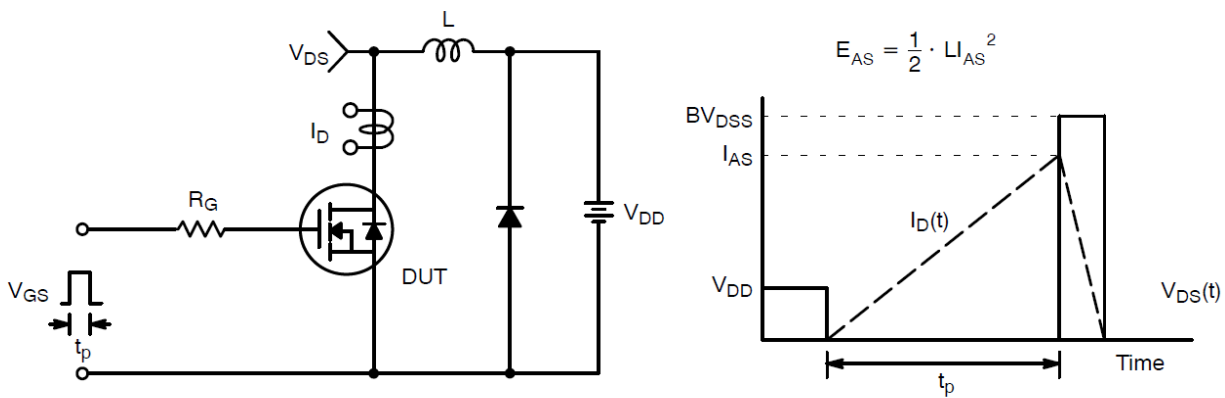
### Test Circuit and Waveform:



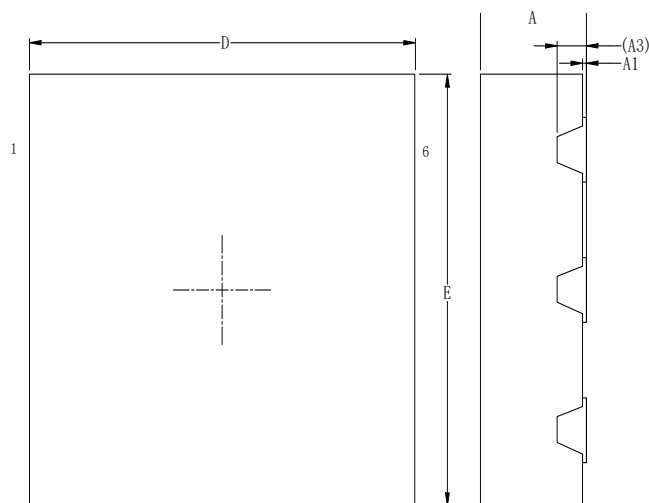
**Gate Charge Test Circuit & Waveform**

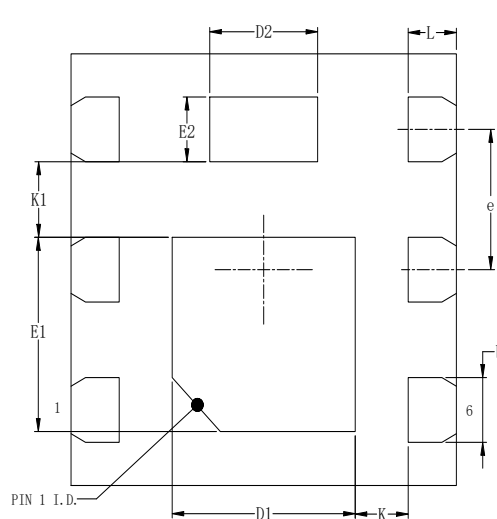


**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching Test Circuit & Waveforms**

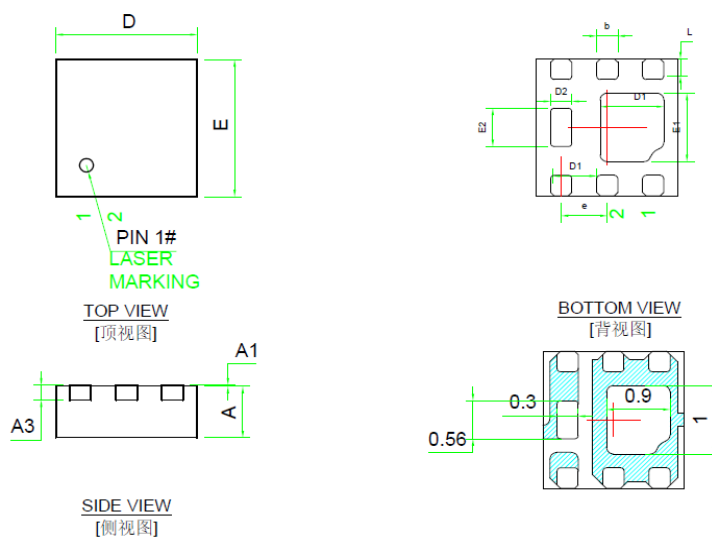
**●Dimensions (DFN2×2)**

 TOP VIEW  
[顶视图]

 SIDE VIEW  
[侧视图]


BOTTOM VIEW

[背视图]

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.5	0.55	0.6
STAND OFF		A1	0	0.02	0.05
L/F THICKNESS		A3	0.152 REF		
LEAD WIDTH		b	0.25	0.3	0.35
BODY SIZE	X	D	1.9	2	2.1
	Y	E	1.9	2	2.1
LEAD PITCH		e	0.65 BSC		
EP SIZE	X	D1	0.85	0.95	1.05
		D2	0.46	0.56	0.66
	Y	E1	0.8	0.9	1
		E2	0.2	0.3	0.4
LEAD LENGTH		L	0.2	0.25	0.3
LEAD TIP TO EP EDGE		K	0.275 REF		
EP EDGE TO EP EDGE		K1	0.35 REF		


 TOP VIEW  
[顶视图]

 BOTTOM VIEW  
[背视图]

 SIDE VIEW  
[侧视图]

Symbol	Dimensions In Millimeters		
	Min	Nom	Max
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
A3	0.203REF		
b	0.250	0.300	0.350
D	1.900	2.000	2.100
D1	0.850	0.900	0.950
D2	0.250	0.300	0.350
e	0.650BSC		
E	1.900	2.000	2.100
E1	0.950	1.000	1.050
E2	0.510	0.560	0.610
L	0.250	0.300	0.350




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