

● General Description

The AGM15P16AS combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$

This device is ideal for load switch and battery protection applications.

● Features

- Advance high cell density Trench technology
- Low $R_{DS(ON)}$ to minimize conductive loss
- Low Gate Charge for fast switching
- Low Thermal resistance
- 100% Avalanche tested
- 100% DVDS tested

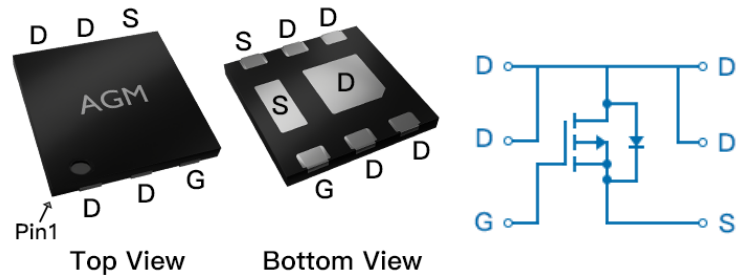
● Application

- MB/VGA Vcore
- SMPS 2nd Synchronous Rectifier
- POL application
- BLDC Motor driver

Product Summary

BVDSS	RDS(ON)	ID
-15V	13mΩ	-7.5A

DFN2*2 Pin Configuration



Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
15P16	AGM15P16AS	DFN2*2	178mm	8mm	3000

Table 1. Absolute Maximum Ratings (TA=25°C)

Symbol	Parameter	Value	Unit
VDS	Drain-Source Voltage (VGS=0V)	-15	V
VGS	Gate-Source Voltage (VDS=0V)	±10	V
ID	Drain Current-Continuous(Tc=25°C) (Note 1)	-7.5	A
	Drain Current-Continuous(Tc=100°C)	-5.0	A
IDM (pluse)	Drain Current-Pulsed (Note 2)	-30	A
PD	Maximum Power Dissipation(Tc=25°C)	1.8	w
	Maximum Power Dissipation(Tc=100°C)	0.7	w
EAS	Avalanche energy (Note 3)	---	mJ
TJ,TSTG	Operating Junction and Storage Temperature Range	-55 To 150	°C

Table 2. Thermal Characteristic

Symbol	Parameter	Typ	Max	Unit
RθJA	Thermal Resistance Junction-ambient (Steady State) ¹	---	69	°C/W

Table 3. Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On/Off States						
BVDSS	Drain-Source Breakdown Voltage	V _{GS} =0V I _D =-250μA	-15	-18	--	V
IDSS	Zero Gate Voltage Drain Current	V _{DS} =-15V, V _{GS} =0V	--	--	-1	μA
IGSS	Gate-Body Leakage Current	V _{GS} =±10V, V _{DS} =0V	--	--	±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-0.4	-0.6	-1.0	V
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-3A	--	5	--	S
R _{DS(on)}	Drain-Source On-State Resistance	V _{GS} =-4.5V, I _D =-4A	--	13	19	mΩ
		V _{GS} =-2.5V, I _D =-3A	--	18	28	mΩ
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} =-10V, V _{GS} =0V, F=1MHZ	--	1024	--	pF
C _{oss}	Output Capacitance		--	192	--	pF
C _{rss}	Reverse Transfer Capacitance		--	177	--	pF
R _g	Gate resistance	f=1.0MHz	--	12	--	Ω
Switching Times						
t _{d(on)}	Turn-on Delay Time	I _D = -1A V _{DS} = -10V V _{GS} = -4.5V R _G = 10Ω	--	10	--	nS
t _r	Turn-on Rise Time		--	35	--	nS
t _{d(off)}	Turn-Off Delay Time		--	40	--	nS
t _f	Turn-Off Fall Time		--	7.0	--	nS
Q _g	Total Gate Charge	V _{GS} =-10V, V _{DS} =-10V, I _D =-4A	--	25	--	nC
Q _{gs}	Gate-Source Charge		--	1.2	--	nC
Q _{gd}	Gate-Drain Charge		--	3.5	--	nC
Source-Drain Diode Characteristics						
I _{SD}	Source-Drain Current(Body Diode)		--	--	-7.5	A
V _{SD}	Forward on Voltage	V _{GS} =0V, I _S =-4A	--	--	-1.2	V
t _{rr}	Reverse Recovery Time	I _{sd} =-4A , di/dt=100A/μs , T _J =25°C	--	--	--	ns
Q _{rr}	Reverse Recovery Charge		--	--	--	nc

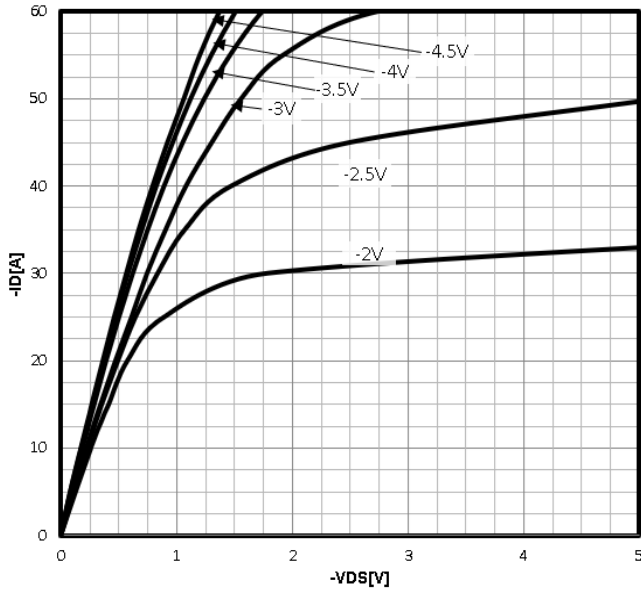
Notes 1.The maximum current rating is package limited.

Notes 2.Repetitive Rating: Pulse width limited by maximum junction temperature

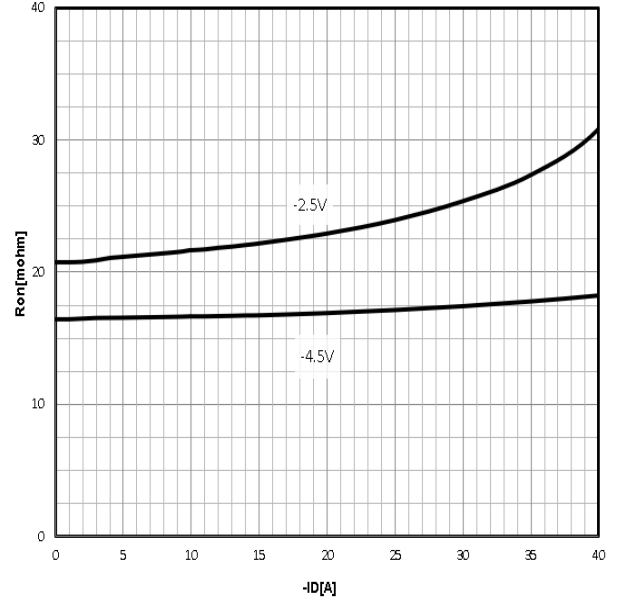
Notes 3.EAS condition: T_J=25°C

Characteristics Curve:

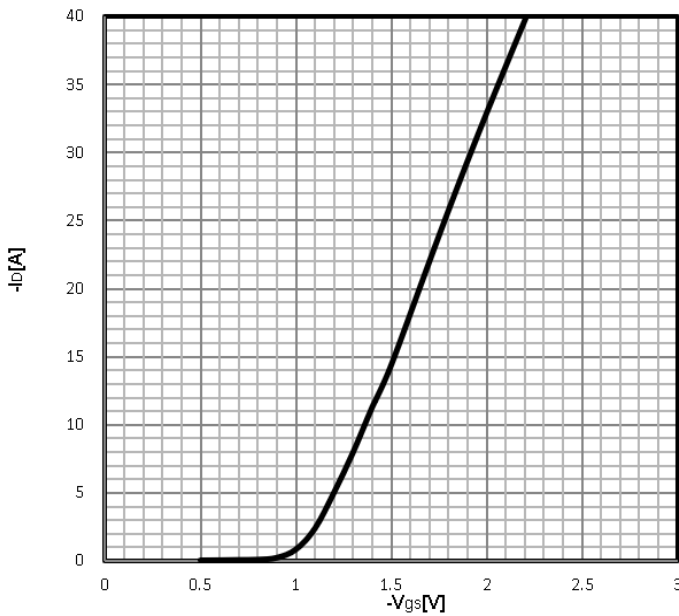
Typ. output characteristics
 $I_D = f(V_{DS})$



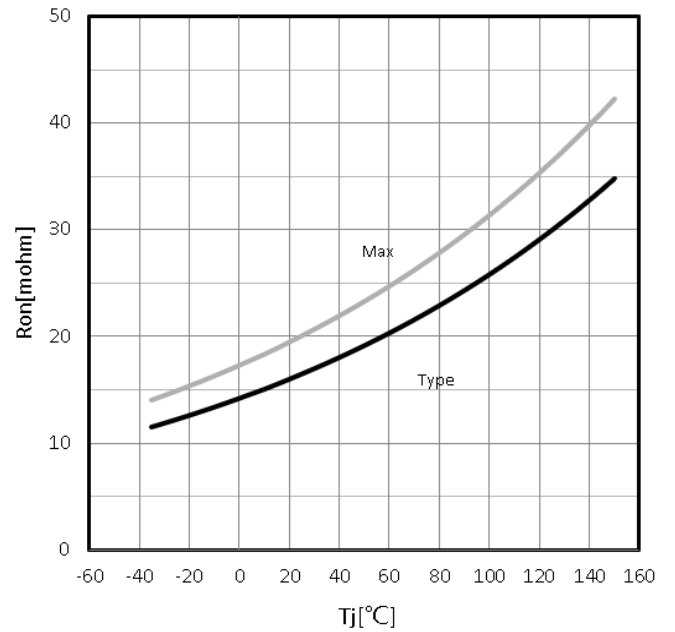
Typ. drain-source on resistance
 $R_{DS(on)} = f(I_D)$



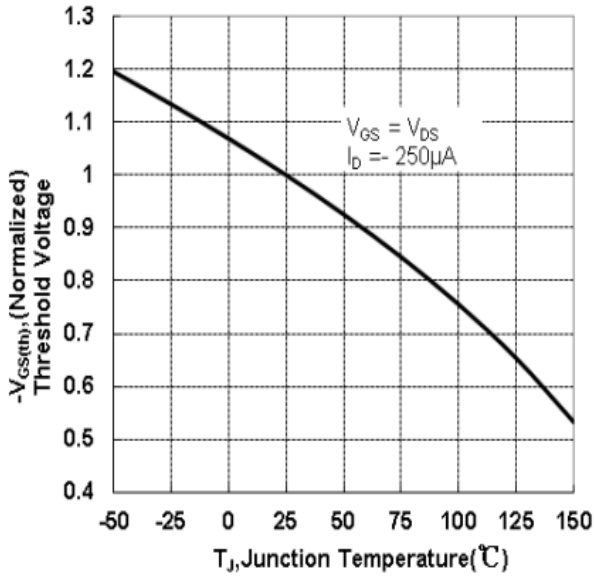
Typ. transfer characteristics
 $I_D = f(V_{GS})$



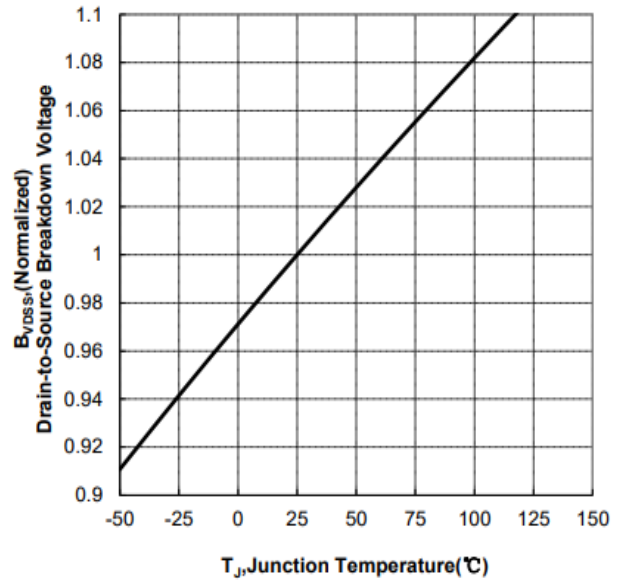
Drain-source on-state resistance
 $R_{DS(on)} = f(T_j); I_D = -4A; V_{GS} = 4.5V$



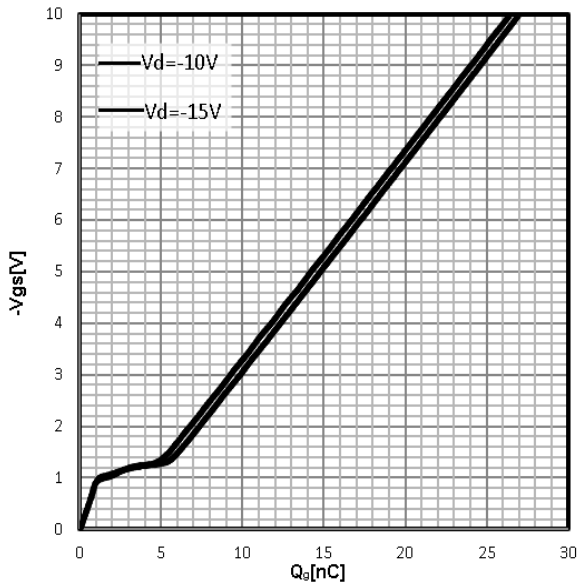
Gate Threshold Voltage
 $-V_{TH}=f(T_j); I_D=-250\mu A$



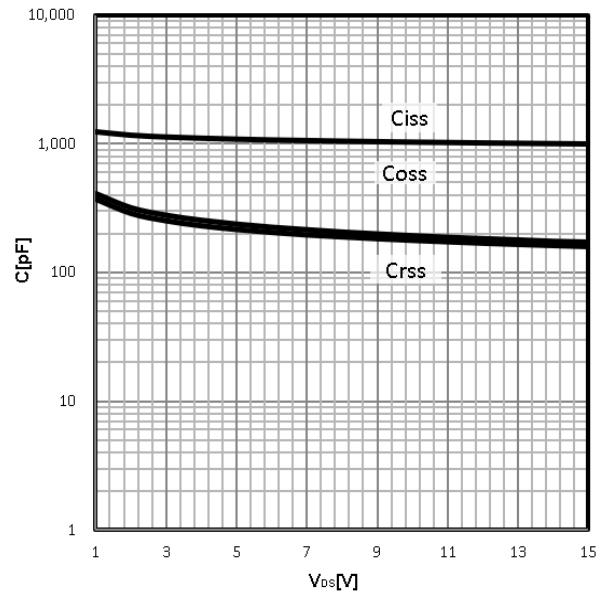
Drain-source breakdown voltage
 $V_{BR(DSS)}=f(T_j); I_D=-250\mu A$



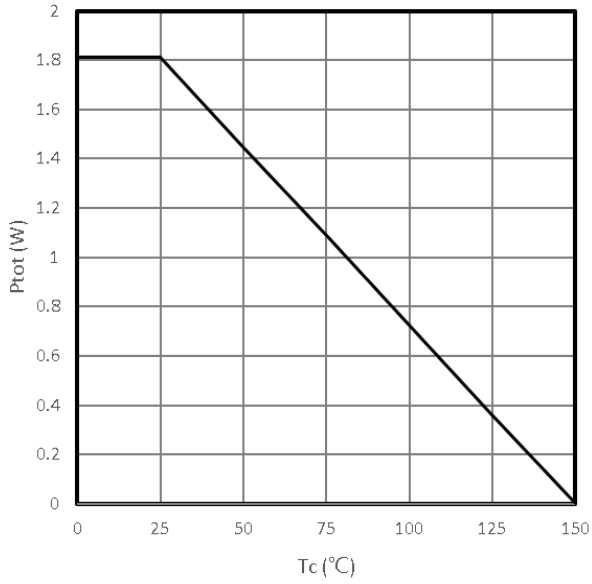
Typ. gate charge
 $V_{GS}=f(Q_g); I_D=-4A$



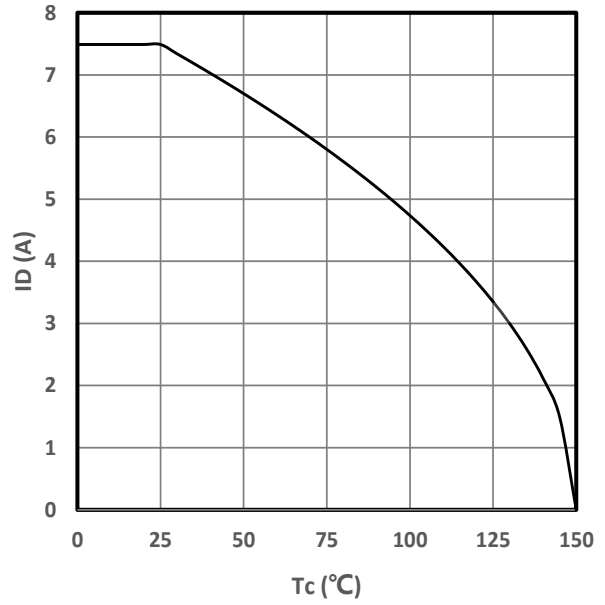
Typ. capacitances
 $C=f(V_{DS}); V_{GS}=0V; f=1MHz$



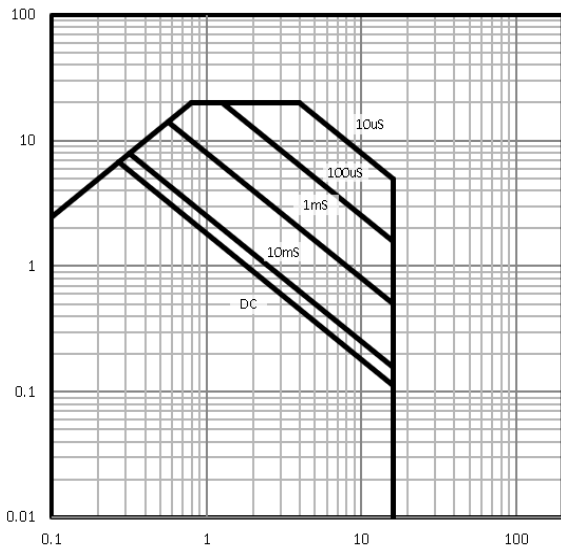
Power Dissipation
 $P_{tot}=f(T_c)$



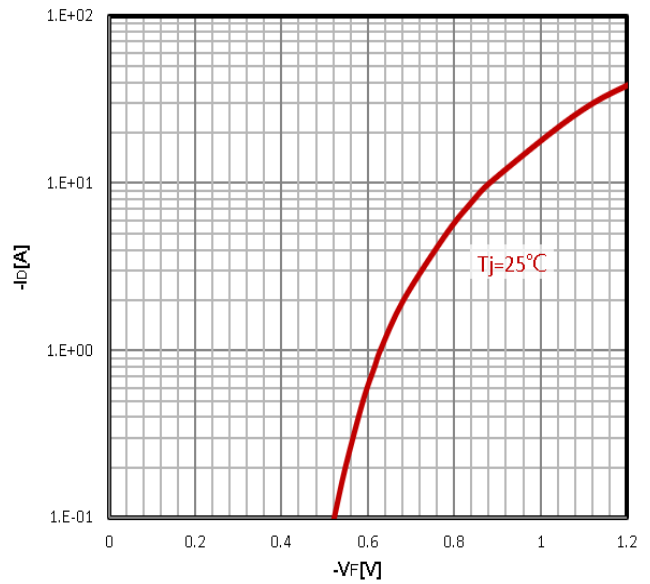
Maximum Drain Current
 $-I_D=f(T_c)$



Safe operating area
 $-I_D=f(-V_{DS})$

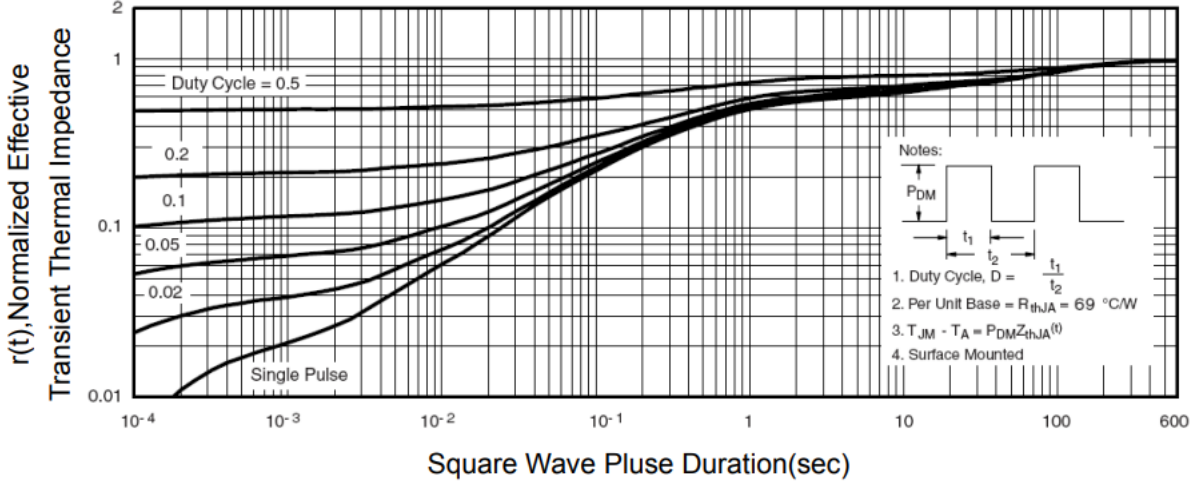


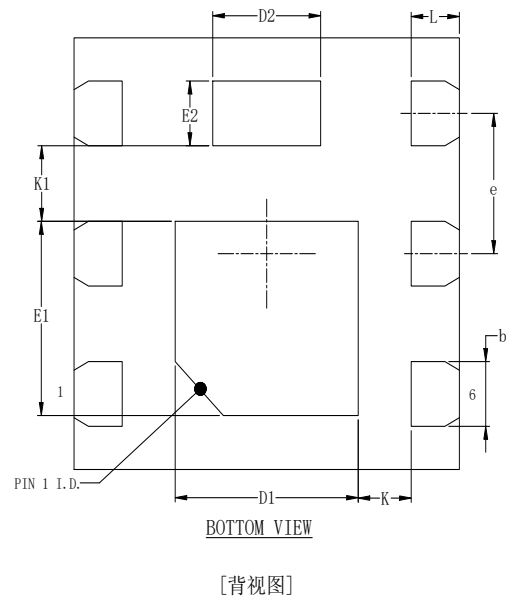
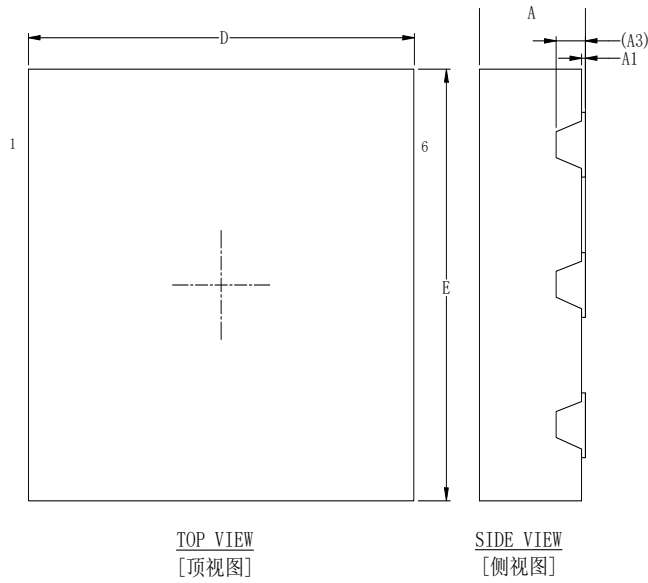
Body Diode Forward Voltage Variation
 $-I_F=f(-V_{GS})$



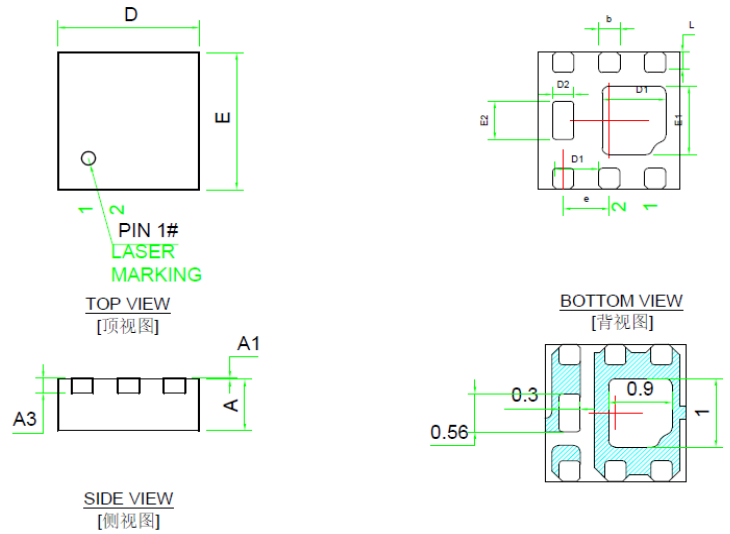
Max. transient thermal impedance

$$Z_{thJC} = f(t_p)$$



●Dimensions (DFN2×2)


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.5	0.55	0.6
STAND OFF		A1	0	0.02	0.05
L/F THICKNESS		A3	0.152 REF		
LEAD WIDTH		b	0.25	0.3	0.35
BODY SIZE	X	D	1.9	2	2.1
	Y	E	1.9	2	2.1
LEAD PITCH		e	0.65 BSC		
EP SIZE	X	D1	0.85	0.95	1.05
		D2	0.46	0.56	0.66
	Y	E1	0.8	0.9	1
		E2	0.2	0.3	0.4
LEAD LENGTH		L	0.2	0.25	0.3
LEAD TIP TO EP EDGE		K	0.275 REF		
EP EDGE TO EP EDGE		K1	0.35 REF		



Symbol	Dimensions In Millimeters		
	Min	Nom	Max
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
A3	0.203REF		
b	0.250	0.300	0.350
D	1.900	2.000	2.100
D1	0.850	0.900	0.950
D2	0.250	0.300	0.350
e	0.650BSC		
E	1.900	2.000	2.100
E1	0.950	1.000	1.050
E2	0.510	0.560	0.610
L	0.250	0.300	0.350


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