

534A

T-46-07-11



74FCT534A

Octal D Flip-Flop with TRI-STATE® Outputs

General Description

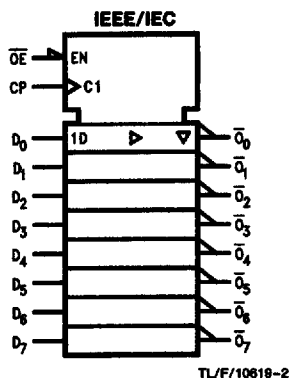
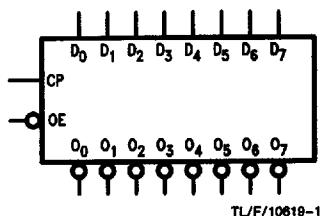
The 74FCT534A is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable (OE) are common to all flip-flops. The 74FCT534A is the same as the 74FCT374A except that the outputs are inverted.

Features

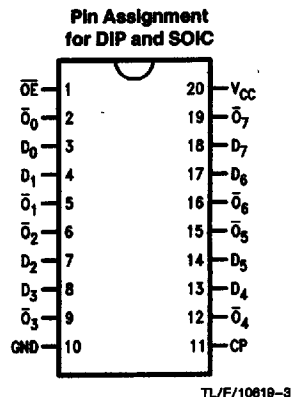
- I_{CC} and I_{OZ} reduced to 40.0 μA and $\pm 2.5 \mu A$ respectively
- NSC 74FCT534A is pin and functionally equivalent to IDT 74FCT534A
- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- TTL input and output level compatible
- TTL inputs accept CMOS levels
- High current latch up
- $I_{OL} = 48 \text{ mA}$

Ordering Code: See Section 8

Logic Symbols



Connection Diagram



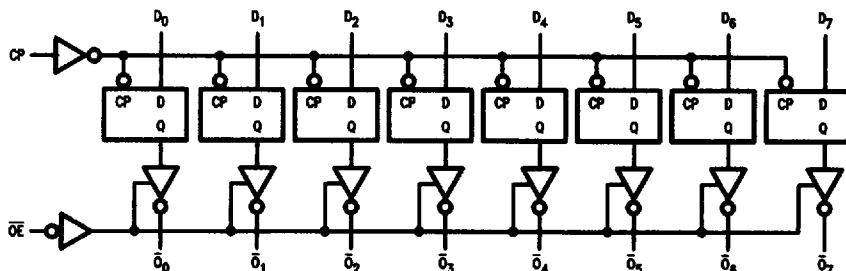
| Pin Names | Description |
|--------------------------------|---------------------------------|
| D ₀ -D ₇ | Data Inputs |
| CP | Clock Pulse Input |
| OE | TRI-STATE Output Enable Input |
| \bar{O}_0 - \bar{O}_7 | Complementary TRI-STATE Outputs |

Functional Description

The 7CT534A consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE complementary outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP)

transition. With the Output Enable (\overline{OE}) LOW, the contents of the eight flip-flops are available at the outputs. When the \overline{OE} is HIGH, the outputs go to the high impedance state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

Logic Diagram



TL/F/10619-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Function Table

| Inputs | | | Output |
|--------|----|---|------------------|
| CP | OE | D | \overline{O} |
| ↗ | L | H | L |
| ↗ | L | L | H |
| L | L | X | \overline{O}_0 |
| X | H | X | Z |

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 ↗ = LOW-to-HIGH Clock Transition
 Z = High Impedance
 \overline{O}_0 = Value stored from previous clock cycle

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|---|-----------------|
| Terminal Voltage with Respect to GND (V _{TERM}) 74FCTA | -0.5V to +7.0V |
| Temperature Under Bias (T _{BIAS}) 74FCTA | -55°C to +125°C |
| Storage Temperature (T _{STG}) 74FCTA | -55°C to +125°C |
| DC Output Current (I _{OUT}) | 120 mA |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ FCT circuits outside databook specifications.

Recommended Operating Conditions

| | |
|---|-----------------------|
| Supply Voltage (V _{CC}) 74FCTA | 4.75V to 5.25V |
| Input Voltage | 0V to V _{CC} |
| Output Voltage | 0V to V _{CC} |
| Operating Temperature (T _A) 74FCTA | -0°C to +70°C |
| Junction Temperature (T _J) PDIP | 140°C |

Note: All commercial packaging is not recommended for applications requiring greater than 2000 temperature cycles from -40°C to +125°C.

DC Characteristics for 'FCTA Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ± 5%, T_A = 0°C to +70°C; V_{HC} = V_{CC} - 0.2V.

| Symbol | Parameter | 74FCTA | | | Units | Conditions | |
|-----------------|-----------------------------------|-------------------------------|-------------------------------|----------------------------|-------|--|--|
| | | Min | Typ | Max | | | |
| V _{IH} | Minimum High Level Input Voltage | 2.0 | | | V | | |
| V _{IL} | Maximum Low Level Input Voltage | | | 0.8 | V | | |
| I _{IH} | Input High Current | | | 5.0 5.0 | μA | V _{CC} = Max | V _I = V _{CC} V _I = 2.7V (Note 2) |
| I _{IL} | Input Low Current | | | -5.0 -5.0 | μA | V _{CC} = Max | V _I = 0.5V (Note 2) V _I = GND |
| I _{OZ} | Maximum TRI-STATE Current | | | 2.5 2.5 -2.5 -2.5 | μA | V _{CC} = Max | V _O = V _{CC} V _O = 2.7V (Note 2) V _O = 0.5V (Note 2) V _O = GND |
| V _{IK} | Clamp Diode Voltage | | | -0.7 -1.2 | V | V _{CC} = Min; I _N = -18 mA | |
| I _{OS} | Short Circuit Current | -60 | -120 | | mA | V _{CC} = Max (Note 1); V _O = GND | |
| V _{OH} | Minimum High Level Output Voltage | 2.8 V _{HC} 2.4 | 3.0 V _{CC} 4.3 | | V | V _{CC} = 3V; V _{IN} = 0.2V or V _{HC} ; I _{OH} = -32 μA | I _{OH} = -300 μA I _{OH} = -15 mA |
| V _{OL} | Maximum Low Level Output Voltage | | GND GND 0.3 | 0.2 0.2 0.5 | V | V _{CC} = 3V; V _{IN} = 0.2V or V _{HC} ; I _{OL} = 300 μA | I _{OL} = 300 μA I _{OL} = 48 mA |
| V _H | Input Hysteresis on Clock Only | | 200 | | mV | | |

DC Characteristics for 'FCTA Family Devices (Continued)

Typical values are at $V_{CC} = 5.0V$, $25^{\circ}C$ ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: $V_{CC} = 5.0V \pm 5\%$, $T_A = 0^{\circ}C$ to $+70^{\circ}C$; $V_{HC} = V_{CC} - 0.2V$.

| Symbol | Parameter | 74FCTA | | | Units | Conditions |
|-----------------|---|--------|------|------|---------|---|
| | | Min | Typ | Max | | |
| I_{CC} | Maximum Quiescent Supply Current | | 1.0 | 40.0 | μA | $V_{CC} = \text{Max}$ $V_{IN} \geq V_{HC}$, $V_{IN} \leq 0.2V$ $f_i = 0$ |
| ΔI_{CC} | Quiescent Supply Current; TTL Inputs HIGH | | 0.5 | 2.0 | mA | $V_{CC} = \text{Max}$ $V_{IN} = 3.4V$ (Note 3) |
| I_{CCD} | Dynamic Power Supply Current (Note 4) | | 0.15 | 0.40 | mA/MHz | $V_{CC} = \text{Max}$ Outputs Open $\overline{OE} = \text{GND}$ One Input Toggling 50% Duty Cycle $V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$ |
| I_C | Total Power Supply Current (Note 6) | | 1.5 | 4.0 | mA | $V_{CC} = \text{Max}$ Outputs Open $f_{CP} = 10 \text{ MHz}$ $\overline{OE} = \text{GND}$ $f_i = 5 \text{ MHz}$ One Bit Toggling 50% Duty Cycle $V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$ |
| | | | 1.8 | 6.0 | | $V_{IN} = 3.4V$ $V_{IN} = \text{GND}$ |
| | | | 3.0 | 7.8 | | $V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$ |
| | | | 5.0 | 16.8 | | $V_{IN} = 3.4V$ $V_{IN} = \text{GND}$ |

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Numbers of Inputs at f_i

All currents are in milliamperes and all frequencies are in megahertz.

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AC Electrical Characteristics: See Section 2 for Waveforms

| Symbol | Parameter | 74FCTA | | Units | Fig. No. |
|------------------------|-------------------------------------|---|--|-------|----------|
| | | $T_A = +25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$ | $T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$ | | |
| | | Typ | Min (Note 1) Max | | |
| t_{PLH} t_{PHL} | Propagation Delay Cp to On | 4.5 | 1.5 6.5 | ns | 2-9 |
| t_{PZH} t_{PZL} | Output Enable Time | 5.5 | 1.5 6.5 | ns | 2-11 |
| t_{PHZ} t_{PLZ} | Output Disable Time | 4.0 | 1.5 5.5 | ns | 2-11 |
| t_s | Set Up Time High or Low Dn to CP | 1.0 | 2.0 | ns | 2-10 |
| t_h | Hold Time High or Low Dn to CP | 1.0 | 1.5 | ns | 2-10 |
| t_w | CP Pulse Width High or Low | 4.0 | 5.0 | ns | 2-9 |

Note 1: Minimum limits guaranteed but not tested on propagation delays.

Capacitance $T_A = +25^\circ\text{C}, f_i = 1.0\text{ MHz}$

| Symbol | Parameter | Typ | Max | Units | Conditions |
|-----------|--------------------|-----|-----|-------|-----------------------|
| C_{IN} | Input Capacitance | 6 | 10 | pF | $V_{IN} = 0\text{V}$ |
| C_{OUT} | Output Capacitance | 8 | 12 | pF | $V_{OUT} = 0\text{V}$ |

Note: This parameter is measured at characterization but not tested.