

# SN74CBT16211 24-BIT BUS SWITCH

SCDS028E – JULY 1995 – REVISED APRIL 1997

- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input and Output Levels
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages

## description

The SN74CBT16211 provides 24 bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

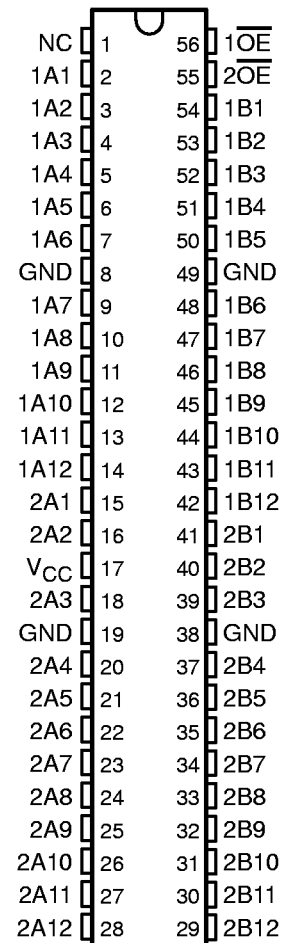
The device operates as a 12-bit or 24-bit bus switch. When  $\overline{1OE}$  is low, 1A is connected to 1B. When  $\overline{2OE}$  is low, 2A is connected to 2B.

The SN74CBT16211 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{1OE}$	$\overline{2OE}$	1A, 1B	2A, 2B
L	L	1A = 1B	2A = 2B
L	H	1A = 1B	Z
H	L	Z	2A = 2B
H	H	Z	Z

DGG, DGV, OR DL PACKAGE  
(TOP VIEW)



NC – No internal connection



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

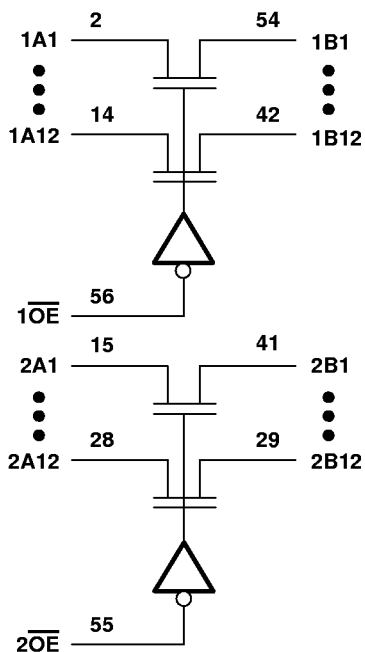
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## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	.....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	.....	-0.5 V to 7 V
Continuous channel current	.....	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	.....	-50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package	.....	81°C/W
	DGV package	86°C/W
	DL package	74°C/W
Storage temperature range, $T_{stg}$	.....	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

## recommended operating conditions

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4	5.5	V
$V_{IH}$	High-level control input voltage	2		V
$V_{IL}$	Low-level control input voltage		0.8	V
$T_A$	Operating free-air temperature	-40	85	°C



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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT			
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA				-1.2	V			
I <sub>I</sub>		V <sub>CC</sub> = 0 V, V <sub>I</sub> = 5.5 V				10	μA			
		V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 5.5 V or GND				±1				
I <sub>CC</sub>		V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND				3	μA			
ΔI <sub>CC</sub> ‡	Control pins	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND				2.5	mA			
C <sub>i</sub>	Control pins	V <sub>I</sub> = 3 V or 0				4.5	pF			
C <sub>io</sub> (OFF)		V <sub>O</sub> = 3 V or 0, $\overline{OE} = V_{CC}$				5.5	pF			
r <sub>on</sub> §		V <sub>CC</sub> = 4 V, V <sub>I</sub> = 2.4 V, I <sub>I</sub> = 15 mA				14	20	Ω		
		V <sub>CC</sub> = 4.5 V		V <sub>I</sub> = 0					5	7
				I <sub>I</sub> = 64 mA					5	7
				V <sub>I</sub> = 2.4 V, I <sub>I</sub> = 15 mA					8	12

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

**switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)**

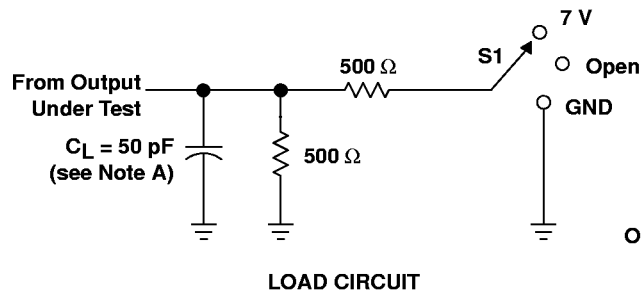
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V ± 0.5 V		V <sub>CC</sub> = 4 V		UNIT
			MIN	MAX	MIN	MAX	
t <sub>pd</sub> ¶	A or B	B or A		0.25		0.25	ns
t <sub>en</sub>	$\overline{OE}$	A or B	3.9	9.3		10.1	ns
t <sub>dis</sub>	$\overline{OE}$	A or B	3.3	8.5		7.1	ns

¶ This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

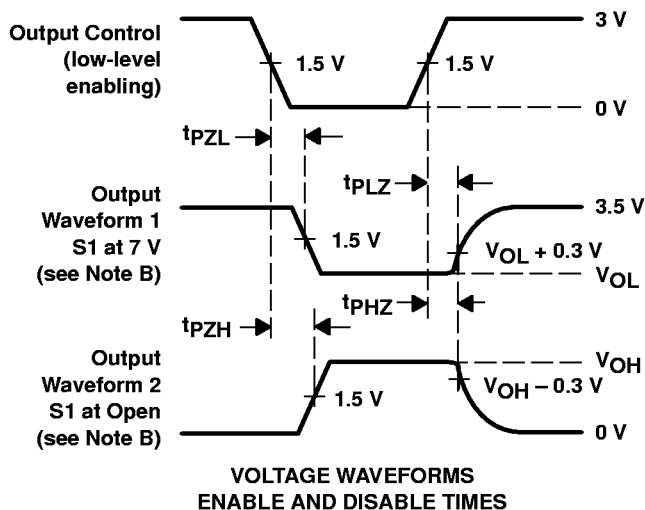
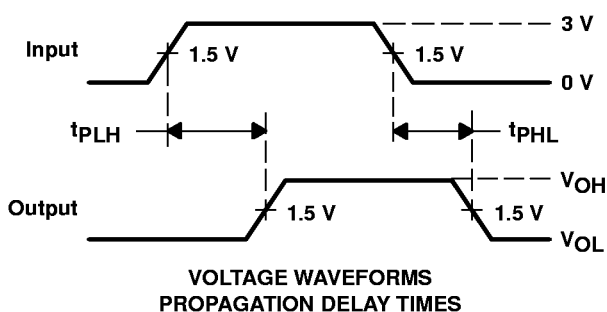
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## PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms