

SN55553, SN55554 ELECTROLUMINESCENT COLUMN DRIVERS

D2744, APRIL 1986

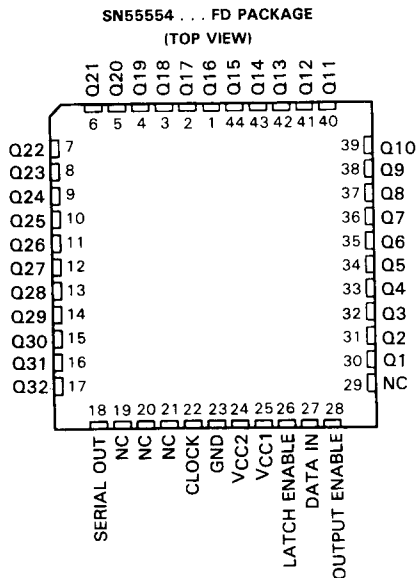
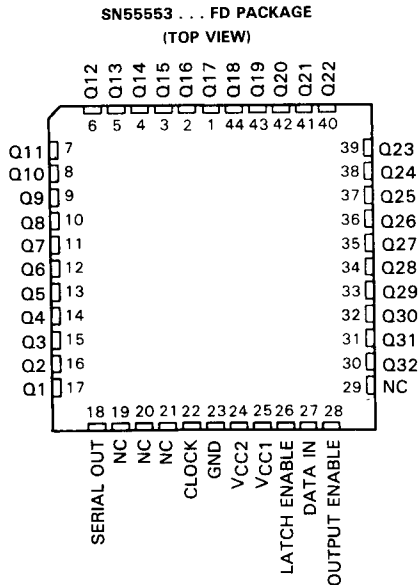
- Each Device Drives 32 Electrodes
- 60-V Output Voltage Swing Capability
- 15-mA Output Source and Sink Current Capability
- High-Speed Serially-Shifted Data Input
- Totem-Pole Outputs
- Latches on All Driver Outputs

description

The SN55553 and SN55554 are monolithic BIDFET[†] integrated circuits designed to drive the column electrodes of an electroluminescent display. The SN55554 output sequence has been reversed from the SN55553 for ease in printed circuit board layout.

The devices consist of a 32-bit shift register, 32 latches, and 32 output AND gates. Serial data is entered into the shift register on the low-to-high transition of the clock input. When high, the Latch Enable input transfers the shift register contents to the outputs of the 32 latches. When Output Enable is high, all Q outputs are enabled. Serial data output from the shift register may be used to cascade shift registers. This output is not affected by the Latch Enable or Output Enable inputs.

The SN55553 and SN55554 are characterized for operation over the full military temperature range of -55°C to 125°C.



NC—No internal connection

[†]BIDFET — Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip — patented process.

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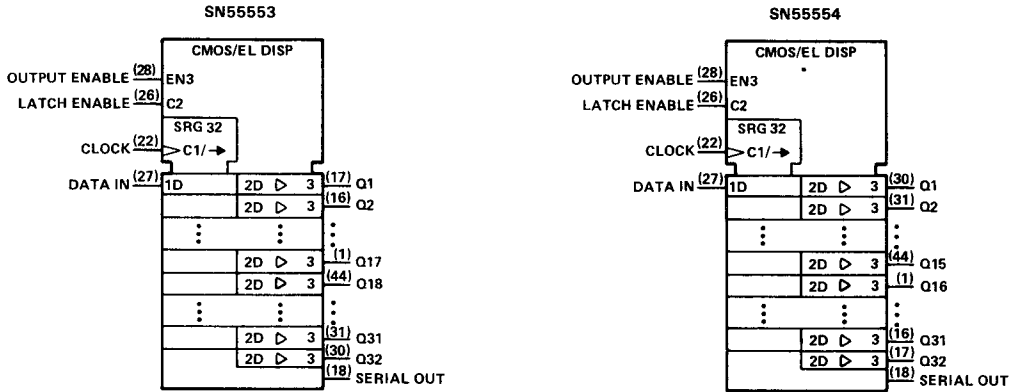


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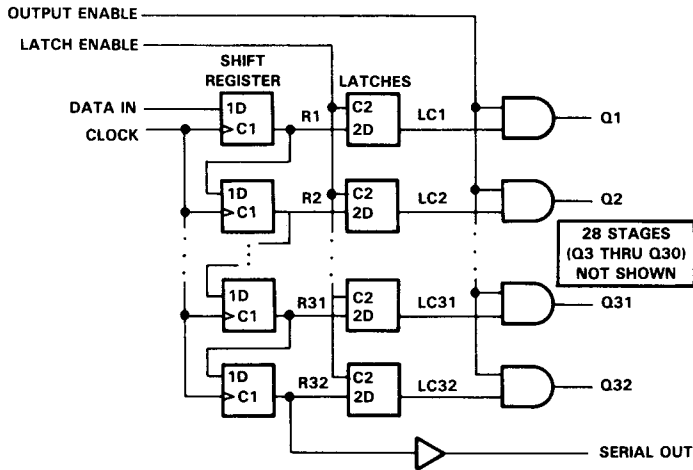
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logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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FUNCTION TABLE

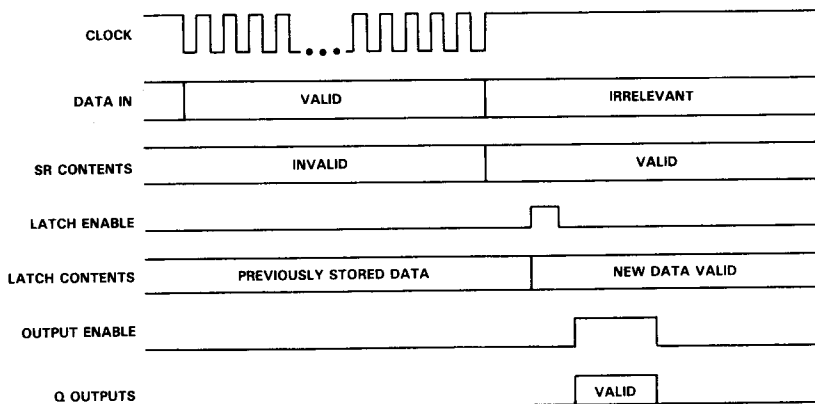
FUNCTION	CONTROL INPUTS			SHIFT REGISTER R1 THRU R32	LATCHES LC1 THRU LC32	OUTPUTS	
	CLOCK	LATCH ENABLE	OUTPUT ENABLE			SERIAL	Q1 THRU Q32
LOAD	↑ No↑	X X	X X	Load and shift† No change	Determined by Latch Enable‡	R32 R32	Determined by Output Enable
LATCH	X X	L H	X X	As determined above As determined above	Stored data New data	R32 R32	Determined by Output Enable
OUTPUT ENABLE	X X	X X	L H	As determined above As determined above	Determined by Latch Enable‡	R32 R32	All L LC1 thru LC32, respectively

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.

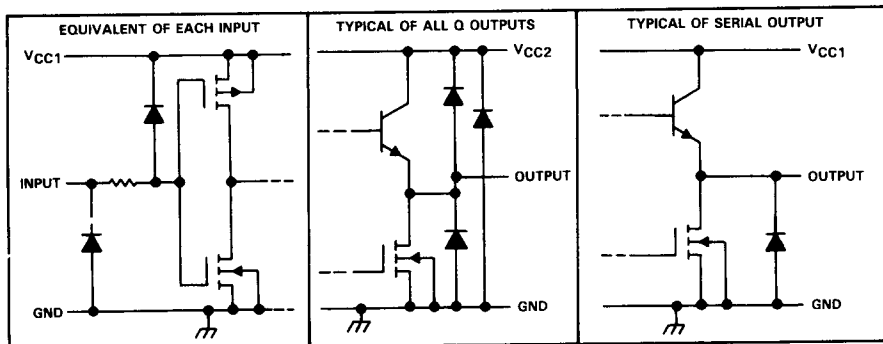
†R32 and the serial output take on the state of R31, R31 takes on the state of R30, . . . R2 takes on the state of R1, and R1 takes on the state of the data input.

‡New data enter the latches while Latch Enable is high. These data are stored while Latch Enable is low.

typical operating sequence



schematic of inputs and outputs



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absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1)	18 V
Supply voltage, V_{CC2}	70 V
Input voltage	$V_{CC1} + 0.3$ V
Ground current	700 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	1825 mW
Minimum operating free-air temperature	-55°C
Operating case temperature	125°C
Storage temperature range	-65°C to 150°C
Case temperature for 60 seconds	260°C

- NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 14.6 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC1}	Supply voltage	10.8	12	13.2	V
V_{CC2}	Supply voltage	0		60	V
V_{IH}	High-level input voltage	$0.75V_{CC}$		$V_{CC}+0.3$	V
V_{IL}	Low-level input voltage	-0.3		$0.25V_{CC}$	V
I_{OH}	High-level output current	-15			mA
I_{OL}	Low-level output current	15			mA
I_{OK}	Peak output clamp diode current			±20	mA
f_{clock}	Clock frequency, $T_A = 25^\circ\text{C}$			6.25	MHz
$t_{w(CLK)}$	Clock pulse duration, high or low, $T_A = 25^\circ\text{C}$	80			ns
$t_{w(LE)}$	Latch enable pulse duration, $T_A = 25^\circ\text{C}$	80			ns
t_{su}	Setup time, data valid before clock 1, $T_A = 25^\circ\text{C}$	20			ns
t_h	Hold time, data valid after clock 1, $T_A = 25^\circ\text{C}$	110			ns
T_A	Operating free-air temperature	-55			
T_C	Operating case temperature			125	

electrical characteristics over recommended operating temperature range, $V_{CC1} = 12$ V, $V_{CC2} = 60$ V

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_O = -15$ mA	55		V
	Q outputs				
V_{OL}	Low-level output voltage	$I_O = 15$ mA		10	V
	Serial output				
I_{IH}	High-level input current (see Note 3)	$V_I = 12$ V		5	μA
	Q outputs				
I_{IL}	Low-level input current (see Note 3)	$V_I = 0$		-5	μA
	Serial output				
I_{CC1}	Supply current, V_{CC1}			7	mA
I_{CC2}	Supply current, V_{CC2}	Outputs high		20	mA
		Outputs low		2	

NOTE 3: I_{IH} and I_{IL} parameter performances are independent of V_{CC2} and need not be 60 V for this test.

switching characteristics, $V_{CC1} = 12\text{ V}$, $V_{CC2} = 60\text{ V}$, $T_C = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{dLH} Delay time, clock \uparrow to serial \downarrow	$C_L = 45\text{ pF}$ to ground,		200	ns
t_{dHL} Delay time, clock \downarrow to serial \downarrow	See Figures 1 and 2		200	ns
t_{dLH} Delay time, LE to Q output \downarrow	$C_L = 45\text{ pF}$ to ground,		1000	ns
t_{dHL} Delay time, LE to Q output \downarrow	See Figures 1 and 3		500	ns

PARAMETER MEASUREMENT INFORMATION

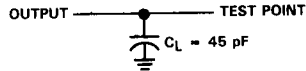


FIGURE 1. OUTPUT LOAD CIRCUIT

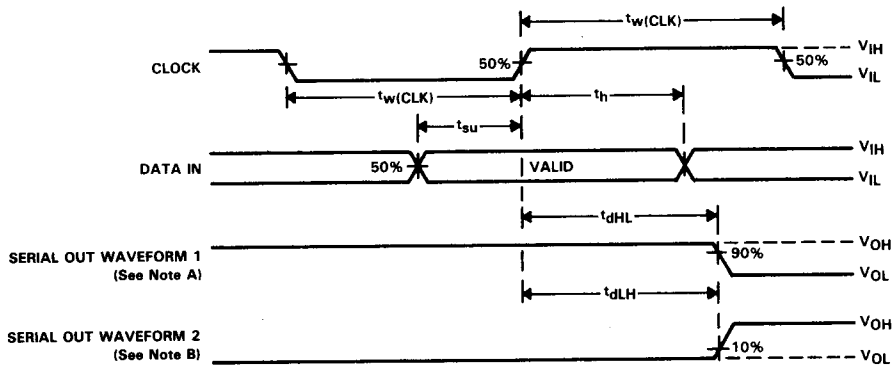


FIGURE 2. VOLTAGE WAVEFORMS FOR SERIAL OUTPUT

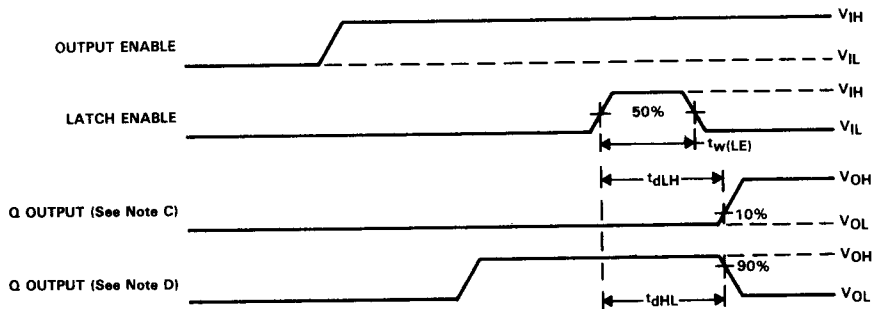


FIGURE 3. VOLTAGE WAVEFORMS FOR Q OUTPUTS

- NOTES: A. Waveform 1 is for internal conditions such that a low is clocked into R32.
 B. Waveform 2 is for internal conditions such that a high is clocked into R32.
 C. To measure t_{dLH} , initially a low is stored in the latch and a high is stored in the shift register.
 D. To measure t_{dHL} , initially a high is stored in the latch and a low is stored in the shift register.