

SN54AS825, SN54AS826 SN74AS825, SN74AS826 8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

D2825, JUNE 1984—REVISED JANUARY 1986

- Functionally Equivalent to AMD's AM29825 and AM29826
- Improved IOH Specifications
- Multiple Output Enables Allow Multiuser Control of the Interface
- Outputs Have Undershoot Protection Circuitry
- Power-Up High-Impedance State
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Buffered Control Inputs to Reduce DC Loading Effect
- Dependable Texas Instruments Quality and Reliability

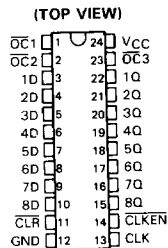
description

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing multiuser registers, I/O ports, bidirectional bus drivers, and working registers.

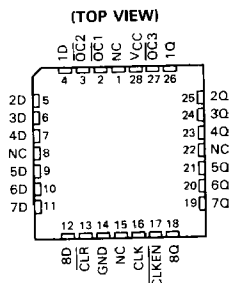
With the clock enable ($\overline{\text{CLKEN}}$) low, the eight D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{\text{CLKEN}}$ high will disable the clock buffer, thus latching the outputs. The 'AS825 has non-inverting D inputs and the 'AS826 has inverting D inputs. Taking the $\overline{\text{CLR}}$ input low causes the eight Q outputs to go low independently of the clock.

Multiuser buffered output-control inputs ($\overline{\text{OC}}1$, $\overline{\text{OC}}2$, and $\overline{\text{OC}}3$) can be used to place the eight outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output controls do not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

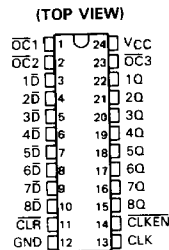
SN54AS825 . . . JT PACKAGE
SN74AS825 . . . DW OR NT PACKAGE



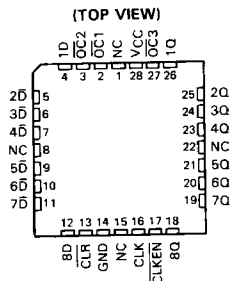
SN54AS825 . . . FK PACKAGE
SN74AS825 . . . FN PACKAGE



SN54AS826 . . . JT PACKAGE
SN74AS826 . . . DW OR NT PACKAGE



SN54AS826 . . . FK PACKAGE
SN74AS826 . . . FN PACKAGE



NC—No internal connection

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.


TEXAS INSTRUMENTS
 POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

Copyright © 1984, Texas Instruments Incorporated

SN54AS825, SN54AS826, SN74AS825, SN74AS826

8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

The SN54AS' family is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AS' family is characterized for operation from 0°C to 70°C .

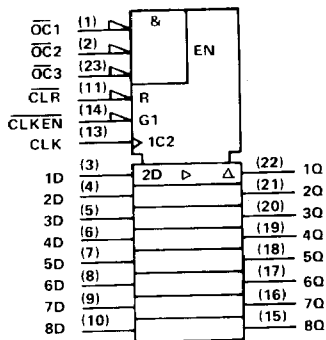
'AS825 FUNCTION TABLE

INPUTS					OUTPUT
$\overline{\text{OC}}^*$	CLR	CLKEN	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

$\overline{\text{OC}}^* = \text{H}$ if any of $\overline{\text{OC}}1$, $\overline{\text{OC}}2$, or $\overline{\text{OC}}3$ are high.

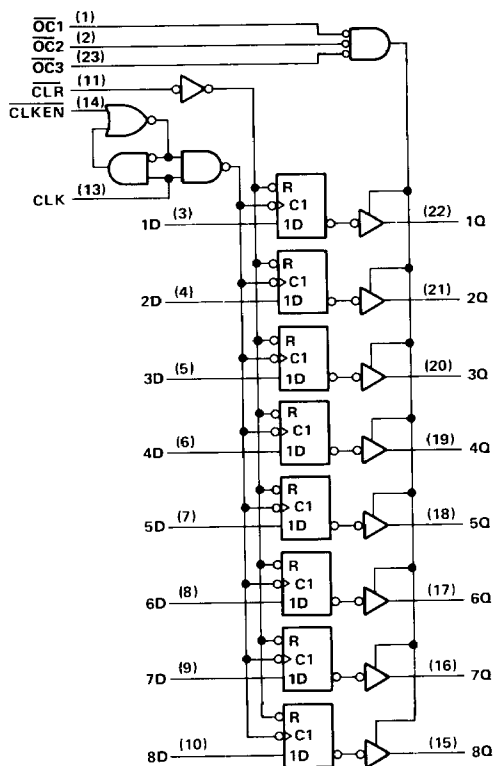
$\overline{\text{OC}}^* = \text{L}$ if all of $\overline{\text{OC}}1$, $\overline{\text{OC}}2$, and $\overline{\text{OC}}3$ are low.

'AS825 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

'AS825 logic diagram (positive logic)



2

LSI Devices

Pin numbers are for DW, JT, and NT packages.

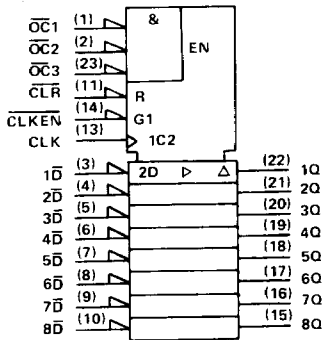
SN54AS826, SN74AS826 8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

'AS826 FUNCTION TABLE

INPUTS					OUTPUT
\overline{OC}^*	CLR	CLKEN	CLK	\overline{D}	Q
L	L	X	X	X	L
L	H	L	↑	H	L
L	H	L	↑	L	H
L	H	H	X	X	Q_0
H	X	X	X	X	Z

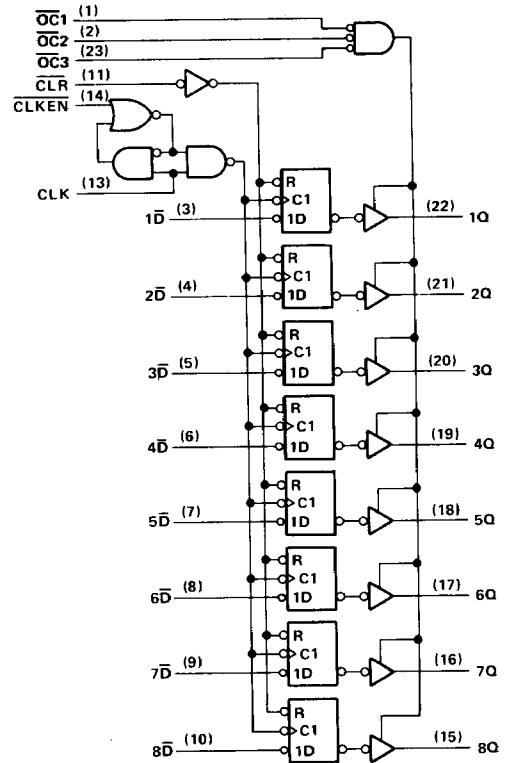
\overline{OC}^* = H if any of $\overline{OC}1$, $\overline{OC}2$, or $\overline{OC}3$ are high.
 \overline{OC}^* = L if all of $\overline{OC}1$, $\overline{OC}2$, and $\overline{OC}3$ are low.

'AS826 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

'AS826 logic diagram (positive logic)



2

LSI Devices

Pin numbers shown are for DW, JT, and NT packages.

SN54AS825, SN54AS826, SN74AS825, SN74AS826

8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range:	
SN54AS825, SN54AS826	-55°C to 125°C
SN74AS825, SN74AS826	0°C to 70°C
Storage temperature range	-65 to 150°C

recommended operating conditions

		SN54AS825 SN54AS826			SN74AS825 SN74AS826			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			-24			-24	mA
I_{OL}	Low-level output current			32			48	mA
t_w	Pulse duration	CLR low	5		4			ns
		CLK high or low	9		8			
t_{su}	Setup time before CLK†	CLR inactive	8		8			ns
		Data	7		6			
		CLKEN high or low	7		6			
t_h	Hold time, \overline{CLKEN} or data after CLK†	0			0			ns
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS825 SN54AS826			SN74AS825 SN74AS826			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $I_{OH} = -2\text{ mA}$	$V_{CC} - 2$			$V_{CC} - 2$			V
	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -15\text{ mA}$	2.4	3.2		2.4	3.2		
	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -24\text{ mA}$	2			2			
V_{OL}	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 32\text{ mA}$		0.3	0.5				V
	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 48\text{ mA}$				0.35	0.5		
I_{OZH}	$V_{CC} = 5.5\text{ V}$, $V_O = 2.7\text{ V}$			50			50	μA
I_{OZL}	$V_{CC} = 5.5\text{ V}$, $V_O = 0.4\text{ V}$			-50			-50	μA
I_I	$V_{CC} = 5.5\text{ V}$, $V_I = 7\text{ V}$			0.1			0.1	mA
I_{IH}	$V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$			20			20	μA
I_{IL}	$V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$			-0.5			-0.5	mA
I_O^\ddagger	$V_{CC} = 5.5\text{ V}$, $V_O = 2.25\text{ V}$	-30		-112	-30		-112	mA
I_{CC}	'AS825	$V_{CC} = 5.5\text{ V}$	Outputs high	45	73	45	73	mA
			Outputs low	56	90	56	90	
			Outputs disabled	59	95	59	95	
	'AS826	$V_{CC} = 5.5\text{ V}$	Outputs high	45	73	45	73	mA
			Outputs low	56	90	56	90	
			Outputs disabled	59	95	59	95	

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

2

LSI Devices

SN54AS825, SN54AS826, SN74AS825, SN74AS826

8-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ $C_L = 50 \text{ pF}$ $R_1 = 500 \Omega$ $R_2 = 500 \Omega$ $T_A = \text{MIN to MAX}$				UNIT
			SN54AS825 SN54AS826		SN74AS825 SN74AS826		
			MIN	MAX	MIN	MAX	
			t_{PLH}	CLK	Any Q	3.5	
t_{PHL}	3.5	11.5	3.5			11	
t_{PHL}	CLR	Any Q	3.5	14	3.5	13	ns
t_{PZH}			\overline{OC}	Any Q	4	12	
t_{PZL}	4	13			4	12	ns
t_{PHZ}	\overline{OC}	Any Q	2	10	2	8	
t_{PLZ}			2	10	2	8	

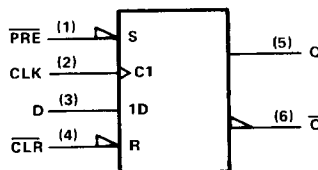
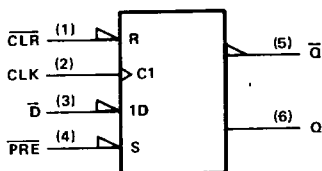
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

D flip-flop signal conventions

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called \overline{Q} . An input that causes a Q output to go high or a \overline{Q} output to go low is called Preset; an input that causes a \overline{Q} output to go high or a Q output to go low is called Clear. Bars are used over these pin names (\overline{PRE} and \overline{CLR}) if they are active-low.

The devices on this data sheet are second-source designs and the pin-name convention used by the original manufacturer has been retained. That makes it necessary to designate the inputs and outputs of the inverting circuit \overline{D} and Q. In some applications it may be advantageous to redesignate the inputs and outputs as D and \overline{Q} . In that case, outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.

Notice that Q and \overline{Q} exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (∇) on \overline{PRE} and \overline{CLR} remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at \overline{D} , Q, and \overline{Q} . Of course pin 5 (Q) is still in phase with the data input D, but now both are considered active high.



2

LSI Devices