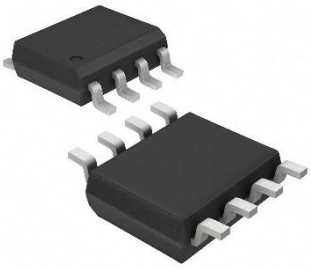
HX1050-S CAN Bus Transceiver

General Description

The HX1050-S serves as the interface between the Controller Area Network (CAN) protocol controller and the physical bus. It is designed for high-speed applications, specifically in passenger cars, supporting speeds of up to 1 MBaud. This device enables differential transmission to the bus and differential reception to the CAN controller.



SOP-8

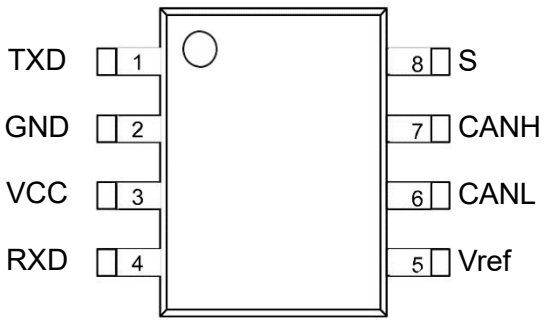
Features

- High speed (up to 1 MBaud)
- Silent mode
- Transceiver in unpowered state disengages from the bus (zero load)
- Differential receiver with high common-mode range for ElectroMagnetic Immunity (EMI)
- At least 110 nodes can be connected
- Transmit Data (TXD) dominant time-out function
- Bus pins protected against transients in automotive environments
- Thermally protected

Applications

- Industrial control automation
- Automotive electronics
- Point-to-point and point-to-multipoint communications
- Intelligent instrumentation
- Building automation systems
- Security systems
- Road traffic control automation
- Level converte

PIN CONFIGURATIONS AND FUNCTIONS



Pin Descriptio		
Pin	**Name**	**Description**
1	TXD	transmit data input
2	GND	ground supply
3	VCC	supply voltage
4	RXD	receive dataoutput;readsoutdata from the bus lines
5	Vref	Reference Voltage Output
6	CANL	LOW-level CAN bus line
7	CANH	HIGH-level CAN busline
8	S	High speed and mute mode selection, low level for high speed

Absolute Maximum Rating				
SYMBOL	PARAMETER	MIN	MAX	UNIT
VCC	Supply voltage range	-0.3	+6	V
TXD, RXD, STB, Vref	MCU Side Port	-0.3	VCC+0.3	V
CANL, CANH	Bus-side port voltage	-60	+60	V
Vtr	Pin 6, 7 Transient Voltage	-200	+200	V
	storage temperature	-55	150	℃
	ambient temperature	-40	125	℃
	Welding temperature range	-	300	℃

SPECIFICATIONS

(VCC=5V±10%, Temp=TMIN~TMAX, typical values at VCC=+5V, Temp=25°C, unless otherwise noted)

Bus Transmitter DC Character						
SYMBOL	PARAMETER	TESTCONDITIONS	MIN	MAX	UNIT	SYMB
VOH(D)	CANH output voltage (dominant)	VI=0V，STB=0V，RL=60Ω F1、 2	2.9	3.4	4.5	
VOL(D)	CANL output voltage (dominant)		0.8		1.5	
VO(R)	Bus Output Differential Voltage(implicit)	VI=3V，STB=0V，RL=60Ω，F1、2	2	2.5	3	V
VOD(D)	Bus Output Differential Voltage (dominant)	VI=0V，STB=0V，RL=60Ω，F1、2	1.5		3	V
VOD(R)	Bus Output Differential Voltage (implicit)	VI=3V, S=0V, F1、 2	-0.012		0.012	V
		VI=3V，STB=0V，NO LOAD	-0. 5		0.05	V
Vdom(TX)sym	dominant output voltage symmetry	Vdom(TX)sym=VCC- VCANH	-400		400	mV
VTXsym	Output Voltage Symmetry	VTXsym= VCANH + VCANL	0.9VC		1.1VC	V
VOC	Common mode output voltage	STB=0V，F 8	2	2.5	3	V
△VOC	Explicit and implicit common mode output voltage difference			30		mV
IOS	Short-circuit output current	CANH=-12V,	-105	-72		mA
VIL	Low Level Input			0.36	1	
I_{OS}	Short-circuit output current Hidden output current	CANH=-12V, CANL=open， F 11	-1	0.5		
$I_{O(R)}$		CANH=12V, CANL=open, F 11		71	105	
		-27V<CANH<32V 0<VCC<5.25V	-2.0		2.5	mA
Bus Transmitter Switch Characteristic						
tPLH	Transmission delay (low to high)	STB=0V，F 4	25	65	120	ns
tPHL	Transmission delay (high to low)		25	45	90	ns
tr	Differential output rise delay time			25		ns
tf	Differential output fall delay time			50		ns
tEN	Enable time from listen mode to dominant	F 7			1	μs
tdom	Explicit timeout	F 10	300	450	700	μs
tBUS	Bus wake-up time		0.7		5	μs

SYMBOL	PARAMETER	TESTCONDITIONS	MIN	MAX	UNIT	SYMBO
Bus Receiver DC Paramete						
	Positive Input Threshold	S=0V		800	900	mV
V_{IT-}	Negative Input Threshold		500	650		
V_{HYS}	Comparator Threshold Hysteresis		100	125		
V_{OH}	High Level Output Voltage	IO=-2mA	4	4.6		V
V_{OL}	Low Level Output Voltage	IO=2mA		0.2	0.4	V
$I_{(OFF)}$	Bus input current at power down	CANH or CANL=5V，Other pin=0V		165	125	μA
C_I	CANH, CANL input capacitance to			13		pF
C_{ID}	CANH, CANL Differential Input			5		pF
R_{IN}	CANH, CANL Input Resistance	TXD=3V，STB=0V	15	30	40	KΩ
R_{ID}	CANH, CANL Differential Input		30		80	KΩ
RI_{match}	RI(CANH), RIN(CANL) mismatches	CANH=CANL	-3%		3%	
V_{COM}	Common mode voltage range		-12		12	V
Bus Receiver Switching Characteris						
tPLH	Propagation delay (low to high)	STB=0V or VCC	60	100	130	ns
tPHL	Propagation delay (high to low)		45	70	90	ns
tr	RXD signal rise time			8		ns
tf	RXD signal fall time			8		ns
Device Switching Character						
Td(LOOP1)	Loop delay 1, driver input to receiver output, implicit to explicit	STB=0V	90		190	ns
Td(LOOP2)	Loop Delay 2, Driver Input to Receiver Output, Explicit to Implicit		90		190	ns
Over-temperature protectio						
Tj(sd)	Over temperature shutdown		155	165	180	℃
TXD Pin Characteristi						T
IIH(TXD)	TXD port high level input current	VI=VCC	-2		2	μA
IIL(TXD)	TXD Port Low Level Input Current	VI=0	-50		-10	μA
IO(off)	Current in TXD when VCC=0V	VCC=0V，			1	μA
VIH	Input High LowerLimit		2		VCC+0.	V
VIL	Input Low Limit		-0.3		0.8	V
TXDO	TXD Port Dangle Voltage			H		logic
Vref pin reference voltage output						
Vref	Reference Output Voltage	-50uA<I_o<50uA	0.4V_{CC}		0.6V_{CC}	V
Power consumption characteristic						
ICC	Silent Mode Power Consumption	S=VCC，VI=VCC		6	10	μA
	Dominant power consumption	VI=0V，S=0V LOAD=60Ω		50	70	mA
	Implicit power consumption	VI=VCC，S=0V NO LOAD		6	10	mA

Menu (1)H=high; L=low; X=no care

Table 1 CAN Transceiver Truth

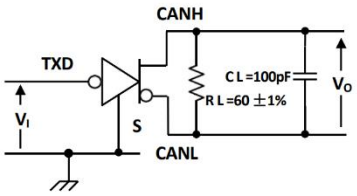
VCC	TXD(1)	STB(1)	CANH(1)	CANL(1)	BUS STATE	RXD(1)
4.5V~5.5V	L	L(or float)	H	L	dominant	L
4.5V~5.5V	H (or float)	X	0.5VCC	0.5VCC	implicit	H
4.5V~5.5V	X	H	0.5VCC	0.5VCC	implicit	H
0<VCC<4.5V	X	X	0V<VCANH<VCC	0V<VCANL<VCC	implicit	X

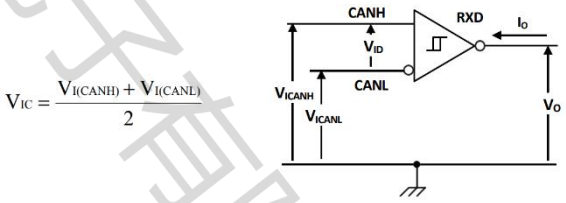
Table 2 Driver Function

INPUTS		OUTPUTS		Bus State
TXD(1)	STB(1)	CANH(1)	CANL(1)	
L	L(or float)	H	L	Dominate(dominant)
H (or floa)	X	Z	Z	Recessive(implicit)
X	H	Z	Z	Recessive(implicit)

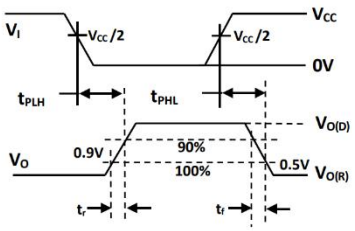
Table 3 Receiver Functio

VID=CANH-CANL	RXD(1)	Bus State(1)
VID≥0.9V	L	Dominate(dominant)
0.5< VID<0.9V		
VID≤0.5V	H	Recessive (implicit)
Open	H	Recessive (implicit)

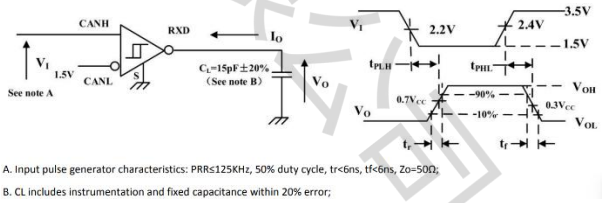




Receiver Voltage and Current Definitions



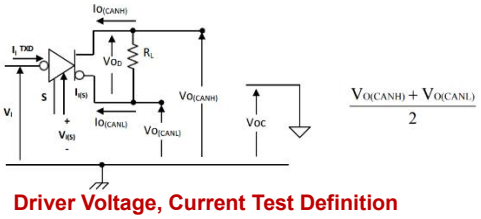
Driver Test Circuit and Voltage Waveforms



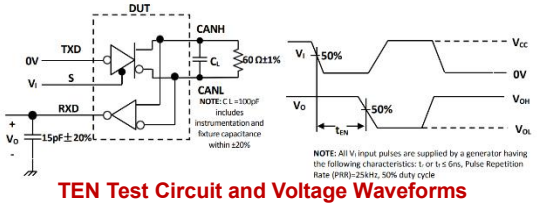
A. Input pulse generator characteristics: PRR≤125KHz, 50% duty cycle, tr<6ns, tf<6ns, Zo=50Ω;

B. CL includes instrumentation and fixed capacitance within 20% error;

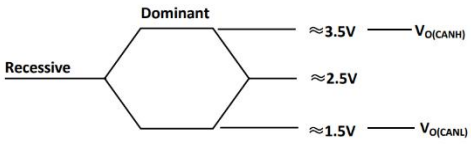
Receiver test circuit and voltage wave



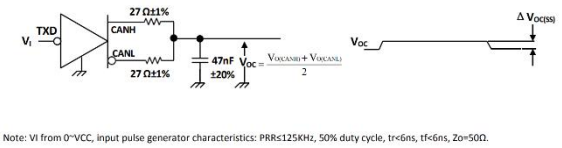
Driver Voltage, Current Test Definition



TEN Test Circuit and Voltage Waveforms

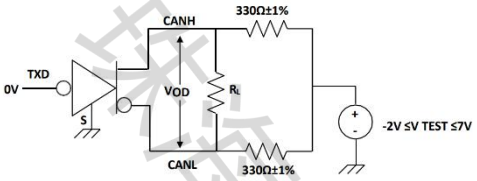


Bus Logic Voltage Definit

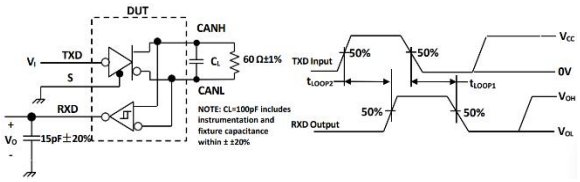


Note: VI from 0~VCC, input pulse generator characteristics: PRR≤125KHz, 50% duty cycle, tr<6ns, tf<6ns, ZO=50Ω.

Common Mode Output Voltage Test and Wave



Driver VOD Test Circuit



t(LOOP) Test Circuit and Waveform

DESCRIPTION

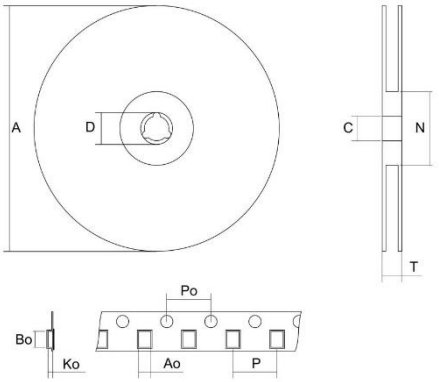
The HX1050-S is a chip that serves as an interface between a CAN protocol controller and the physical bus in various applications such as trucks, buses, cars, and industrial control systems. It is designed to comply with the ISO 11898 standard and can achieve a speed of 1Mbps.

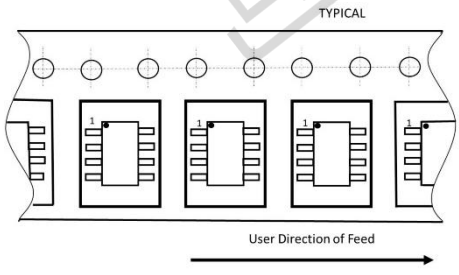
One of the key features of the HX1050-S is its short circuit protection, which prevents the driver circuit from short-circuiting to positive and negative supply voltages. This protection mechanism limits the current flow and safeguards the driver stage from damage.

Additionally, the HX1050-S incorporates an over-temperature protection function. When triggered, this function reduces the current in the driver stage, which helps to lower the chip's temperature. Meanwhile, the rest of the chip continues to function normally.

Another important feature is the built-in TXD dominant timeout timer circuit. This circuit prevents the bus line from being permanently driven to a dominant state, which could block all network communications, in case of a hardware or software failure that keeps the TXD pin low for an extended period. The timer is triggered by a negative edge on the TXD pin, and if the low level duration exceeds the internal timer value, the transmitter is disabled, causing the bus to enter a recessive state. The timer can be reset by a positive edge on the TXD pin.

Packing





package	quantity
Taping	2500

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