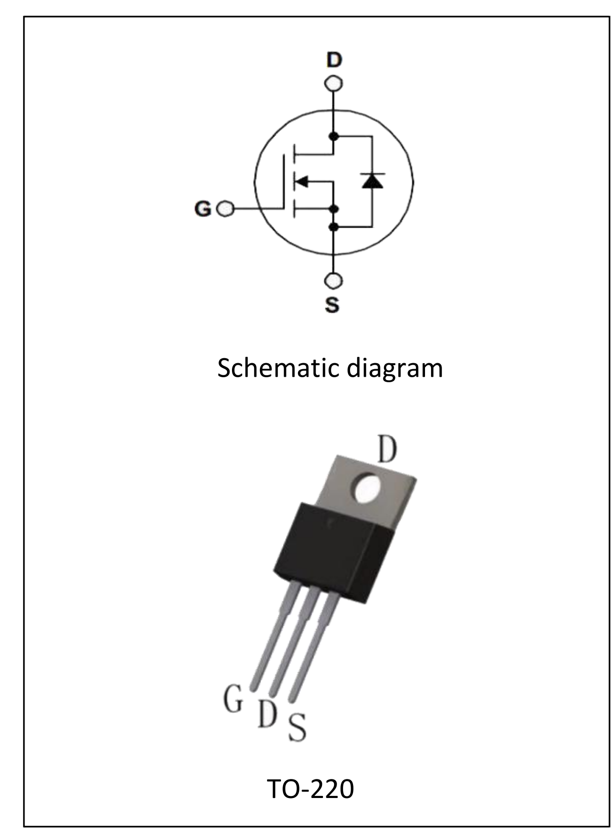
IRFZ24N

60V N-Channel Power MOSFET

DESCRIPTION

The IRFZ24N uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.



Schematic diagram

TO-220

KEY CHARACTERISTICS

① VDS = 60V,ID = 30A

RDS(ON) < 30mΩ @ VGS=10V

RDS(ON) < 40mΩ @ VGS=4.5V

② High density cell design for lower Rdson

③ Fully characterized avalanche voltage and current

④ Good stability and uniformity with high EAS

⑤ Excellent package for good heat dissipation

Application

① Power switching application

② Hard switched and High frequency circuits

③ Uninterruptible power supply

Package Marking And Ordering Information

Device Marking	Ordering Codes	Package	Product Code	Packing
IRFZ24N	IRFZ24N	TO-220	IRFZ24N	Tube

Absolute Maximum Ratings (TA=25℃ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	30	A
Drain Current-Pulsed (Note 1)	I_{DM}	80	A
Maximum Power Dissipation(Tc=25℃)	P_D	44	W
Single pulse avalanche energy(Note 2)	E_{AS}	56	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case	$R_{\theta JC}$	3.4	℃/W

Electrical Characteristics (TA=25℃ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1.3	1.8	2.3	V
Drain-Source On-State Resistance(Note 3)	$R_{DS(ON)}$	V_{GS}=10V, I_D=10A	-	25	30	mΩ
		V_{GS}=4.5V, I_D=10A	-	30	40	
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=10A	-	11	-	S
Dynamic Characteristics						
Input Capacitance	C_{lss}	V_{DS}=25V,V_{GS}=0V, f=1.0MHz	-	670	-	pF
Output Capacitance	C_{oss}		-	76	-	pF
Reverse Transfer Capacitance	C_{rss}		-	66	-	pF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=30V, ID=10A, V_{GS}=10V,R_{GEN}=10Ω	-	19.2	-	nS
Turn-on Rise Time	t_r		-	6.4	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	29.2	-	nS
Turn-Off Fall Time	t_f			8.2	-	nS
Total Gate Charge	Q_g	V_{DS}=48V,I_D=10A V_{GS}=10V	-	21	-	nC
Gate-Source Charge	Q_{gs}		-	5	-	nC
Gate-Drain Charge	Q_{gd}		-	6.5	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	V_{GS}=0V,I_S=20A	-	-	1.2	V
Reverse Recovery Time	T_{rr}	Tj=25℃，IF=10A，di/dt=100A/uS（note3）	-	33.6	-	nS
Reverse Recovery Charge	Q_{rr}		-	32.1	-	nC

Notes:
1. Repetitive Rating: Pulse width limited by maximum junctiontemperature.
2. E_{AS} condition :T_j=25℃,V_{DD}=30V,V_{GS}=10V,L=0.5mH,Rg=25Ω
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤2%.
4. Guaranteed by design, not subject to production.

Characteristics Curves

Figure 1 Output Characteristics	Figure 2 Transfer Characteristics
Figure 3 On-Resistance vs. I_D and V_{GS}	Figure 4 On-Resistance vs. Junction Temperature
Figure 5 On-Resistance vs. V_{GS}	Figure 6 Body Diode Forward Voltage

Figure 7 Gate-Charge Characteristics

V_{DS} =48V
I_D = 10A
V_{GS},Gate-to-Source Voltage,V
Q_G,Total Gate Charge,nC

Figure 8 Capacitance Characteristics

f = 1MHz
$C_{iss} = C_{gs}+C_{gd}$
$C_{oss} = C_{ds}+C_{gd}$
$C_{rss} = C_{gd}$
Capacitance,pF
V_{DS},Drain-to-Source Voltage,V

Figure 9 Maximum Forward Biased Safe Operation Area

10µs
100µs
1ms
10ms
DC
Operation in This Area is Limited by $R_{DS(on)}$
SINGLE PULSE
T_C=25℃
T_J=175℃
I_D,Drain Current,A
V_{DS},Drain-to-Source Voltage,V

Figure 10 Single Pulse Power Rating Junction-to-Ambient

T_A=25℃
$T_{J(MAX)}$=175℃
Single Pulse
Power(W)
Pluse Width（S）

Figure 11 Normalized Maximum Transient Thermal Impedance

In descending order
D=0.5,0.2,0.1,0.05,0.02,0.01, Sing Pulse
$Z_{\theta JC}$,Normalized Transient Thermal Resistance
T , Rectangular Pulse Duration [sec]

$D=T_{on}/T$

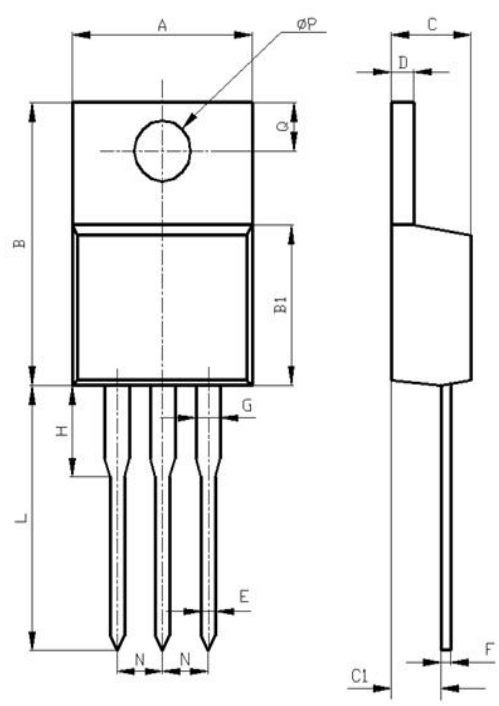
$T_{J,PK}=T_C+P_{DM}\cdot Z_{\theta JC}\cdot R_{\theta JC}$

$R_{\theta JC}$=3.4℃/W

Test Circuit and Waveform

Gate Charge Test Circuit	Gate Charge Test Waveform
+ VDC - Vds DUT Vgs Ig	Vgs Qg 10V Qgs Qgd Charge
Resistive Switching Test Circuit	**Resistive Switching Test Waveforms**
RL Vds DUT + VDC Vdd - Vgs Rg Vgs	Vds 90% 10% Vgs $t_{d(on)}$ t_r t_{on} $t_{d(off)}$ t_f t_{off}
Unclamped Inductive Switching (UIS) Test Circuit	**Unclamped Inductive Switching (UIS) Test Waveforms**
L Vds Id Vgs + VDC Vdd - Vgs Rg DUT Vgs	$E_{AR} = 1/2\ LI_{AR}^2$ BV_{DSS} Vds Id I_{AR} Vgs
Diode Recovery Test Circuit	**Diode Recovery Test Waveforms**
Vds + DUT Vds - Isd L + VDC Vdd - Vgs Ig	$Q_{rr} = -\int Idt$ Vgs Isd I_F dI/dt t_{rr} I_{RM} Vds Vdd

Package Description



Items	Values(mm)	
	MIN	MAX
A	9.60	10.6
B	15.0	16.0
B1	8.90	9.50
C	4.30	4.80
C1	2.30	3.10
D	1.20	1.40
E	0.70	0.90
F	0.30	0.60
G	1.17	1.37
H	2.70	3.80
L	12.6	14.8
N	2.34	2.74
Q	2.40	3.00
ΦP	3.50	3.90

TO-220 package

NOTE:

1. Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. Please do not exceed the absolute maximum ratings of the device when circuit designing.
2. When installing the heat sink, please pay attention to the torsional moment and the smoothness of the heat sink.
3. MOSFETs is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.
4. Shenzhen Minos reserves the right to make changes in this specification sheet and is subject to change withoutprior notice.

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