

60V N-Channel Power MOSFET

DESCRIPTION

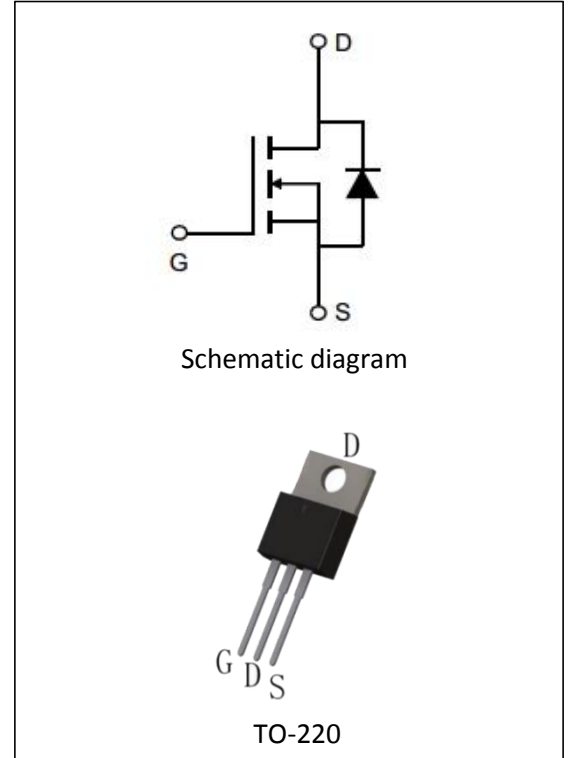
The IRF1405 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.

KEY CHARACTERISTICS

- ① $V_{DS} = 60V, I_D = 190A$
 $R_{DS(ON)} < 3.5m\Omega @ V_{GS}=10V$
- ② High density cell design for lower R_{dson}
- ③ Fully characterized avalanche voltage and current
- ④ Good stability and uniformity with high EAS
- ⑤ Excellent package for good heat dissipation

Application

- ① Power switching application
- ② Hard switched and High frequency circuits
- ③ Uninterruptible power supply



Package Marking And Ordering Information

Ordering Codes	Package	Product Code	Packing
IRF1405	TO-220	IRF1405	Tube

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	190	A
Drain Current-Pulsed ^(Note 1)	I_{DM}	600	A
Maximum Power Dissipation($T_c=25^\circ C$)	P_D	210	W
Single pulse avalanche energy ^(Note 2)	E_{AS}	1000	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.7	$^\circ C/W$
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Electrical Characteristics (TA=25 °C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=60V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3	4	V
Drain-Source On-State Resistance ^(Note 3)	$R_{DS(on)}$	$V_{GS}=10V, I_D=50A$	-	3.2	3.5	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=50V, I_D=75A$	-	180	-	S
Dynamic Characteristics						
Input Capacitance	C_{iss}	$V_{DS}=25V,$ $V_{GS}=0V,$ $f=1.0MHz$	-	8200	-	pF
Output Capacitance	C_{oss}		-	760	-	pF
Reverse Transfer Capacitance	C_{rss}		-	680	-	pF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	td(on)	$V_{DD}=30V, I_D=40A,$ $V_{GS}=10V, R_{GEN}=3\Omega$	-	27	-	nS
Turn-on Rise Time	tr		-	25	-	nS
Turn-Off Delay Time	td(off)		-	90	-	nS
Turn-Off Fall Time	tf		-	40	-	nS
Total Gate Charge	Qg	$V_{DS}=60V, I_D=40A, V_{GS}=10V$	-	186	-	nC
Gate-Source Charge	Qgs		-	46	-	nC
Gate-Drain Charge	Qgd		-	70	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=190A$	-	-	1.2	V

Notes:

- 1.Repetitive Rating: Pulse width limited by maximum junction temperature.
- 2.EAS condition :T j=25 °C ,VDD=50V,VG=10V,L=0.5mH,Rg=25 Ω
- 3.Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
- 4.Guaranteed by design, not subject to production.

Characteristics Curves

Figure 1 Output Characteristics

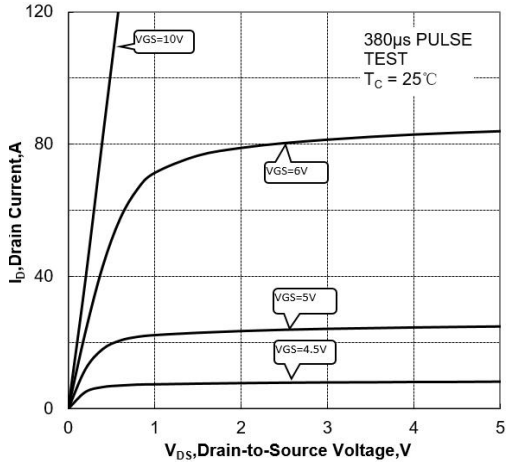


Figure 2 Transfer Characteristics

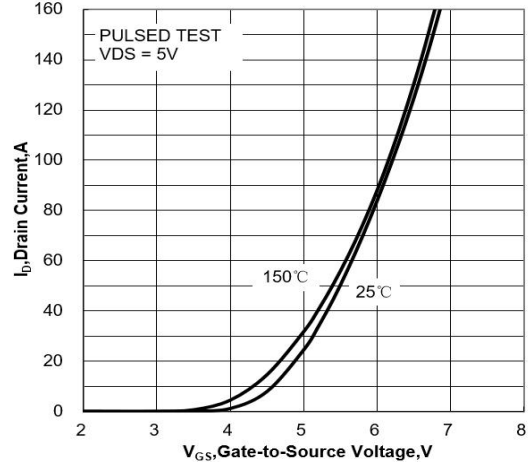


Figure 3 On-Resistance vs. ID and VGS

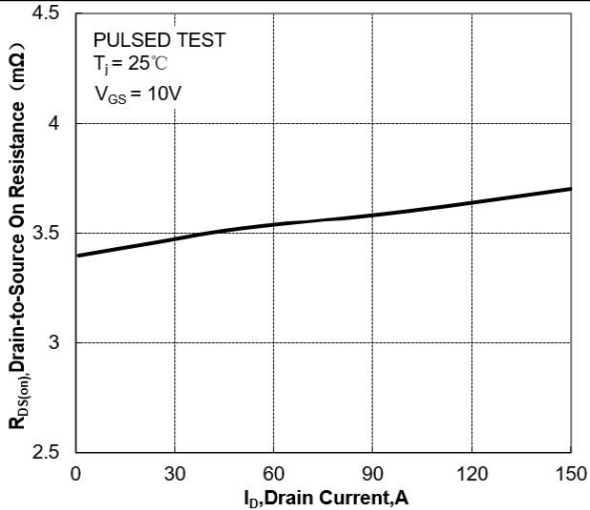


Figure 4 On-Resistance vs. Junction Temperature

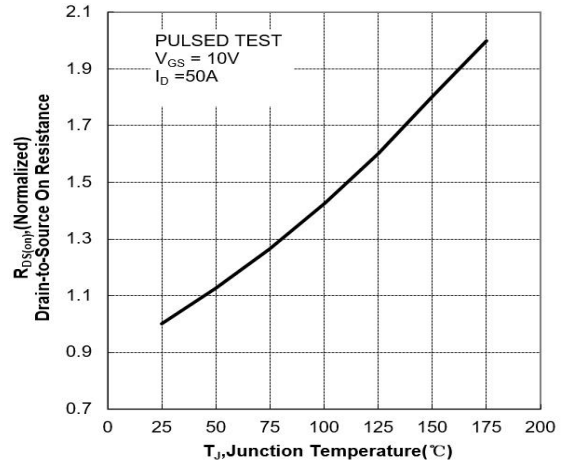


Figure 5 On-Resistance vs. VGS

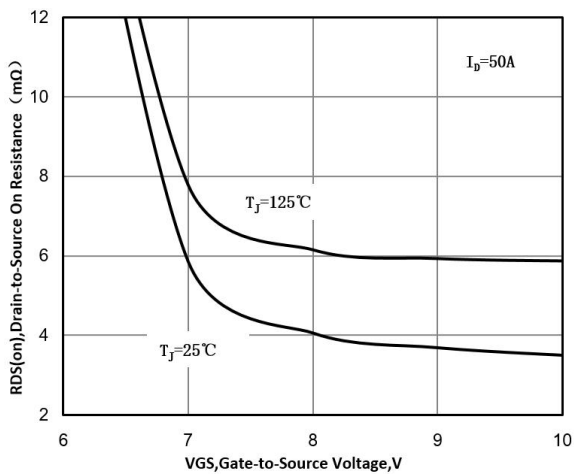


Figure 6 Body Diode Forward Voltage

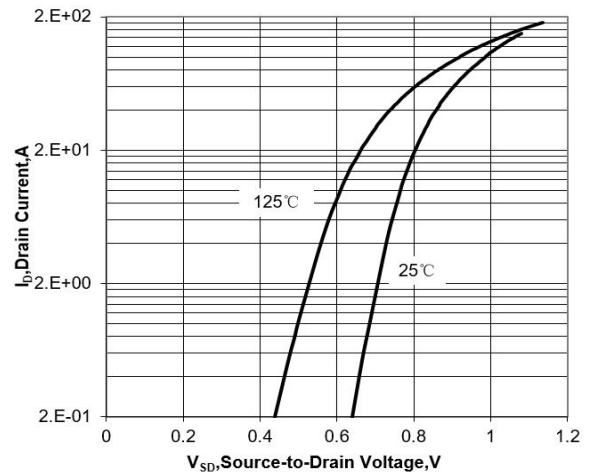


Figure 7 Gate-Charge Characteristics

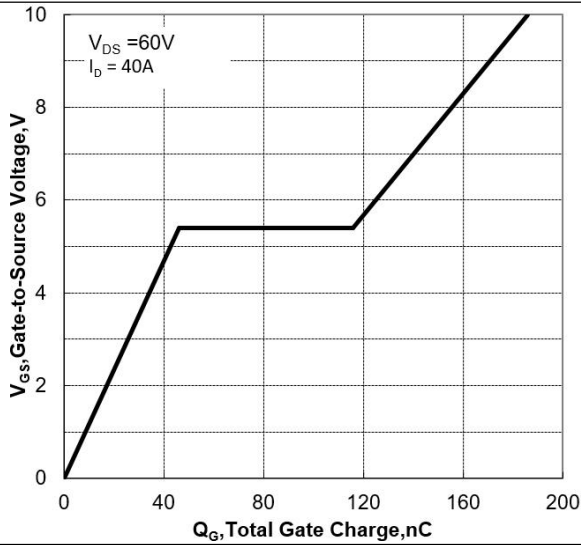


Figure 8 Capacitance Characteristics

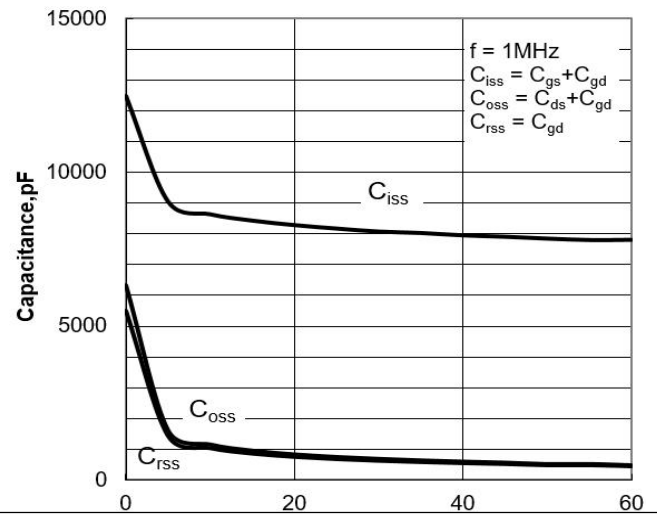


Figure 9 Maximum Forward Biased Safe Operation Area

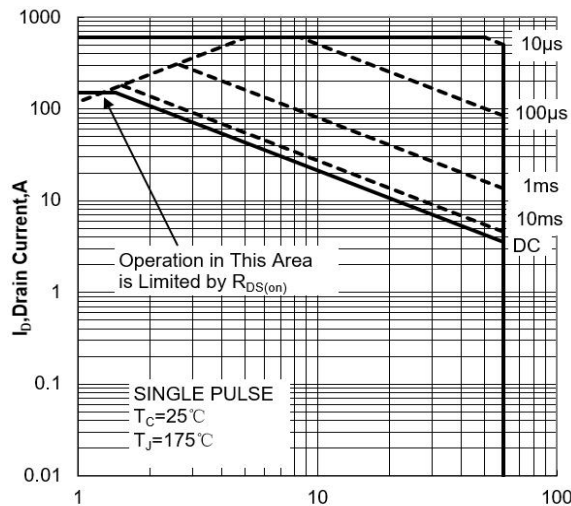


Figure 10 Single Pulse Power Rating Junction-to-Ambient

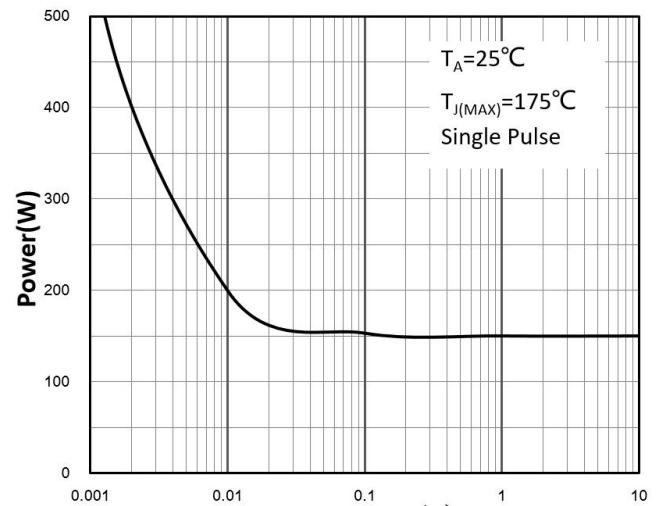
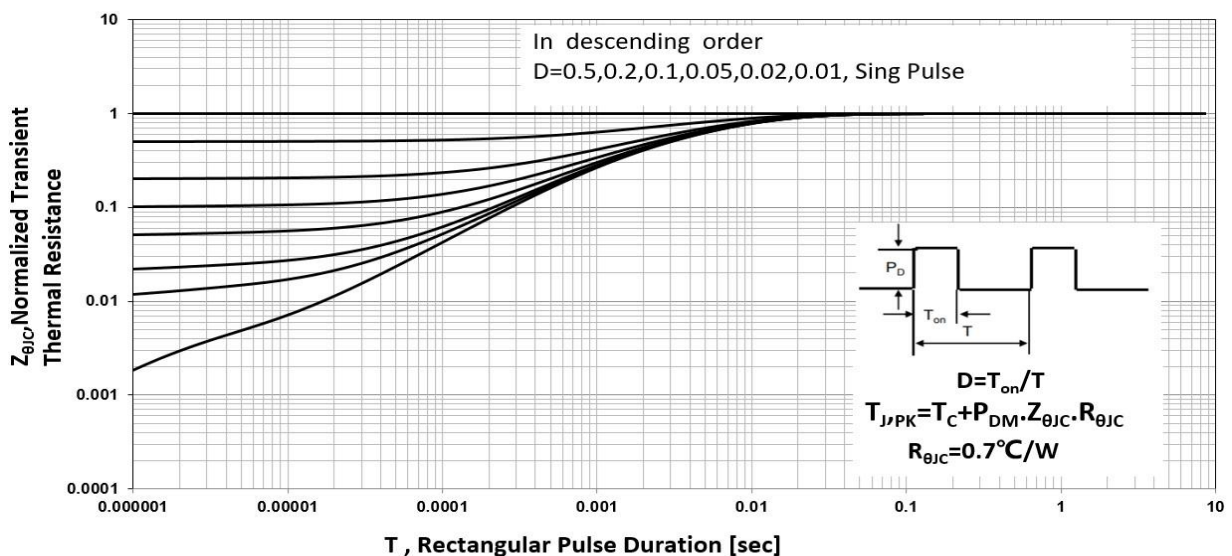
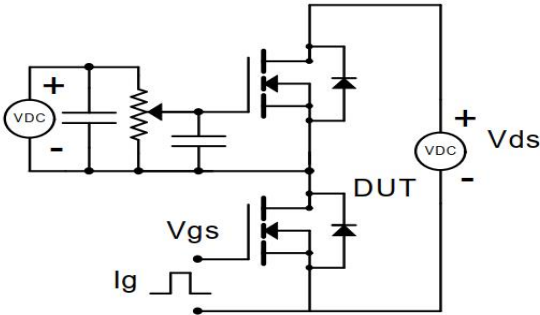
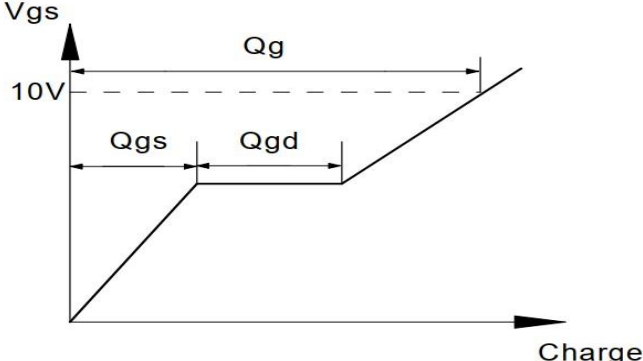
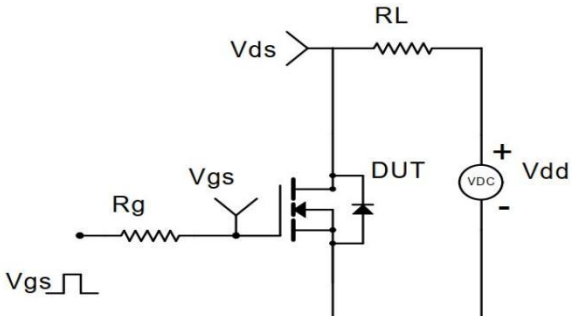
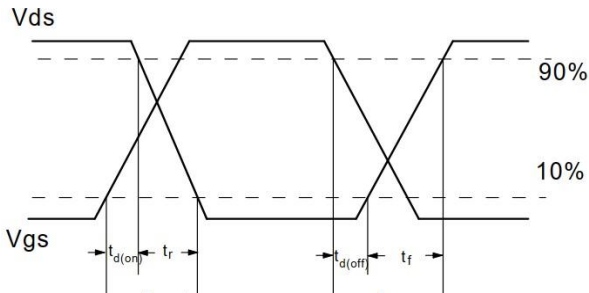
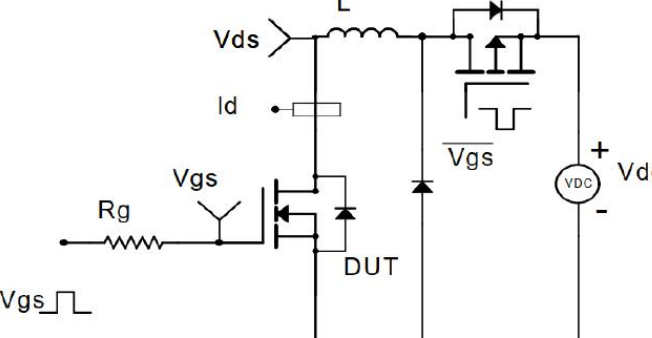
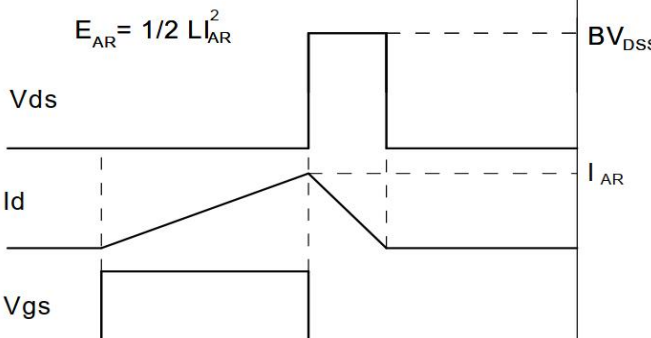
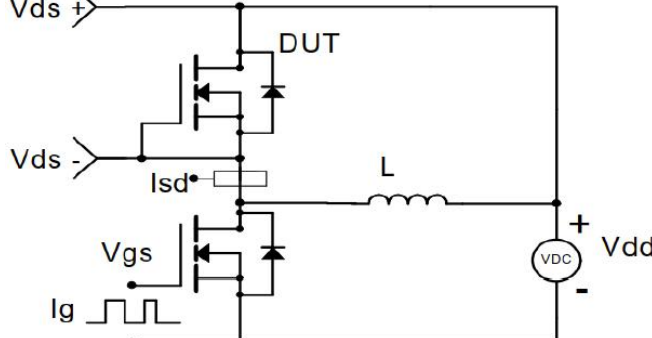
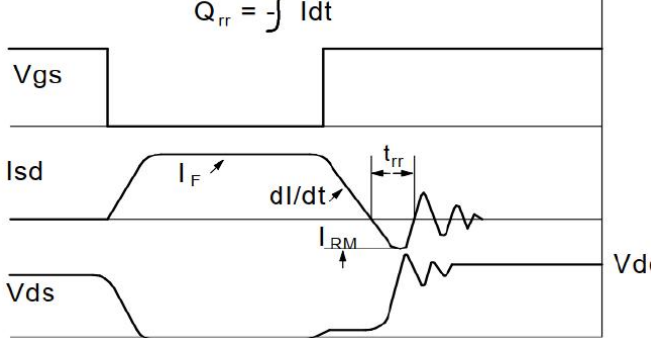


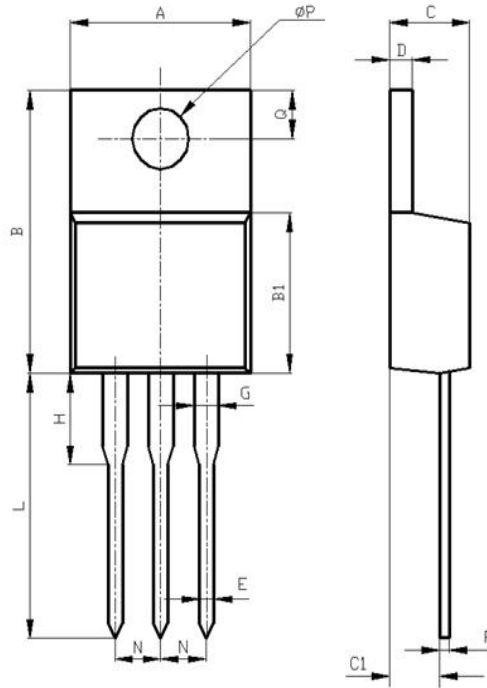
Figure 11 Normalized Maximum Transient Thermal Impedance



Test Circuit and Waveform

Gate Charge Test Circuit	Gate Charge Test Waveform
 <p>The diagram shows a MOSFET (DUT) with its gate connected to a pulse generator (Vgs) through a gate resistor (Rg). The drain is connected to a load resistor (RL) and a DC source (Vds). The source is connected to ground. A current source (Ig) is also shown connected to the gate.</p>	 <p>The graph plots Vgs (V) on the y-axis against Charge on the x-axis. The gate voltage rises linearly from 0V to 10V, then remains constant for a short duration, and then falls linearly back to 0V. The total area under the curve is labeled Qg. The area under the rising edge is Qgs, and the area under the falling edge is Qgd.</p>
Resistive Switching Test Circuit	Resistive Switching Test Waveforms
 <p>The diagram shows a MOSFET (DUT) with its gate connected to a pulse generator (Vgs) through a gate resistor (Rg). The drain is connected to a load resistor (RL) and a DC source (Vdd). The source is connected to ground.</p>	 <p>The graph shows Vds and Vgs waveforms. Vgs is a square wave. Vds is a trapezoidal wave that rises during the Vgs rise time and falls during the Vgs fall time. Key timing parameters are labeled: t_{d(on)}, t_r, t_{on}, t_{d(off)}, t_f, and t_{off}. The Vds levels are marked at 90% and 10%.</p>
Unclamped Inductive Switching (UIS) Test Circuit	Unclamped Inductive Switching (UIS) Test Waveforms
 <p>The diagram shows a MOSFET (DUT) with its gate connected to a pulse generator (Vgs) through a gate resistor (Rg). The drain is connected to an inductor (L) and a DC source (Vdd). The source is connected to ground. A diode is connected in parallel with the inductor.</p>	 <p>The graph shows Vds, Id, and Vgs waveforms. Vgs is a square wave. Id is a triangular wave that rises during the Vgs rise time and falls during the Vgs fall time. Vds is a trapezoidal wave that rises during the Id rise time and falls during the Id fall time. The peak Vds is labeled BV_{DSS}. The peak Id is labeled I_{AR}. The energy stored in the inductor is given by the equation: $E_{AR} = 1/2 L I_{AR}^2$.</p>
Diode Recovery Test Circuit	Diode Recovery Test Waveforms
 <p>The diagram shows a MOSFET (DUT) with its gate connected to a pulse generator (Vgs) through a gate resistor (Rg). The drain is connected to an inductor (L) and a DC source (Vdd). The source is connected to ground. A diode is connected in parallel with the inductor.</p>	 <p>The graph shows Vgs, Isd, and Vds waveforms. Vgs is a square wave. Isd is a trapezoidal wave that rises during the Vgs rise time and falls during the Vgs fall time. Vds is a trapezoidal wave that rises during the Isd rise time and falls during the Isd fall time. The peak Isd is labeled I_F. The peak Vds is labeled V_{RM}. The energy stored in the inductor is given by the equation: $Q_{rr} = \int Idt$.</p>

Package Description



Items	Values(mm)	
	MIN	MAX
A	9.60	10.6
B	15.0	16.0
B1	8.90	9.50
C	4.30	4.80
C1	2.30	3.10
D	1.20	1.40
E	0.70	0.90
F	0.30	0.60
G	1.17	1.37
H	2.70	3.80
L	12.6	14.8
N	2.34	2.74
Q	2.40	3.00
ϕP	3.50	3.90

TO-220 package



NOTE:

1. Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. Please do not exceed the absolute maximum ratings of the device when circuit designing.
2. When installing the heat sink, please pay attention to the torsional moment and the smoothness of the heat sink.
3. MOSFETs is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.
4. Shenzhen Minos reserves the right to make changes in this specification sheet and is subject to change without prior notice.

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