# Truesemi®

TSP50N25M
250V N-Channel MOSFET

General Description

This Power MOSFET is produced using Truesemi's advanced planar stripe DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

Features

•50A,250V,Max.RDS(on)=0.078Ω @ VGS =10V
♦ Fast switching speed
♦ Low gate charge
♦ RoHS compliant device
Applications
♦ Synchronous Rectification
♦ Power Management in Inverter System

GDS   TO-220
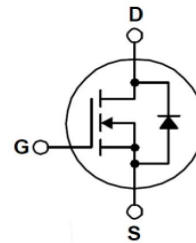
Absolute Maximum Ratings T_C=25℃ unless otherwise specified

Symbol	Parameter		Value	Units
V_{DSS}	Drain-Source Voltage		250	V
V_{GS}	Gate-Source Voltage		± 30	V
I_D	Drain Current	T_C = 25℃	50	A
		T_C = 100℃	31.6	A
I_{DM}	Pulsed Drain Current		200	A
E_{AS}	Single Pulsed Avalanche Energy (Note 1)		1250	mJ
I_{AS}	Single avalanche current		20	A
P_D	Power Dissipation (T_C = 25℃)		194	W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	℃

* Limited only maximum junction temperature

Thermal Resistance Characteristics

Symbol	Parameter	Typ.	Max.	Units
$R_{θJC}$	Thermal Resistance,Junction-to-Case	--	0.64	℃/W
$R_{θJA}$	Thermal Resistance,Junction-to-Ambient	--	62.0	℃/W

Electrical Characteristics $T_C=25\ ℃$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250$ uA	2	--	4	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 10$ V, $I_D = 25A$	--	0.065	0.078	Ω
Rg	Internal gate resistance	$V_{GS}=0V$, $V_{DS}=0V$, f=1MHz	--	0.8	--	Ω
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0$ V, $I_D = 250$ uA	250	--	--	V
I_{DSS}	Drain-source cut-off current	$V_{DS} = 250$ V, $V_{GS} = 0$ V	--	--	1	uA
I_{GSS}	Gate leakage current	$V_{DS}=0V$, $V_{GS}=\pm30V$	--	--	±100	nA
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25$ V, $V_{GS} = 0$ V, f = 1.0 MHz (Note 3,4)	--	5521	--	pF
C_{oss}	Output Capacitance		--	395	--	pF
C_{rss}	Reverse Transfer Capacitance		--	42	--	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Time	$V_{DD} = 125V$, $I_D = 50A$, $R_G = 25\ \Omega$, $V_{GS}=10V$ (Note 3,4)	--	55	--	ns
t_r	Turn-On Rise Time		--	50	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	212	--	ns
t_f	Turn-Off Fall Time		--	31	--	ns
Q_g	Total Gate Charge	$V_{DS} = 200$ V, $I_D =50A$, $V_{GS} = 10$ V (Note 3,4)	--	76	--	nC
Q_{gs}	Gate-Source Charge		--	20	--	nC
Q_{gd}	Gate-Drain Charge		--	25	--	nC
Source-Drain Diode Maximum Ratings and Characteristics						
I_S	Continuous Source-Drain Diode Forward Current		--	--	50	A
I_{SM}	Pulsed Source-Drain Diode Forward Current		--	--	200	A
V_{SD}	Source-Drain Diode Forward Voltage	$I_{SD} =50A$, $V_{GS} = 0$ V	--	--	1.2	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 50A$, $V_{GS} = 0$ V $di_F/dt = 100$ A/µs (Note 3,4)	--	271	--	ns
Q_{rr}	Reverse Recovery Charge		--	2.4	--	uC

NOTES:

1. L=5mH, IAS=20 VDD=50V, Starting TJ=25◇C

2. Pulse test: Pulse width≤300us, Duty cycle≤2%

3. Essentially independent of operating temperature typical characteristics

4. Guaranteed by design, not subject to production testing.

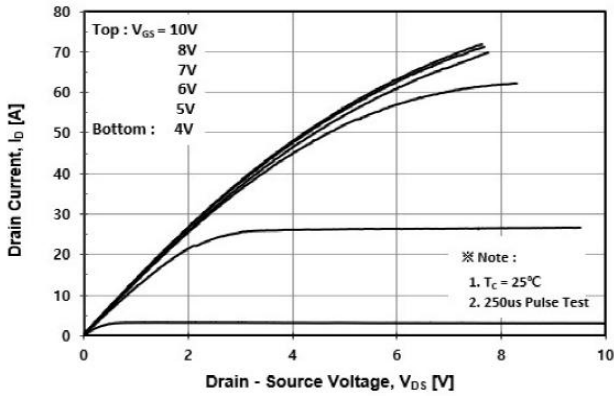# Typical Electrical Characteristics Curves

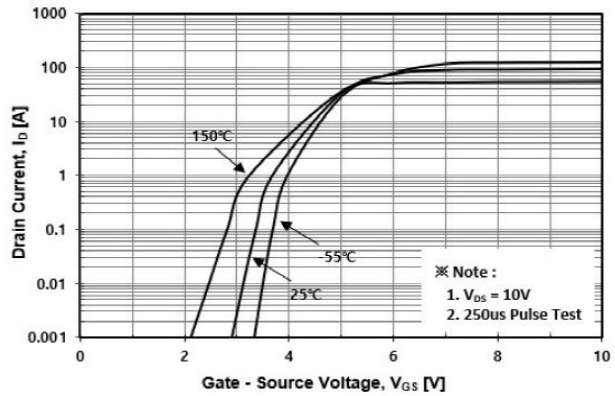### Fig. 1 I_D - V_{DS}
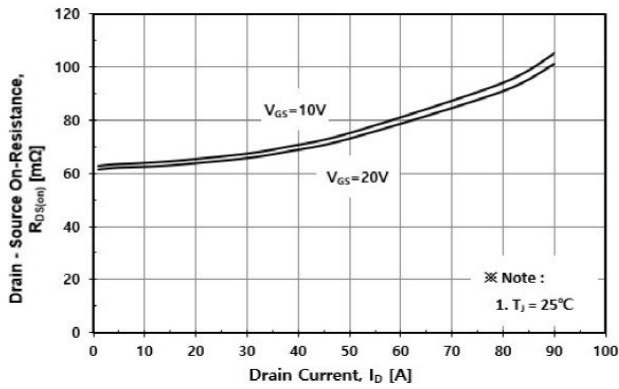
Top : V_{GS} = 10V
8V
7V
6V
5V
Bottom : 4V

※ Note :
1. T_C = 25℃
2. 250us Pulse Test

Fig. 2 I_D - V_{GS}

150℃
-55℃
25℃

※ Note :
1. V_{DS} = 10V
2. 250us Pulse Test

Fig. 3 $R_{DS(ON)}$ - I_D

V_{GS}=10V
V_{GS}=20V

※ Note :
1. T_J = 25℃

Fig. 4 I_S - V_{SD}

※ Note :
1. V_{GS} = 0V
2. T_J=25℃
3. 250us Pulse Test

Fig. 5 Capacitance - V_{DS}

Ciss
Coss
Crss

※ Note :
1. V_{GS} = 0V
2. f = 1MHz

Fig. 6 V_{GS} - Q_G

※ Note :
1. V_{DS}= 200V
2. I_D = 50A
3. V_{GS} = 10V
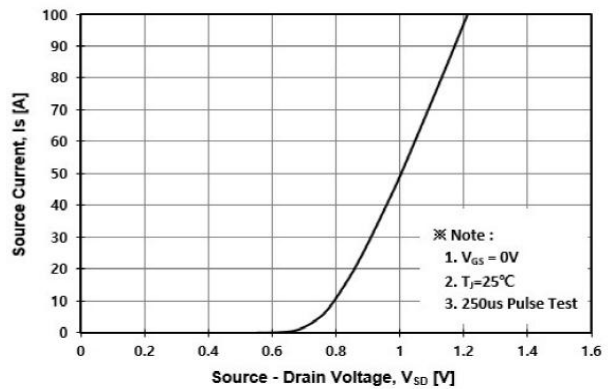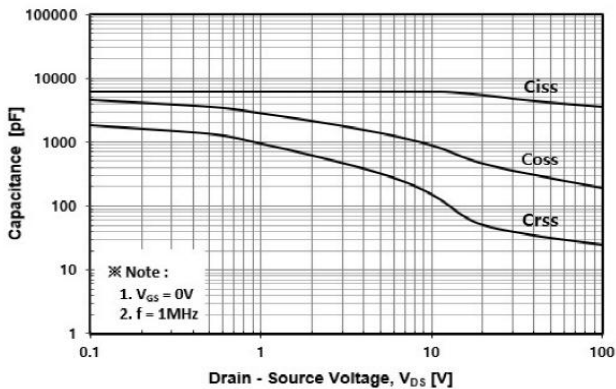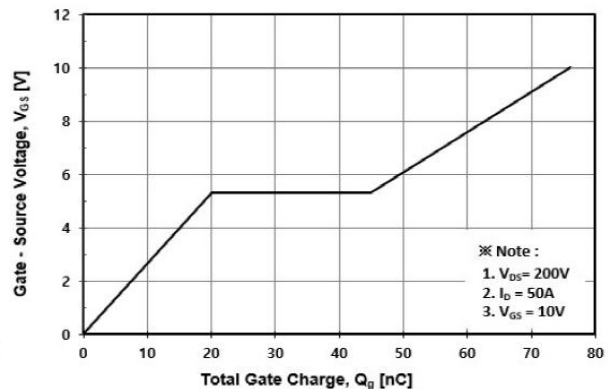
Typical Electrical Characteristics Curves

Fig. 7 BV$_{DSS}$ - T$_J$

※ Note :
1. V$_{GS}$ = 0V
2. I$_{DS}$ = 250uA

Fig. 8 R$_{DS(ON)}$ - T$_J$

※ Note :
1. V$_{GS}$ = 10V
2. I$_D$ = 25A
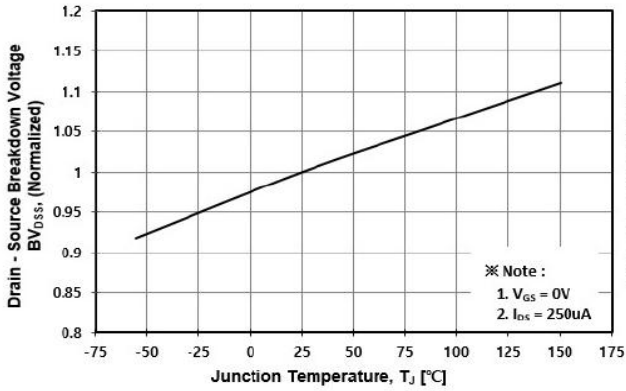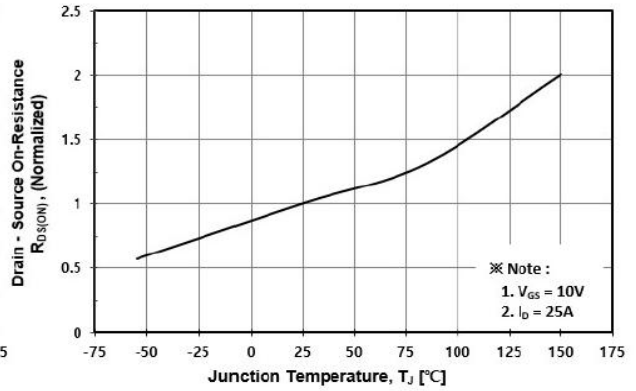
Fig. 9 I$_D$ - T$_C$
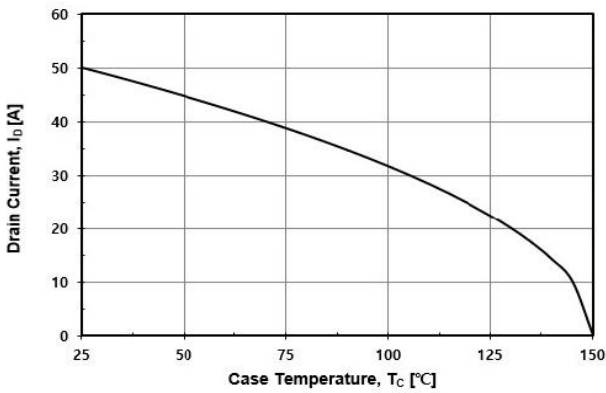
Fig. 10 Safe Operating Area

Operation in This Area is Limited by R$_{DS(on)}$

※ Note :
1. T$_C$ = 25℃
2. T$_J$ = 150℃
3. Single Pulse
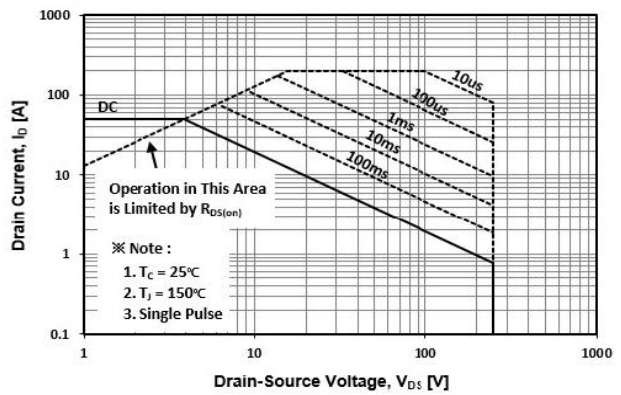
Fig. 11 Transient Thermal Impedance

Single Pulse
δ=0.01
δ=0.02
δ=0.05
δ=0.1
δ=0.2
δ=0.5

※ Note :
1. Z$_{θJC}$(t) = 0.64℃/W Max.
2. Duty Factor, δ = t1 / t2
3. T$_{JM}$ - T$_C$ = P$_{DM}$ x Z$_{θJC}$(t)

Ver.B1
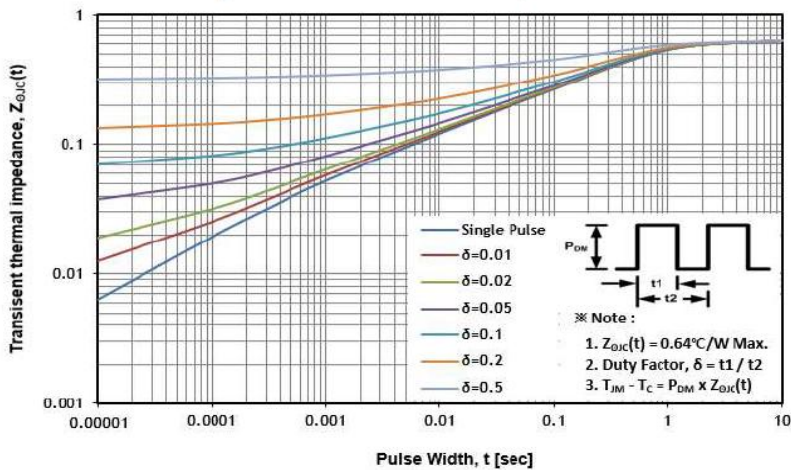
Fig. 12 Gate Charge Test Circuit & Waveform

Current Regulator

Same Type as DUT

12V
50KΩ
200nF
300nF
VDS
VGS
R1
R2
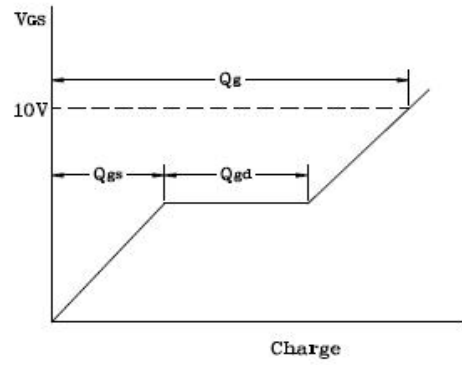Current Sampling (IG) Resistor
Current Sampling (ID) Resistor

VGS
10V
Qg
Qgs
Qgd
Charge
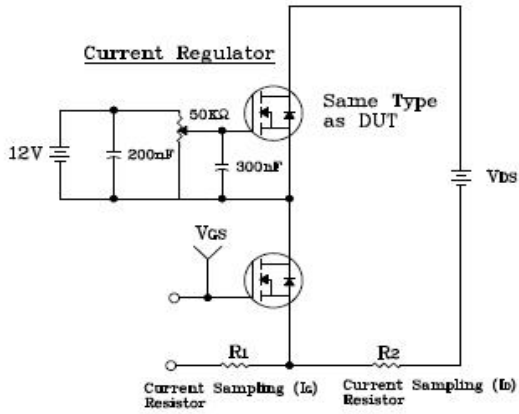
Fig. 13 Resistive Switching Test Circuit & Waveform

Vout
R1
VDD
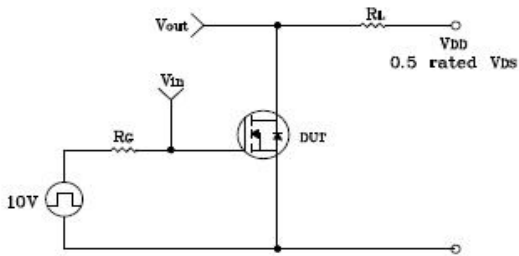0.5 rated VDS
Vin
RG
DUT
10V

Vout
90%
Vin
10%
td(on)
tr
ton
td(off)
tf
toff
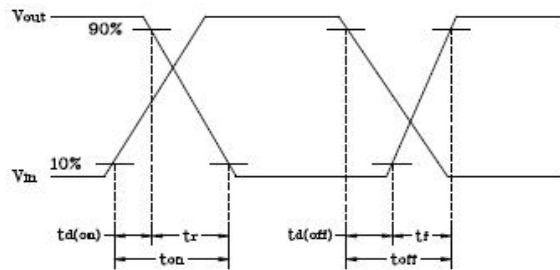
Fig. 14 E$_{AS}$ Test Circuit & Waveform

VDS
LL
ID
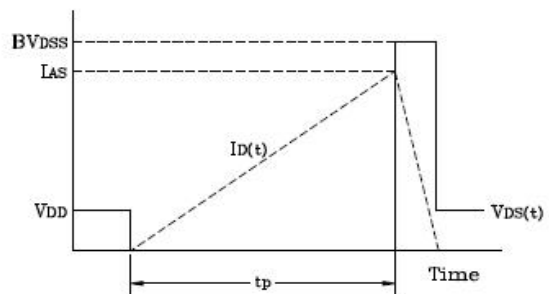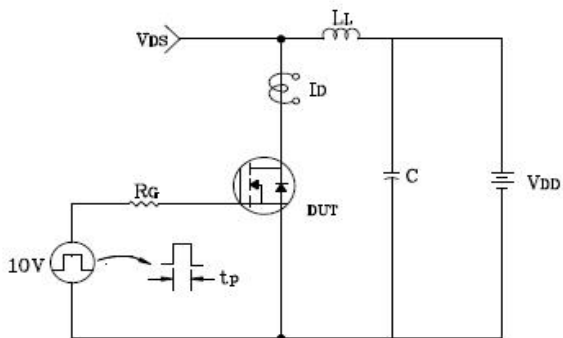RG
DUT
C
VDD
10V
tp

BVDSS
IAS
ID(t)
VDD
VDS(t)
tp
Time

Fig. 15 Diode Reverse Recovery Time Test Circuit & Waveform

$$D = \frac{Gate\ Pulse\ Width}{Gate\ Pulse\ Period}$$

Fig. 15 Diode Reverse Recovery Time Test Circuit & Waveform