

TSA12N90M

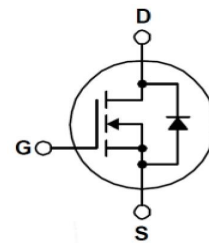
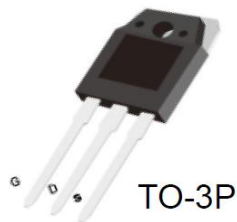
900V N-Channel MOSFET

General Description

This Power MOSFET is produced using Truesemi's advanced planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

Features

- 12A,900V,Max.RDS(on)=1.1Ω @ VGS =10V
- Low gate charge: Qg=83nC (Typ.)
- 100% avalanche tested
- RoHS compliant device



Absolute Maximum Ratings T_c=25°C unless otherwise specified

Symbol	Parameter	Value	Units
V _{DSS}	Drain-Source Voltage	900	V
V _{GS}	Gate-Source Voltage	± 30	V
I _D	Drain Current	T _C = 25°C	12
		T _C = 100°C	8.0
I _{DM}	Pulsed Drain Current *	48	A
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	238	mJ
I _{AS}	Repetitive avalanche current (Note 2)	15	A
E _{AR}	Repetitive Avalanche Energy (Note 1)	15.6	mJ
P _D	Power Dissipation (T _C = 25°C)	156	W
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +150	°C

* Limited only maximum junction temperature

Thermal Resistance Characteristics

Symbol	Parameter	Typ.	Max.	Units
R _{θJC}	Thermal Resistance, Junction-to-Case	--	0.80	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient	--	62.5	°C/W

Electrical Characteristics $T_c=25\text{ }^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3.0	--	5.0	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 5.5\text{ A}$	--	0.86	1.10	Ω
R_g	Internal gate resistance	Open drain, $f=1\text{ MHz}$	--	1	--	Ω

Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	900	--	--	V
I_{DSS}	Drain-source cut-off current	$V_{DS} = 900\text{ V}, V_{GS} = 0\text{ V}$	--	--	10	μA
		$V_{DS} = 900\text{ V}, T_c = 125\text{ }^\circ\text{C}$	--	--	100	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	2900	--	pF
C_{oss}	Output Capacitance		--	210	--	pF
C_{rss}	Reverse Transfer Capacitance		--	32	--	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Time	$V_{DD} = 450\text{ V}, I_D = 12\text{ A},$ $R_G = 25\text{ }\Omega$ (Note 3,4)	--	66	--	ns
t_r	Turn-On Rise Time		--	63	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	195	--	ns
t_f	Turn-Off Fall Time		--	74	--	ns
Q_g	Total Gate Charge	$V_{DS} = 720\text{ V}, I_D = 12\text{ A},$ $V_{GS} = 10\text{ V}$ (Note 3,4)	--	83	--	nC
Q_{gs}	Gate-Source Charge		--	15	--	nC
Q_{gd}	Gate-Drain Charge		--	42	--	nC

Source-Drain Diode Maximum Ratings and Characteristics

I_S	Continuous Source-Drain Diode Forward Current		--	--	12	A
I_{SM}	Pulsed Source-Drain Diode Forward Current		--	--	33	
V_{SD}	Source-Drain Diode Forward Voltage	$I_S = 12\text{ A}, V_{GS} = 0\text{ V}$	--	--	1.5	V
t_{rr}	Reverse Recovery Time	$I_S = 12\text{ A}, V_{GS} = 0\text{ V}$ $di_p/dt = 100\text{ A}/\mu\text{s}$ (Note 3, 4)	--	920	--	ns
Q_{rr}	Reverse Recovery Charge		--	7.2	--	μC

NOTES:

1. Repeated rating: Pulse width limited by safe operating area
2. $L=2\text{ mH}, I_{AS}=15\text{ A}, V_{DD}=50\text{ V}, R_G=25\text{ }\Omega$, Starting $T_J=25\text{ }^\circ\text{C}$
3. Pulse test: Pulse width $\leq 300\text{ }\mu\text{s}$, Duty cycle $\leq 2\%$
4. Essentially Independent of Operating Temperature Typical Characteristics

Typical Characteristics

Fig. 1 $I_D - V_{DS}$

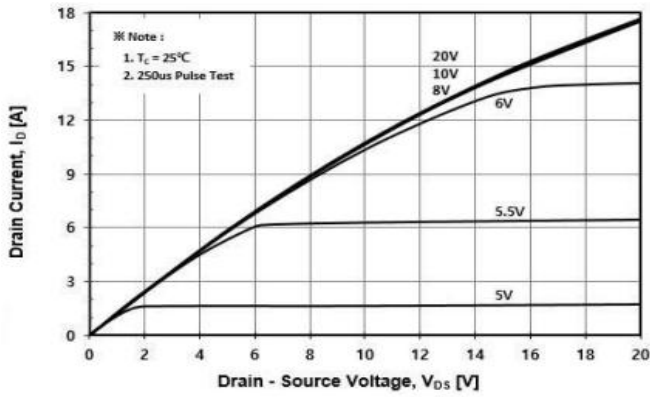


Fig. 2 $I_D - V_{GS}$

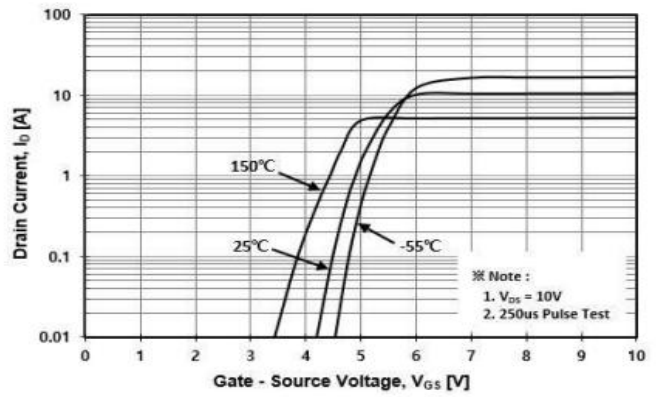


Fig. 3 $R_{DS(ON)} - I_D$

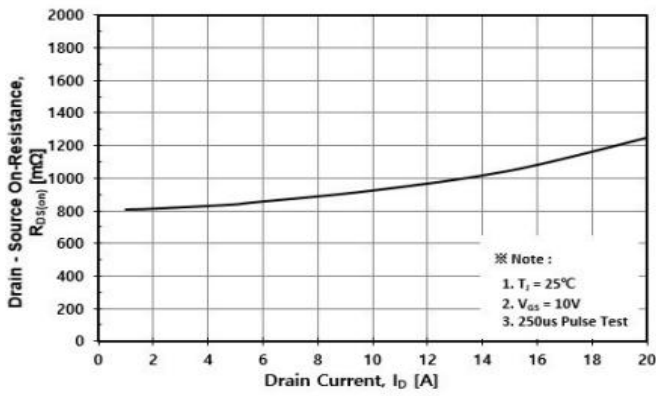


Fig. 4 $I_S - V_{SD}$

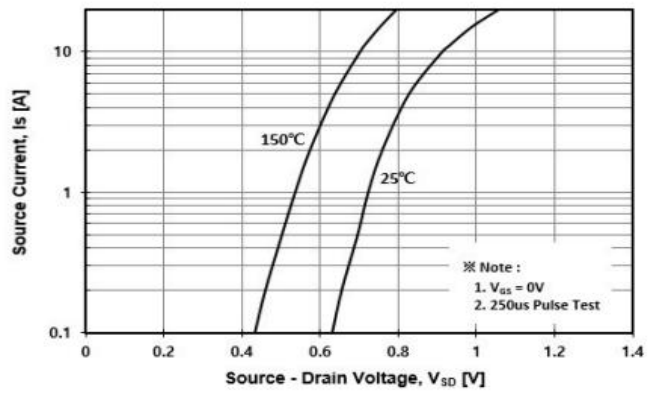


Fig. 5 Capacitance - V_{DS}

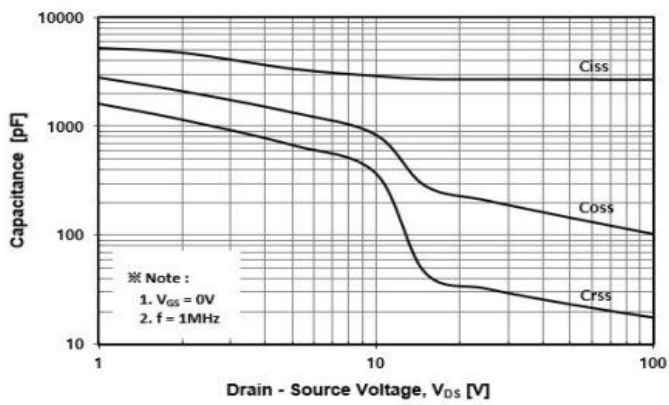
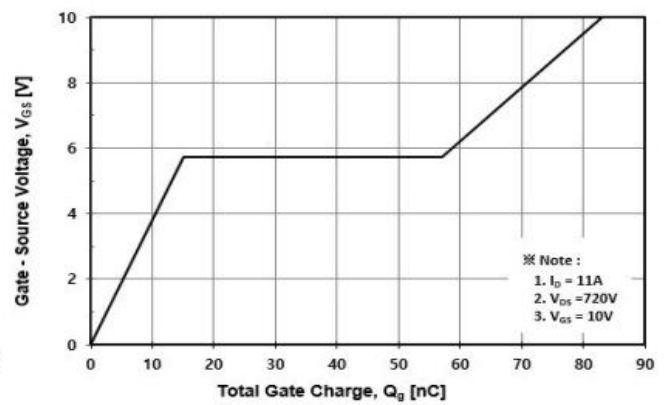


Fig. 6 $V_{GS} - Q_G$



Typical Characteristics Curve (Continue)

Fig. 7 $BV_{DSS} - T_J$

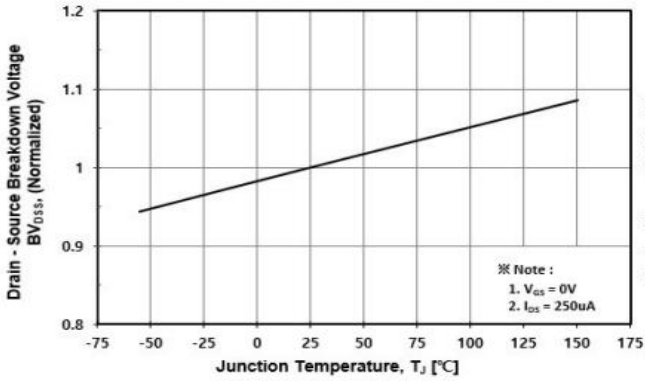


Fig. 8 $R_{DS(ON)} - T_J$

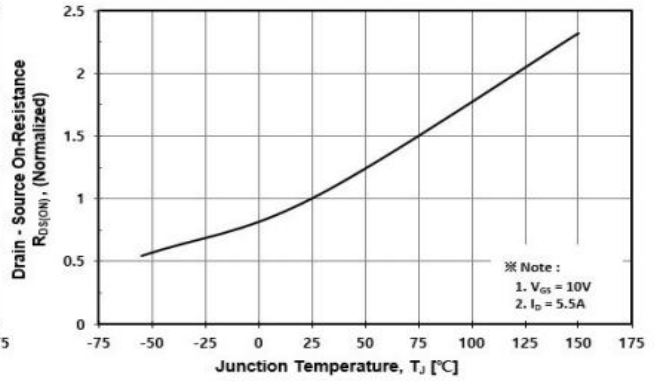


Fig. 9 $I_D - T_C$

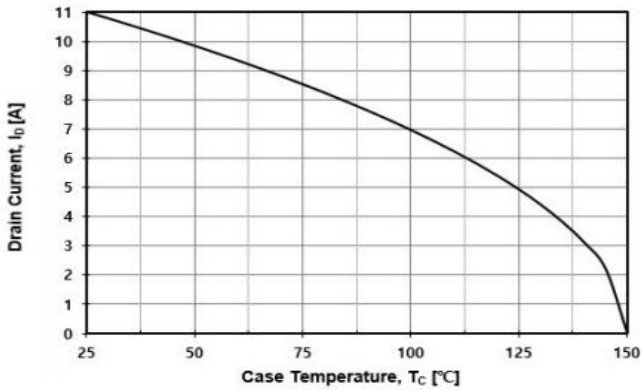


Fig. 10 Safe Operating Area

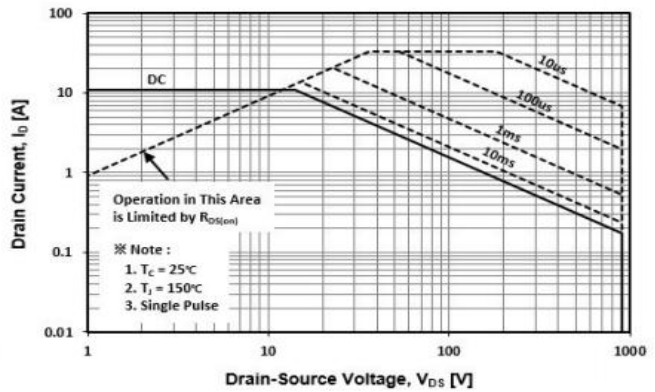


Fig. 11 Transient Thermal Impedance

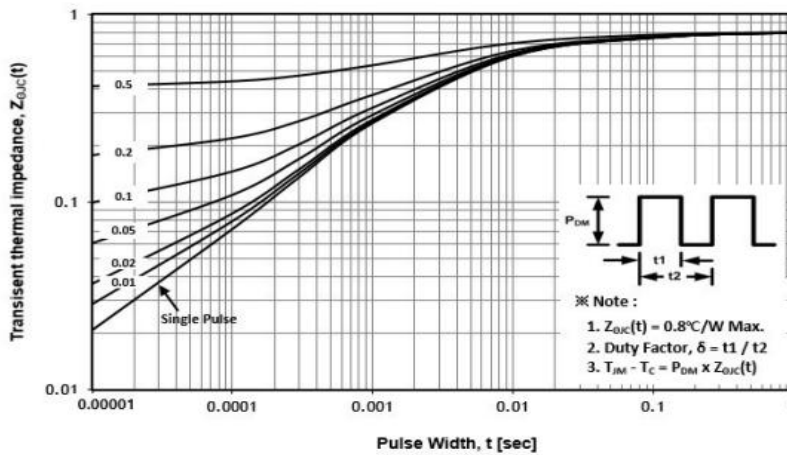


Fig. 12 Gate Charge Test Circuit & Waveform

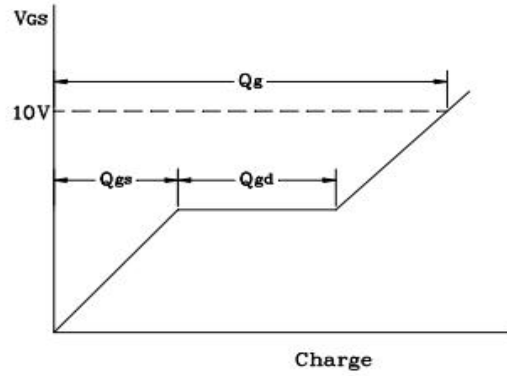
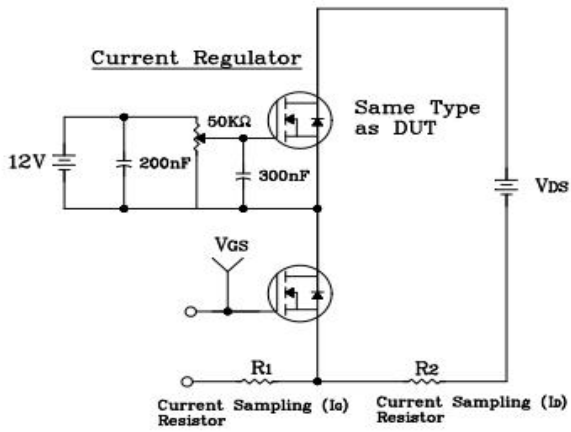


Fig. 13 Resistive Switching Test Circuit & Waveform

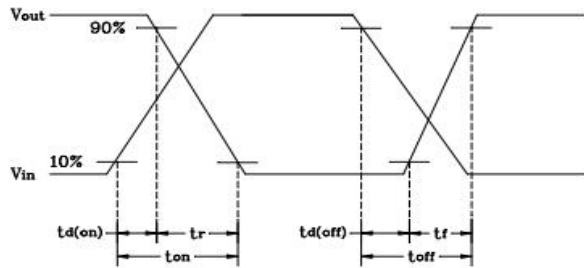
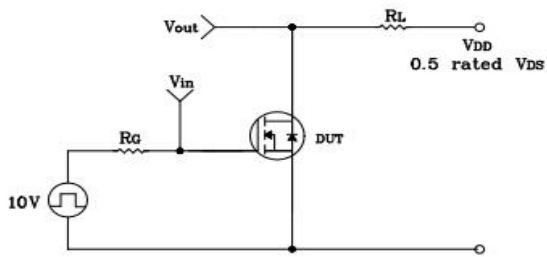


Fig. 14 EAS Test Circuit & Waveform

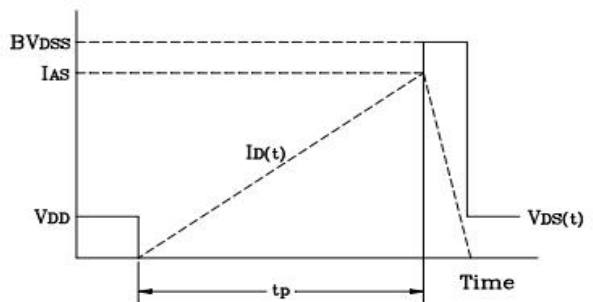
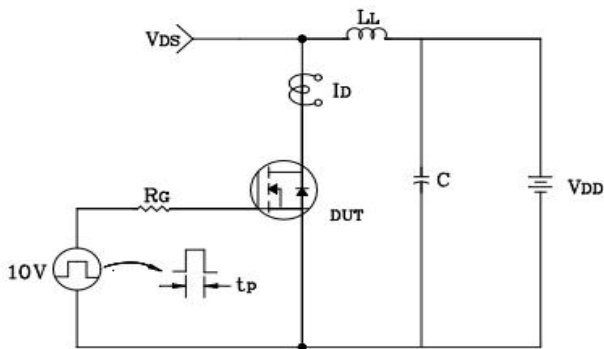


Fig. 15 Diode Reverse Recovery Time Test Circuit & Waveform

