

**9XXX Series**

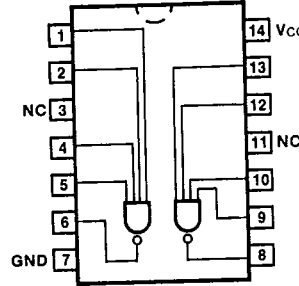
**9009  
NAND BUFFER**

**CONNECTION DIAGRAM  
PINOUT A**

*T-43-15*

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0\text{ V}, \pm 5\%$ , $T_A = 0^\circ\text{C to } +75^\circ\text{C}$	$V_{CC} = +5.0\text{ V} \pm 10\%$ , $T_A = -55^\circ\text{C to } +125^\circ\text{C}$	
Ceramic DIP (D)	A	9009DC	9009DM	6A
Flatpak (F)	A	9009FC	9009FM	3I



$V_{CC} = \text{Pin } 14$   
 $GND = \text{Pin } 7$

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	9XXX (U.L.) HIGH/LOW
Inputs	3.0/2.0
Outputs	90/26 (99)/(25.5)

**DC AND AC CHARACTERISTICS OVER COMMERCIAL TEMPERATURE RANGE:  $V_{CC} = +5.0\text{ V} \pm 5\%$**

SYMBOL	PARAMETER	0°C		25°C		75°C		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
$V_{IH}$	Input HIGH Voltage	1.9		1.8		1.6		V	Guaranteed Input HIGH Threshold
$V_{IL}$	Input LOW Voltage		0.85		0.85		0.85	V	Guaranteed Input LOW Threshold
$V_{OL}$	Output LOW Voltage		0.45		0.45		0.45	V	$V_{CC} = 5.25\text{ V}$ , $I_{OL} = 48\text{ mA}$ , $V_{IN} = 5.25\text{ V}$
									$V_{CC} = 4.75\text{ V}$ , $I_{OL} = 42.3\text{ mA}$ , Inputs at $V_{IH}$
$I_{IH}$	Input HIGH Current				120		120	$\mu\text{A}$	$V_{CC} = 5.25\text{ V}$ , $V_{IN} = 4.5\text{ V}$ Gnd on Other Inputs
$I_{IL}$	Input LOW Current		-3.2		-3.2		-3.2	mA	$V_{CC} = 5.25\text{ V}$ , $V_{IN} = .45\text{ V}$ 5.25 V on Other Inputs
			-2.82		-2.82		-2.82		$V_{CC} = 4.75\text{ V}$ , $V_{IN} = .45\text{ V}$ 5.25 V on Other Inputs
$I_{CCH}$ $I_{CCL}$	Power Supply Current (each gate)	ON	14.6		14.6		14.6	mA	$V_{IN} = \text{Open}$
		OFF	3.4		3.4		3.4		$V_{IN} = \text{Gnd}$
$t_{PLH}$ $t_{PHL}$	Propagation Delay			3.0	17			ns	Figs. 3-1, 3-4 $C_L = 15\text{ pF}$
				2.0	13				

**9XXX Series**

*T-43-15*

DC AND AC CHARACTERISTICS OVER MILITARY TEMPERATURE RANGE:  $V_{CC} = +5.0 V \pm 10\%$

SYMBOL	PARAMETER	-55°C		25°C		125°C		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
$V_{IH}$	Input HIGH Voltage	2.0		1.7		1.4		V	Guaranteed Input HIGH Threshold
$V_{IL}$	Input LOW Voltage		0.8		0.9		0.8	V	Guaranteed Input LOW Threshold
$V_{OL}$	Output LOW Voltage		0.4		0.4		0.4	V	$V_{CC} = 5.5 V$ , $I_{OL} = 52.8 mA$ $V_{IN} = 5.5 V$
									$V_{CC} = 4.5 V$ , $I_{OL} = 40.8 mA$ , Inputs at $V_{IH}$
$I_{IH}$	Input HIGH Current				120		120	$\mu A$	$V_{CC} = 5.5 V$ , $V_{IN} = 4.5 V$ Gnd on Other Inputs
$I_{IL}$	Input LOW Current		-3.2		-3.2		-3.2	mA	$V_{CC} = 5.5 V$ $V_{IN} = 0.4 V$ 5.5 V on Other Inputs
			-2.48		-2.48		-2.48		$V_{CC} = 4.5 V$ $V_{IN} = 0.4 V$ 5.5 V on Other Inputs
$I_{CCH}$ $I_{CCL}$	Power Supply Current (each gate)	ON	12.9		12.9		12.9	mA	$V_{IN} = \text{Open}$
		OFF	3.2		3.2		3.2		$V_{IN} = \text{Gnd}$
$t_{PLH}$ $t_{PHL}$	Propagation Delay			4.0 3.0	15 10			ns	Figs. 3-1, 3-4 $C_L = 15 pF$