

# TIBPALT19L8C, TIBPALT19R4C, TIBPALT19R6C, TIBPALT19R8C HIGH-PERFORMANCE LATCHED-INPUT PAL® CIRCUITS

D2709, DECEMBER 1982 - REVISED AUGUST 1989

- High-Performance Operation . . . 30 MHz
- Preload Capability on Output Registers
- DIP Options Include Both 300-mil Plastic and 600-mil Ceramic
- Dependable Texas Instruments Quality and Reliability

DEVICE	I/D INPUTS	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
'PALT19L8	11	2	2	0	6
'PALT19R4	11	0	0	4 (3-state buffers)	4
'PALT19R6	11	0	0	6 (3-state buffers)	2
'PALT19R8	11	0	0	8 (3-state buffers)	0

## description

These programmable array logic devices feature high speed and functionality similar to the TIBPAL16L8, 16R4, 16R6, 16R8 series, but with the added advantage of D-type transparent latches on the inputs. If any input register is not desired, it can be converted to an input buffer by simply programming the architectural fuse.

Combining Advanced Low-Power Schottky† technology, with proven titanium-tungsten fuses, these devices will provide reliable high performance substitutes over conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically result in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

Extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

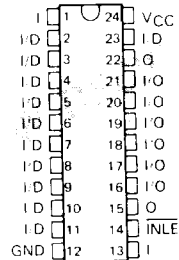
A C suffix designates commercial-temperature circuits that are characterized for operation from 0°C to 70°C.

INPUT LATCH FUNCTION TABLE

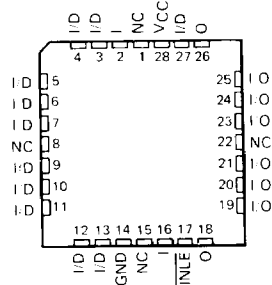
INLE	D	LATCH OUTPUT
L	L	L
L	H	H
H	X	Q <sub>0</sub>

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.  
PAL is a trademark of Monolithic Memories Inc.

TIBPALT19L8'  
JW OR NT PACKAGE  
(TOP VIEW)



TIBPALT19L8'  
FN PACKAGE  
(TOP VIEW)

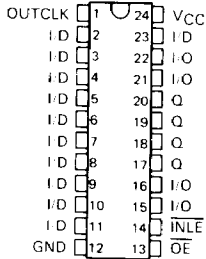


NC No internal connection

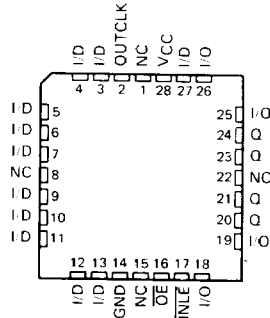
Pin assignments in operating mode

# TIBPALT19R4C, TIBPALT19R6C, TIBPALT19R8C HIGH-PERFORMANCE LATCHED-INPUT PAL® CIRCUITS

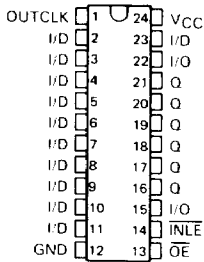
**TIBPALT19R4'**  
JW OR NT PACKAGE  
(TOP VIEW)



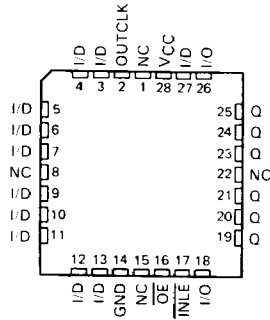
**TIBPALT19R4'**  
FN PACKAGE  
(TOP VIEW)



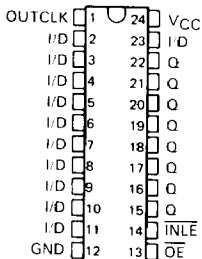
**TIBPALT19R6'**  
JW OR NT PACKAGE  
(TOP VIEW)



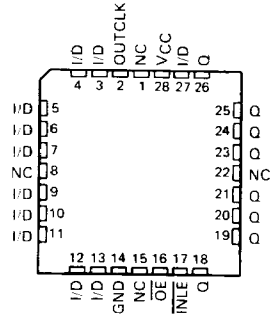
**TIBPALT19R6'**  
FN PACKAGE  
(TOP VIEW)



**TIBPALT19R8'**  
JW OR NT PACKAGE  
(TOP VIEW)



**TIBPALT19R8'**  
FN PACKAGE  
(TOP VIEW)

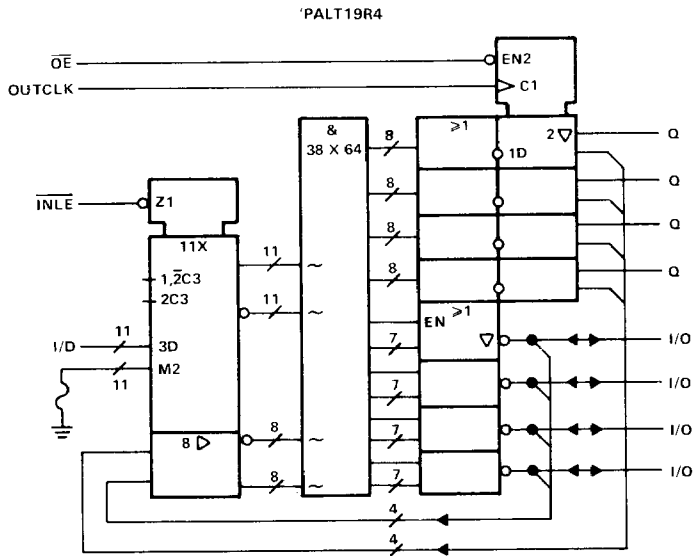
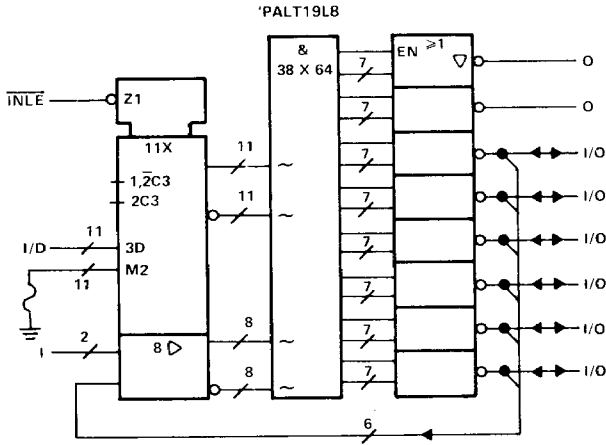


Pin assignments in operating mode

NC — No internal connection

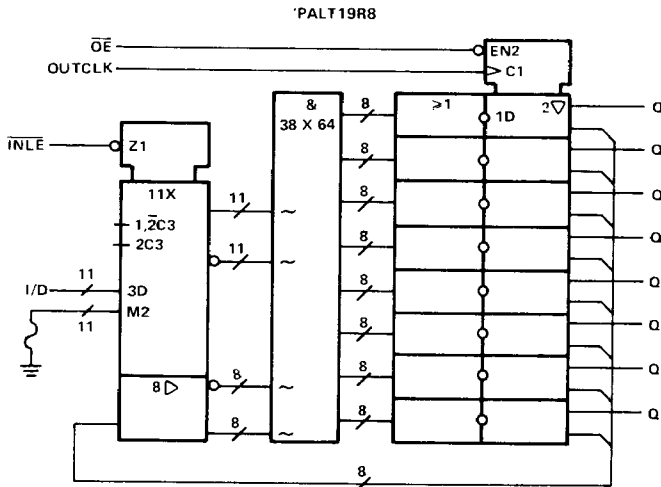
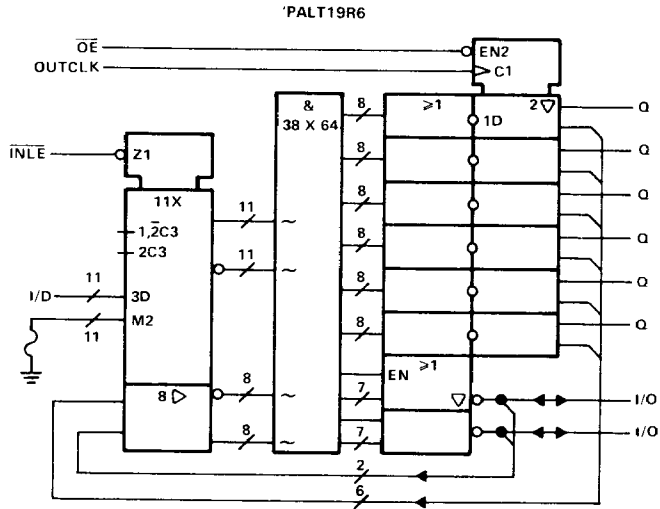
# TIBPALT19L8C, TIBPALT19R4C HIGH-PERFORMANCE LATCHED-INPUT PAL® CIRCUITS

functional block diagrams (positive logic)



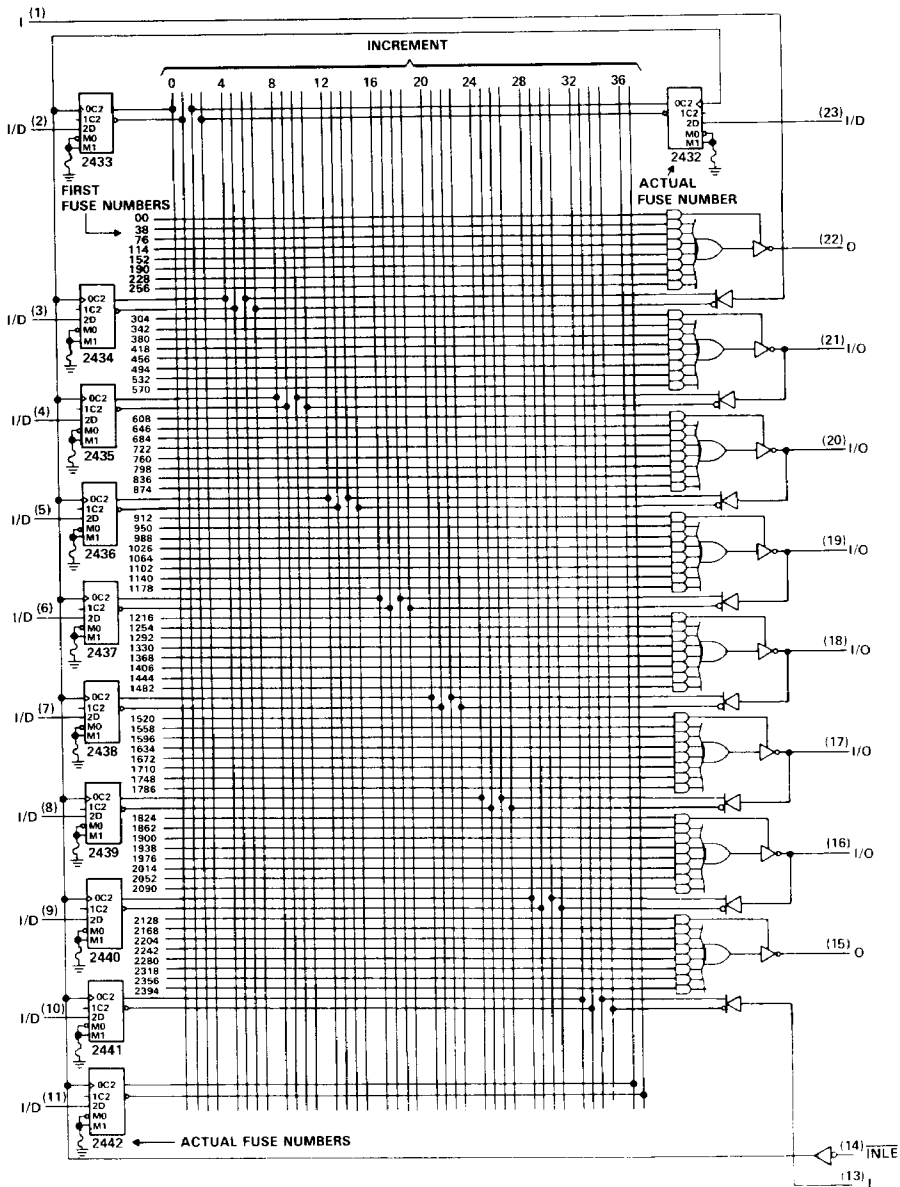
**TIBPALT19R6C, TIBPALT19R8C**  
**HIGH-PERFORMANCE LATCHED-INPUT PAL® CIRCUITS**

functional block diagrams (positive logic)



# TIBPALT19L8C HIGH-PERFORMANCE LATCHED-INPUT PAL® CIRCUITS

logic diagram (positive logic)

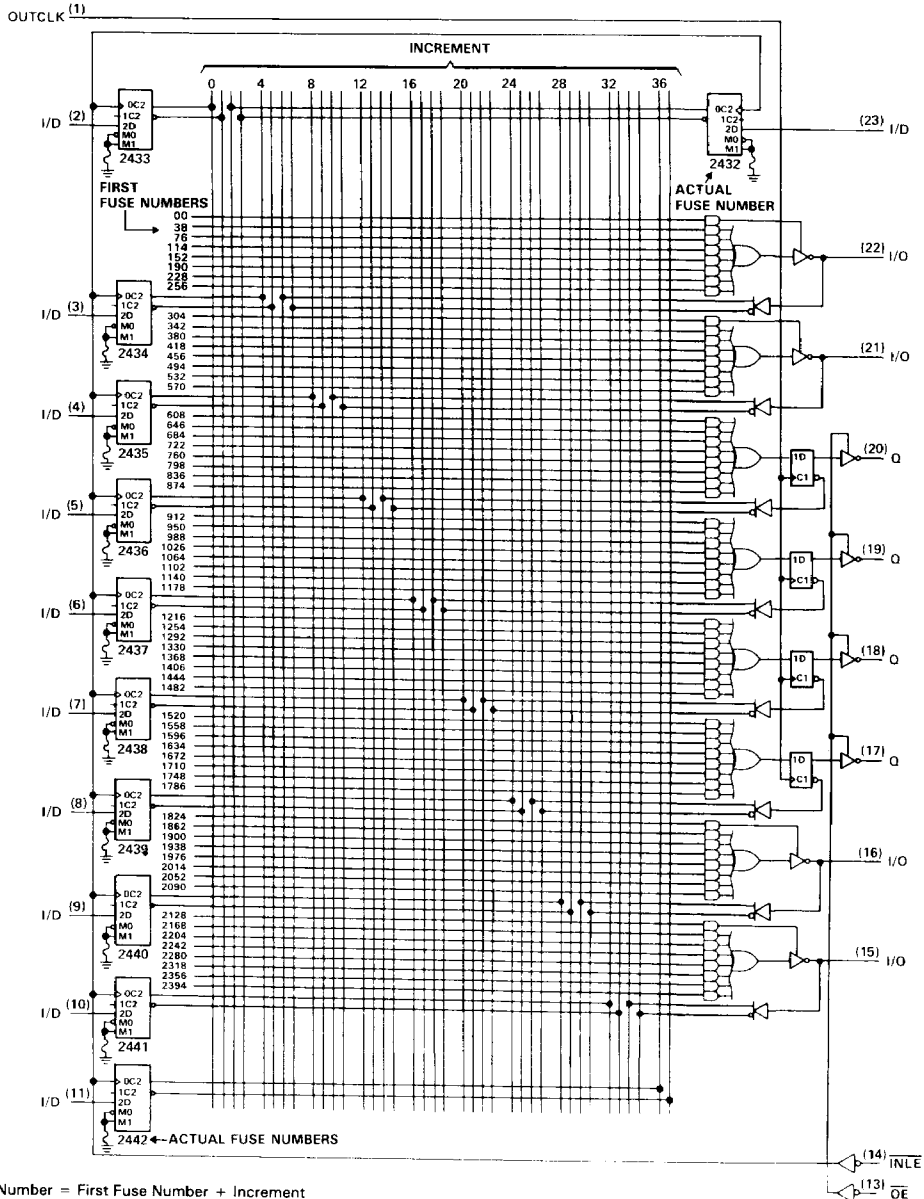


Fuse Number = First Fuse Number + Increment  
Pin numbers shown are for JW and NT packages.

# TIBPALT19R4C

## HIGH-PERFORMANCE LATCHED-INPUT PAL® CIRCUITS

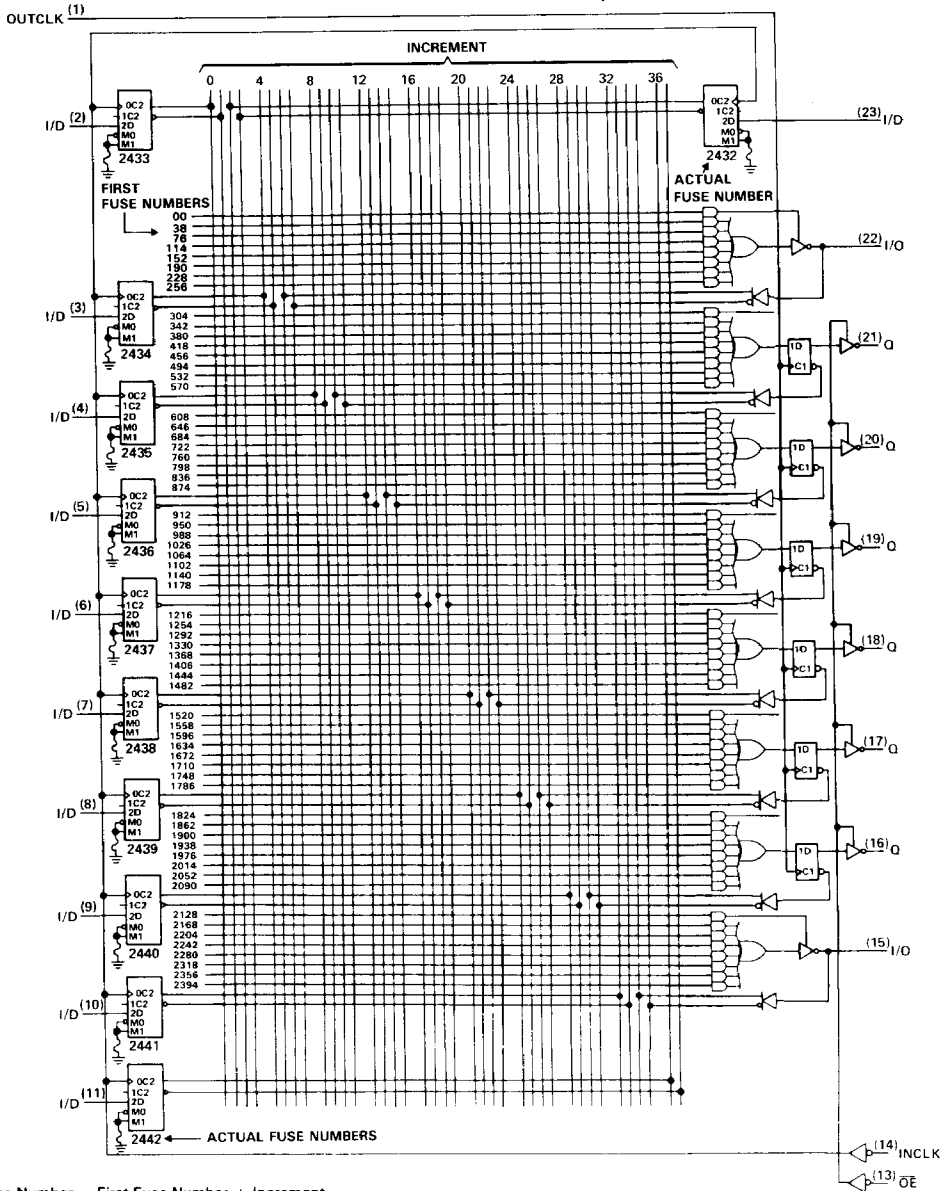
logic diagram (positive logic)



Fuse Number = First Fuse Number + Increment  
 Pin numbers shown are for JW and NT packages.

# TIBPALT19R6C HIGH-PERFORMANCE LATCHED-INPUT PAL® CIRCUITS

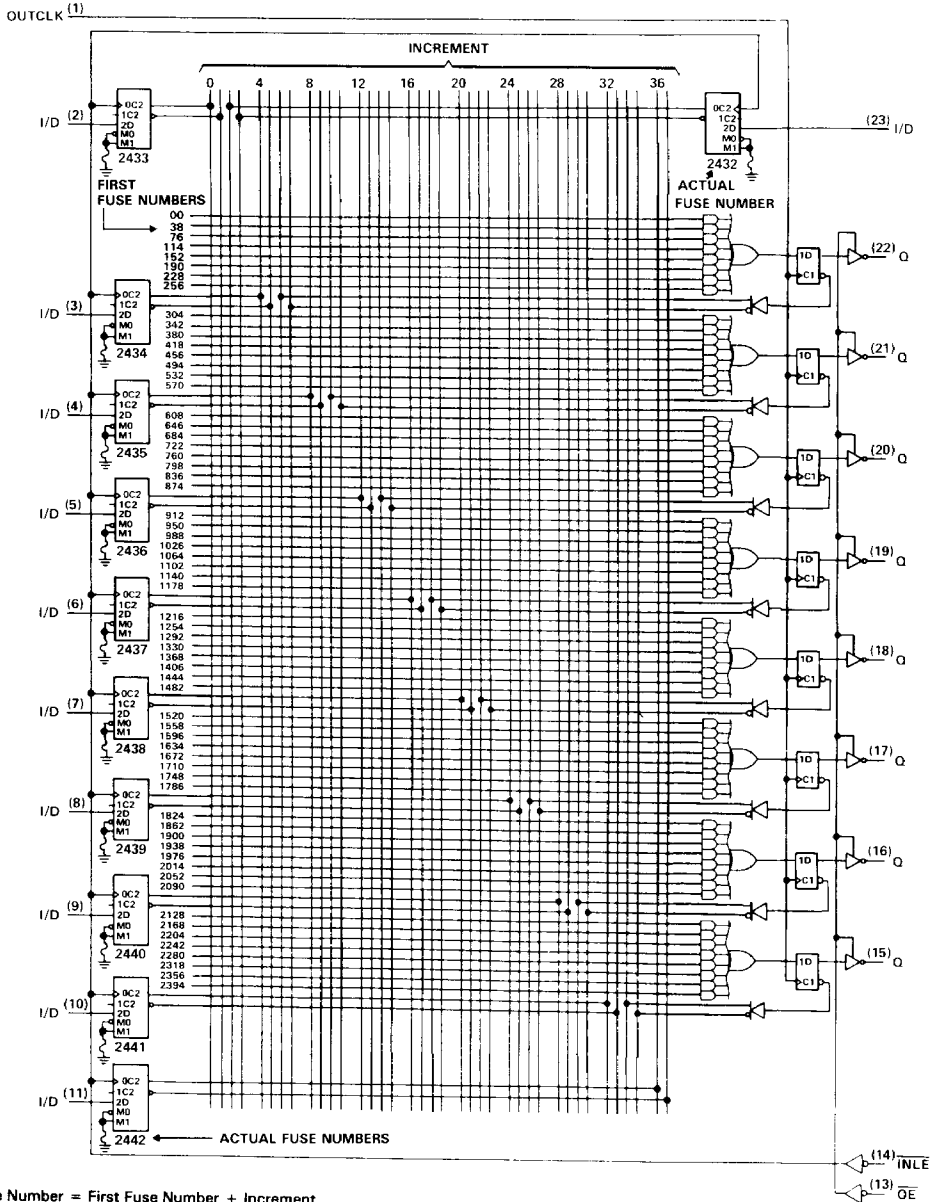
logic diagram (positive logic)



Fuse Number = First Fuse Number + Increment  
Pin numbers shown are for JW and NT packages.

# TIBPALT19R8C HIGH-PERFORMANCE LATCHED-INPUT PAL® CIRCUITS

logic diagram (positive logic)





# TIBPALT19L8C, TIBPALT19R4C, TIBPALT19R6C, TIBPALT19R8C HIGH-PERFORMANCE LATCHED-INPUT PAL® CIRCUITS

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) .....	7 V
Input voltage (see Note 1) .....	5.5 V
Voltage applied to a disabled output (see Note 1) .....	5.5 V
Operating free-air temperature range .....	0°C to 70°C
Storage temperature range .....	-65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during preload cycle.

## recommended operating conditions

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.75	5	5.25	V
$V_{IH}$	High-level input voltage	2		5.5	V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{OH}$	High-level output current			-3.2	mA
$I_{OL}$	Low-level output current			24	mA
$f_{clock}$	Clock frequency	0		30	MHz
$t_w$	Pulse duration	OUTCLK			ns
		$\overline{INLE}$ low	15		
		OUTCLK high	15		
$t_{su}$	Setup time	OUTCLK low	15		ns
		Data before $\overline{INLE}$ ↑	10		
		Data before OUTCLK↑	25		
$t_h$	Hold time	$\overline{INLE}$ low before OUTCLK↑ (See Note 2)	30		ns
		Data after $\overline{INLE}$ ↑	5		
$T_A$	Operating free-air temperature	Data after OUTCLK↑	0		ns
			0	70	

NOTE 2: This setup time ensures the output registers will see stable data from the input latches.

**TIBPALT19L8C, TIBPALT19R4C, TIBPALT19R6C, TIBPALT19R8C**  
**HIGH-PERFORMANCE LATCHED-INPUT PAL® CIRCUITS**

**electrical characteristics over recommended free-air operating temperature range**

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>†</sup>	MAX	UNIT
V <sub>IK</sub>		V <sub>CC</sub> = 4.75 V,	I <sub>I</sub> = -18 mA			-1.5	V
V <sub>OH</sub>		V <sub>CC</sub> = 4.75 V,	I <sub>OH</sub> = -3.2 mA	2.4	3.3		V
V <sub>OL</sub>		V <sub>CC</sub> = 4.75 V,	I <sub>OL</sub> = 24 mA	0.35	0.5		V
I <sub>OZH</sub>	Outputs	V <sub>CC</sub> = 5.25 V,	V <sub>IH</sub> = 2.7 V			20	μA
	I/O ports					100	
I <sub>OZL</sub>	Outputs	V <sub>CC</sub> = 5.25 V,	V <sub>IH</sub> = 0.4 V			-20	μA
	I/O ports					-250	
I <sub>I</sub>	OE Input	V <sub>CC</sub> = 5.25 V,	V <sub>I</sub> = 5.5 V			0.2	mA
	All others					0.1	
I <sub>IH</sub>	OE Input	V <sub>CC</sub> = 5.25 V,	V <sub>I</sub> = 2.7 V			40	μA
	All others					20	
I <sub>IL</sub>	OE Input	V <sub>CC</sub> = 5.25 V,	V <sub>I</sub> = 0.4 V			-0.4	mA
	All others					-0.2	
I <sub>O</sub> <sup>‡</sup>		V <sub>CC</sub> = 5.25 V,	V <sub>O</sub> = 2.25 V	-30		-125	mA
I <sub>CC</sub>		V <sub>CC</sub> = 5.25 V, Outputs open	V <sub>I</sub> = 0 V,		150	210	mA

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP <sup>†</sup>	MAX	UNIT	
f <sub>max</sub>	OUTCLK↑	Q	R1 = 500 Ω, R2 = 500 Ω, C <sub>L</sub> = 50 pF, See Figure 1		30		MHz	
t <sub>pd</sub>	I, I/O	I/O, O				15	25	ns
t <sub>pd</sub>	I/D <sup>§</sup>	I/O, O				25	40	ns
t <sub>pd</sub>	INLE↓	I/O, O				28	40	ns
t <sub>pd</sub>	OUTCLK↑	Q				10	20	ns
t <sub>en</sub>	OE↓	Q				10	20	ns
t <sub>en</sub>	I, I/O	I/O, O				14	25	ns
t <sub>en</sub>	I/D <sup>§</sup>	I/O, O				30	40	ns
t <sub>en</sub>	INLE↓	I/O, O				30	40	ns
t <sub>dis</sub>	OE↑	Q				11	20	ns
t <sub>dis</sub>	I, I/O	I/O, O				12	25	ns
t <sub>dis</sub>	I/D <sup>§</sup>	I/O, O				14	25	ns
t <sub>dis</sub>	INLE↓	I/O, O				14	25	ns

<sup>†</sup> All typical values are V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

<sup>‡</sup> The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit current, I<sub>OS</sub>.

<sup>§</sup> Input configured as an input buffer or INLE low.

# TIBPALT19L8C, TIBPALT19R4C, TIBPALT19R6C, TIBPALT19R8C HIGH-PERFORMANCE LATCHED-INPUT PAL® CIRCUITS

## programming information

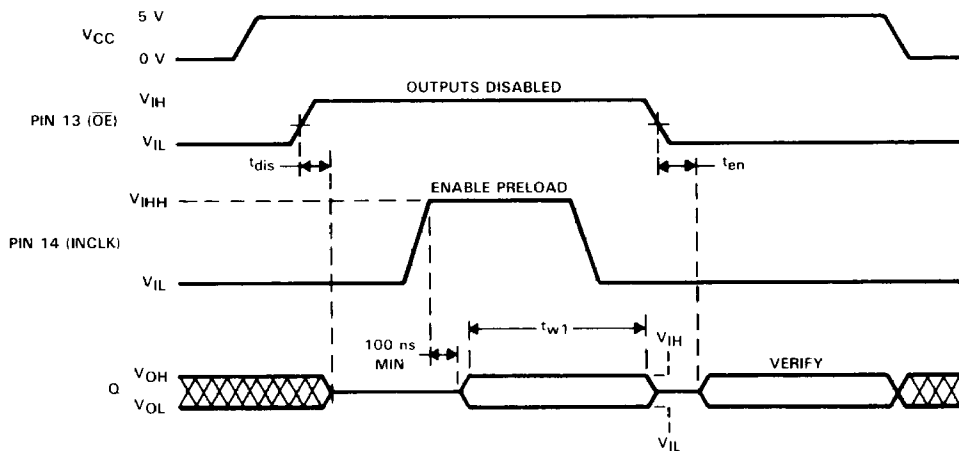
Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

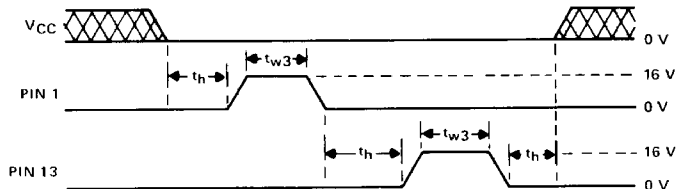
## preload procedure for registered outputs (see Note 3)

- Step 1 Pin 13 to  $V_{IH}$ , Pin 1 to  $V_{IL}$ , and  $V_{CC}$  to 5 volts.
- Step 2 Pin 14 to  $V_{IH}$
- Step 3 At Q outputs, apply  $V_{IL}$  to preload a low and  $V_{IH}$  to preload a high.
- Step 4 Pin 14 to  $V_{IL}$ .
- Step 5 Remove the voltages applied to the outputs.
- Step 6 Pin 13 to  $V_{IL}$
- Step 7 Check the output states to verify preload.

## preload waveforms (see Note 3)



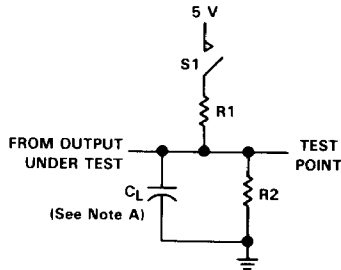
## security fuse programming (see Note 3)



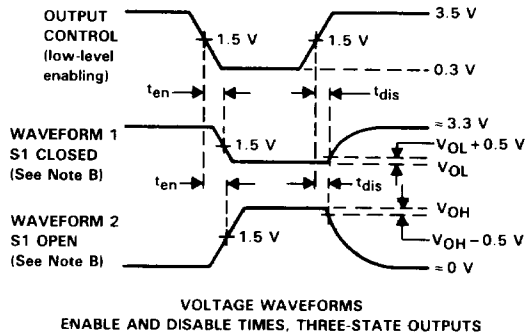
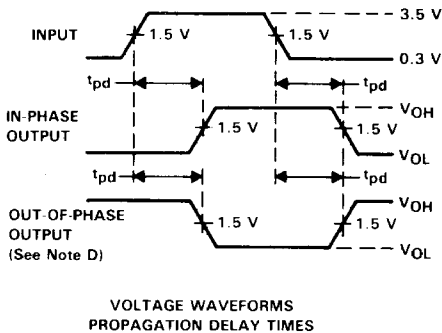
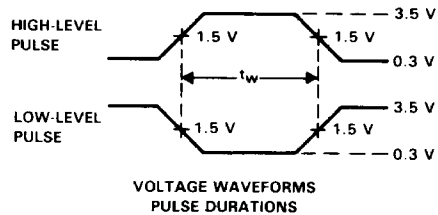
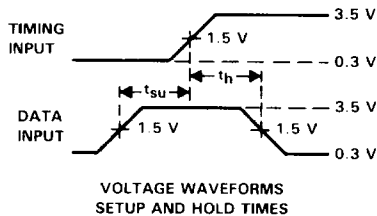
NOTE 3: Pin numbers shown are for JW and NT packages only. If chip carrier socket adapter is not used, pin numbers must be changed accordingly.

**TIBPALT19L8C, TIBPALT19R4C, TIBPALT19R6C, TIBPALT19R8C**  
**HIGH-PERFORMANCE LATCHED-INPUT PAL® CIRCUITS**

**PARAMETER MEASUREMENT INFORMATION**



**LOAD CIRCUIT FOR THREE-STATE OUTPUTS**



- NOTES: A.  $C_L$  includes probe and jig capacitance and is 50 pF for  $t_{pd}$  and  $t_{en}$ , 5 pF for  $t_{dis}$ .  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses have the following characteristics: PRR  $\leq$  1 MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%  
 D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.

**FIGURE 1**