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Z20K11xM Data Sheet

Contents

1 Introduction

1.1 Features

- Operating characteristics
  - Voltage range: 2.97 V to 5.5 V supply with fully functional flash memory program/erase/read operations
  - Ambient operating temperature range: –40 °C to 125 °C
- Arm™ Cortex M0+ core, 32-bit CPU
  - Up to 64 MHz frequency
  - Configurable Nested Vectored Interrupt Controller (NVIC)
  - Core MPU
- Clock interfaces
  - 4 ~ 40 MHz external oscillator
  - Up to 50 MHz DC external square input clock in external clock mode
  - UP to 64 MHz Internal RC oscillator
  - 32.768 KHz external oscillator
  - 32 KHz Low Power Internal RC Oscillator
  - 32 KHz Real Time Counter external clock (RTC_CLKIN)
  - Up to 20 MHz SWD_CLK
- Power management
  - Low-power Arm Cortex-M0+ core with excellent energy efficiency
  - Power Management Unit (PMU) with multiple power modes: RUN, WAIT, STOP, Standby
  - Clock gating and low power operation supported on specific peripherals
- Memory and memory interfaces
  - Up to 256 KB Code Flash memory with ECC
  - Up to 128 KB Data Flash memory with ECC
  - Up to 32 KB User IFR with ECC
  - Up to 32 KB SRAM with ECC
- Mixed-signal analog
  - One 12-bit Analog-to-Digital Converter (ADC) with up to 18 external analog inputs
  - One Analog Comparator (CMP, up to 11 channels) with internal 8-bit Digital-to-Analog Converter (DAC)
- Debug functionality
  - Serial Wire Debug Port (SWD)

- Human-machine interface (HMI)
  - Up to 55 GPIO pins with interrupt functionality
  - Non-maskable Interrupt (NMI)
- Communications interfaces
  - Up to four Universal Asynchronous Receiver/Transmitter (UART/LIN) modules with DMA support and low power availability
  - Up to three Serial Peripheral Interface (SPI) modules with DMA support and low power availability
  - Up to two Inter-Integrated Circuit (I2C) modules with DMA support and low power availability
  - Up to two CAN modules (with optional CAN-FD support)
- Safety and Security
  - 128-bit Unique Identification (ID) number
  - Error-Correcting Code (ECC) on flash and SRAM memories
  - CPU Memory Protection Unit
  - Cyclic Redundancy Check (CRC) module
  - Internal Watchdog (WDOG)
  - External Watchdog Timer (EWDT) module
- Timing and control
  - Up to three independent 16-bit Timers (TIM) modules, offering up to 8 standard channels (IC/OC/PWM) per module
  - One 4 channels 32-bit System Timer (STIM)
  - One Trigger Delay Generator (TDG) with flexible trigger system
  - 32-bit Real Time Counter (RTC)
- Package
  - 32-pin QFN-EP, 48-pin LQFP, 64-pin LQFP with up to 55 GPIO pins
- DMA and DMAMUX
  - 16 channel DMA with up to 57 request sources using DMAMUX

1.2 List of part number

Part Number	Pin Count	Package
Z20K114MCMME	32 pins	32-pin QFN-EP (5*5 mm, 0.5 mm pitch)
Z20K114MCMFL	48 pins	48-pin LQFP (7*7 mm, 0.5 mm pitch)
Z20K116MCMME	32 pins	32-pin QFN-EP (5*5 mm, 0.5 mm pitch)
Z20K116MCMFL	48 pins	48-pin LQFP

Part Number	Pin Count	Package
		(7*7 mm, 0.5 mm pitch)
Z20K116MCMHL	64 pins	64-pin LQFP (10*10 mm, 0.5 mm pitch)
Z20K118MCCFL	48 pins	48-pin LQFP (7*7 mm, 0.5 mm pitch)
Z20K118MCMFL	48 pins	48-pin LQFP (7*7 mm, 0.5 mm pitch)
Z20K118MCCHL	64 pins	64-pin LQFP (10*10 mm, 0.5 mm pitch)
Z20K118MCMHL	64 pins	64-pin LQFP (10*10 mm, 0.5 mm pitch)

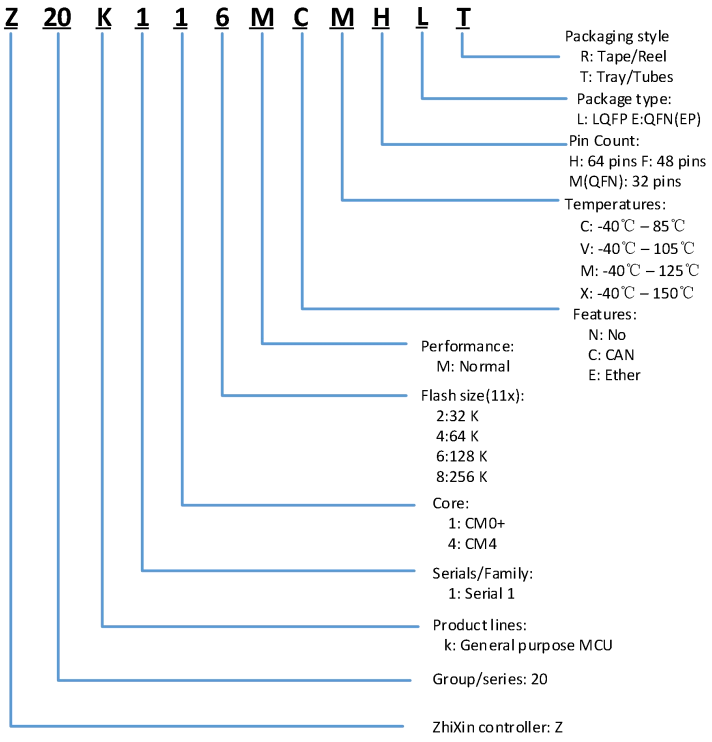

Figure 1. Classification of part number

1.3 Block diagram

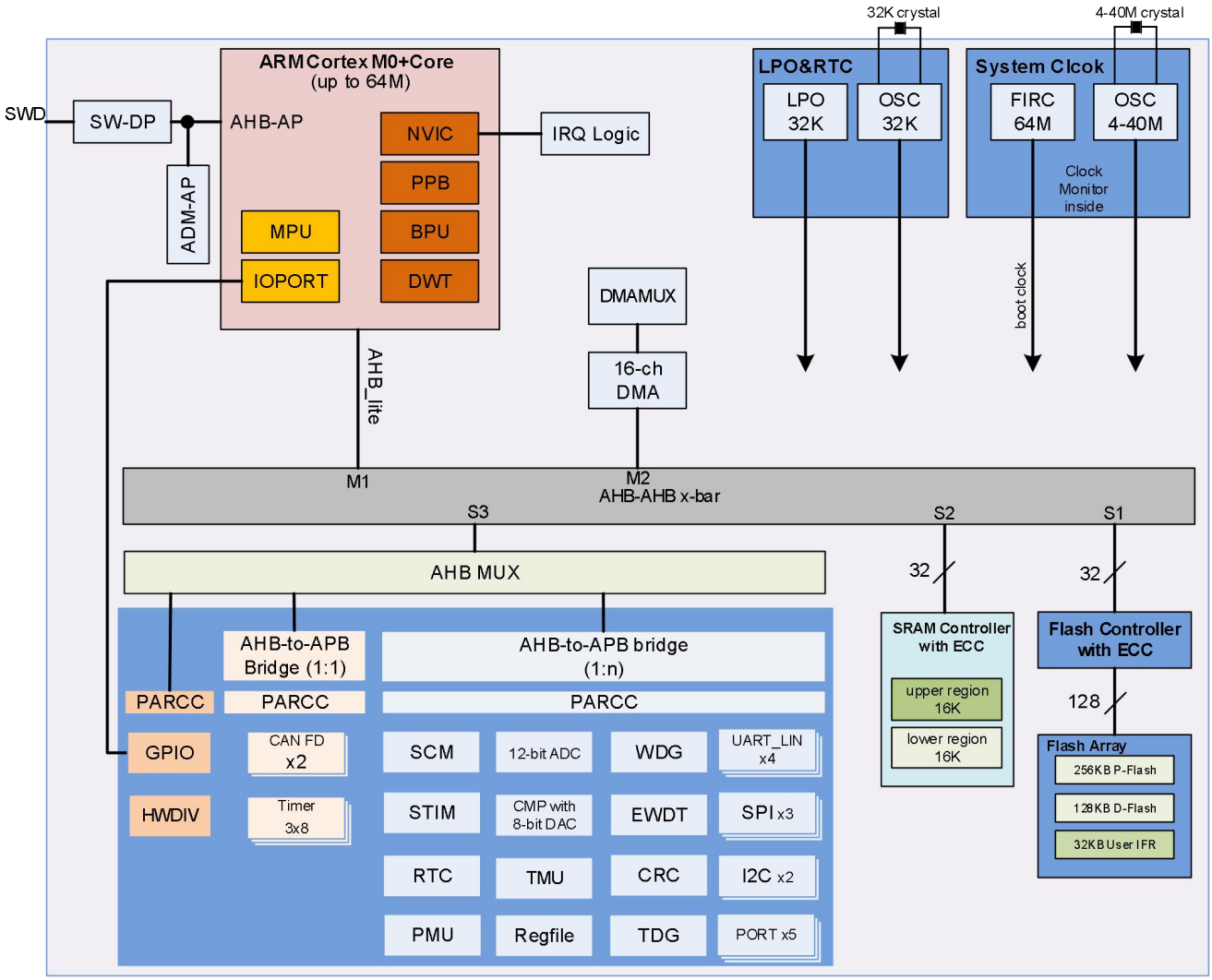

Figure 2. Z20K11xM block diagram

1.4 Package pinouts and signal descriptions

For package pinouts and signal descriptions, refer to the *Reference Manual*.

2 General electrical characteristics

2.1 Absolute maximum ratings

NOTE

- Functional operating conditions appear in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maximum values is not guaranteed. Product quality may suffer if the absolute maximum rating is exceeded even

momentarily for any parameter.

- Stress beyond the listed maximum values may affect device reliability or cause permanent damage to the device.
- All the limits defined in the data sheet specification must be honored together and any violation to any one or more will not guarantee desired operation.
- Unless otherwise specified, all maximum and minimum values in the data sheet are across process, voltage, and temperature.

Table 1. Absolute maximum ratings for Z20K11xM Series

Symbol	Parameter	Conditions[1]	Min	Max	Unit
V_{DD}[2]	2.97 V – 5.5 V input supply voltage	—	-0.3	5.8[3]	V
V_{DDA}	2.97 V – 5.5 V analog supply voltage	—	-0.3	5.8[3]	V
V_{REFH}	3.3 V / 5.0 V ADC high reference voltage	—	-0.3	5.8[3]	V
$I_{INJPAD\_DC\_ABS}$[4]	Continuous DC input current (positive/negative) that can be injected into an I/O pin	—	-3	+3	mA
V_{IN_DC}	Continuous DC Voltage on any I/O pin with respect to VSS	—	-0.8	5.8[5]	V
$I_{INJSUM\_DC\_ABS}$	Sum of absolute value of injected currents on all the pins (Continuous DC limit)	—	—	30	mA
T_{ramp}[6]	ECU supply ramp rate	—	0.5 V/min	500 V/ms	—
T_{ramp_MCU}[7]	MCU supply ramp rate	—	0.5 V/min	100 V/ms	—
T_A[8]	Operating ambient temperature	—	-40	125	°C
T_{STG}	Storage temperature	—	-55	150	°C
$V_{IN\_TRANSIENT}$	Transient overshoot voltage allowed on I/O pin beyond VIN_DC limit	—	—	6.8[9]	V

Note:

1. All voltages are referred to VSS unless otherwise specified.
2. As VDD varies between the minimum value and the absolute maximum value, the analog characteristics of the I/O and the ADC will both change. See sections I/O parameters and Analog characteristics respectively for details.
3. 60 seconds lifetime – No restrictions i.e. the part is not held in reset and can switch. 10 hours lifetime – The part is held in reset by an external circuit i.e. the part cannot switch. The supply should be kept in operating conditions and once out of operating conditions, the device should be either reset or powered off.

Operation with supply between 5.5 V and 5.8 V not in reset condition is allowed for 60 seconds cumulative over lifetime, the part will operate with reduced functionality. Operation with supply between 5.5 V and 5.8 V but held in reset condition by external circuit is allowed for 10 hours cumulative over lifetime.
If the given time limits or supply levels are exceeded, the device may get damaged.

4. When input pad voltage levels are close to VDD or VSS, practically no current injection is possible.

   The input pad voltage on ADC capability pads should not be higher than VDD, which means no current injection is allowed.

5. While respecting the maximum current injection limit.
6. This is the Electronic Control Unit (ECU) supply ramp rate and not directly the MCU ramp rate. Limit applies to both maximum absolute maximum ramp rate and typical operating conditions.
7. This is the MCU supply ramp rate and the ramp rate assumes that the Z20K11xM HW design guidelines are followed. Limit applies to both maximum absolute maximum ramp rate and typical operating conditions.
8. TJ (Junction temperature)=135 °C. Assumes TA=125 °C

   • Assumes maximum θ_{JA} for 2s2p board. See Thermal characteristics.

9. 60 seconds lifetime; device in reset (no outputs enabled/toggling).

2.2 Voltage and current operating requirements

NOTE

- Device functionality is guaranteed up to the LVD assert level, however electrical performance of 12-bit ADC, CMP with 8-bit DAC, IO electrical characteristics, and communication modules electrical characteristics would be degraded when voltage drops below 2.97 V.

Table 2. Voltage and current operating requirements for Z20K11xM series[1]

Symbol	Description	Min.	Max.	Unit
VDD[2, 3]	Supply voltage	2.97	5.5	V
VDD_OFF	Voltage allowed to be developed on VDD pin when it is not powered from any external power supply source.	0	0.1	V
VDDA[3]	Analog supply voltage	2.97	5.5	V
VDD – VDDA[3]	VDD-to-VDDA differential voltage	– 0.1	0.1	V
VREFH[4]	ADC reference voltage high	2.97	VDDA + 0.1	V
VREFL	ADC reference voltage low	-0.1	0.1	V
V_{ODPU}[5]	Open drain pullup voltage level	VDD	VDD	V

Symbol	Description	Min.	Max.	Unit
$I_{INJPAD\_DC\_OP}$[6]	Continuous DC input current (positive / negative) that can be injected into an I/O pin	-3	+3	mA
$I_{INJSUM\_DC\_OP}$	Continuous total DC input current that can be injected across all I/O pins such that there's no degradation in accuracy of analog modules: ADC and ACMP (See sections Analog characteristics and CMP with 8-bit DAC electrical specifications).	—	30	mA

1. Typical conditions assume VDD = VDDA = VREFH = 5 V, temperature = 25 °C and typical silicon process unless otherwise stated.
2. As VDD varies between the minimum value and the absolute maximum value, the analog characteristics of the I/O and the ADC will both change. See sections I/O parameters and Analog characteristics respectively for details.
3. VDD and VDDA must be shorted to a common source on PCB. Appropriate decoupling capacitors should be used to filter noise on the supplies.
4. VREFH should always be equal to or less than VDDA + 0.1 V and VDD + 0.1 V.
5. Open drain outputs must be pulled to VDD.
6. When input pad voltage levels are close to VDD or VSS, practically no current injection is possible.

2.3 Thermal operating characteristics

Table 3. Thermal operating characteristics for Z20K11xM series

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
$T_{A\ C\text{-}Grade\ Part}$	Ambient temperature under bias	-40	—	85	℃
$T_{J\ C\text{-}Grade\ Part}$	Junction temperature under bias	-40	—	105	℃
$T_{A\ V\text{-}Grade\ Part}$	Ambient temperature under bias	-40	—	105	℃
$T_{J\ V\text{-}Grade\ Part}$	Junction temperature under bias	-40	—	125	℃
$T_{A\ M\text{-}Grade\ Part}$	Ambient temperature under bias	-40	—	125	℃
$T_{J\ M\text{-}Grade\ Part}$	Junction temperature under bias	-40	—	135	℃

2.4 Power and ground pins

NOTE

VDD and VDDA must be shorted to a common source on PCB.

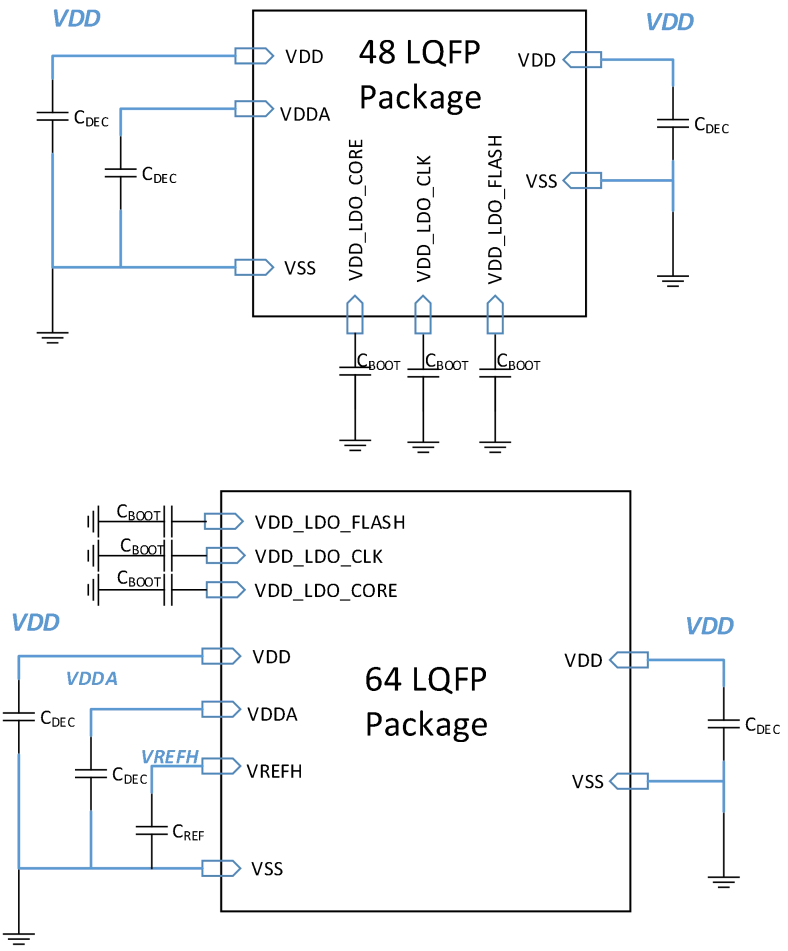

Figure 3. Pinout decoupling

Table 4. Supplies decoupling capacitors[1, 2]

Symbol	Description	Min.[3]	Typ.	Max.	Unit
C_{REF}[4, 5]	ADC reference high decoupling capacitance	70	100	—	nF
C_{DEC}[5, 6, 7]	Recommended decoupling capacitance	70	100	—	nF
C_{BOOT}[8]	Recommended LDO boot capacitance	700	1000	—	nF

1. VDD and VDDA must be shorted to a common source on PCB. Appropriate decoupling capacitors should be used to filter noise on the supplies. All VSS pins should be connected to common ground at the PCB level.
2. All decoupling capacitors must be low ESR ceramic capacitors (for example X7R type).
3. Minimum recommendation is after considering component aging, temperature and tolerance.
4. For improved performance, it is recommended to use 10 μF, 0.1 μF and 1 nF capacitors in parallel.
5. All decoupling capacitors should be placed as close as possible to the corresponding supply and ground pins.
6. Contact your local Field Applications Engineer for details on best analog routing practices.

7. The filtering used for decoupling the device supplies must comply with the following best practices rules:

- The protection/decoupling capacitors must be on the path of the trace connected to that component.
- No trace exceeding 1 mm from the protection to the trace or to the ground.
  The protection/decoupling capacitors must be as close as possible to the input pin of the device (maximum 2 mm).
- The ground of the protection is connected as short as possible to the ground plane under the integrated circuit.

8. All boot capacitors should be placed as close as possible to the corresponding pins and ground pins, and must comply with the following best practices rules:

- The boot capacitors must be as close as possible to the pin of the device (maximum 2 mm).
- The ground of the boot capacitors is connected as short as possible to the ground plane under the integrated circuit.
- For improved performance, it is recommended to use 1 μF, 0.1 μF in parallel.

2.5 LVW, LVD and POR operating requirements

Table 5. VDD supply LVW, LVD and POR operating requirements for Z20K11xM series

Symbol	Description	Min.	Typ.	Max.	Unit
V_{POR}	Rising and falling VDD POR detect voltage	0.9	1.6	2.2	V
V_{LVW}	Falling low-voltage warning threshold	—	4.3	—	V
V_{LVW_FLT} [1]	LVW filter window	—	2/16	—	us
V_{LVD}	Falling low-voltage detect threshold	—	2.4	—	V
V_{LVD_FLT} [1]	LVD filter window	—	2/16	—	us
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V

1. LVD, LVW filter window can be configured as 2us or 16us, and default value is 16us.

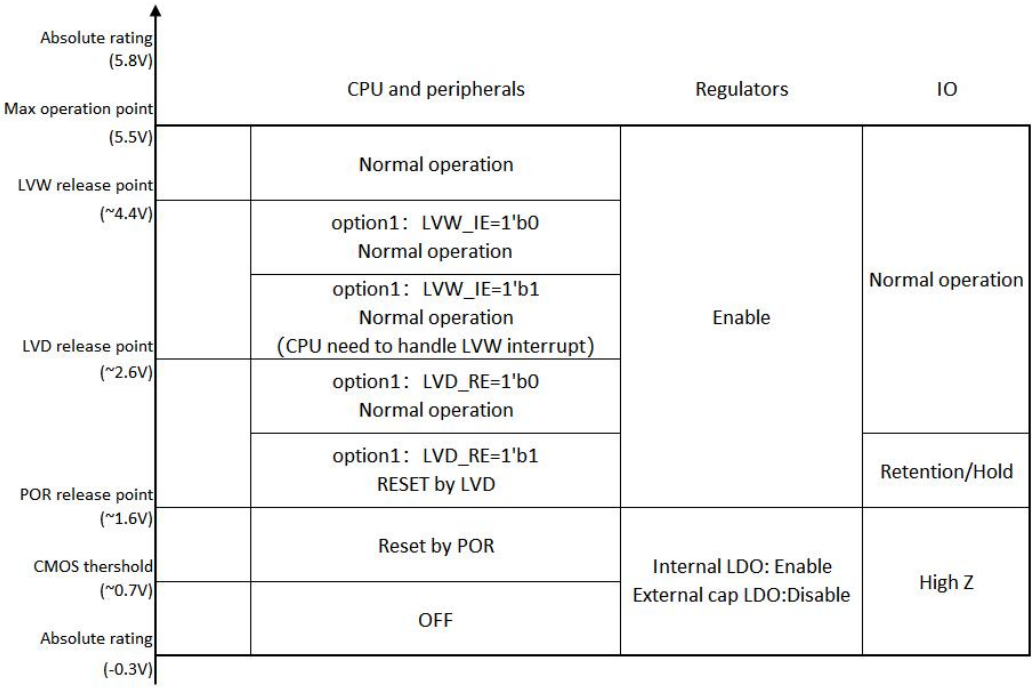

Figure 4 Device operations supply range

2.6 Power mode transition operating behaviors

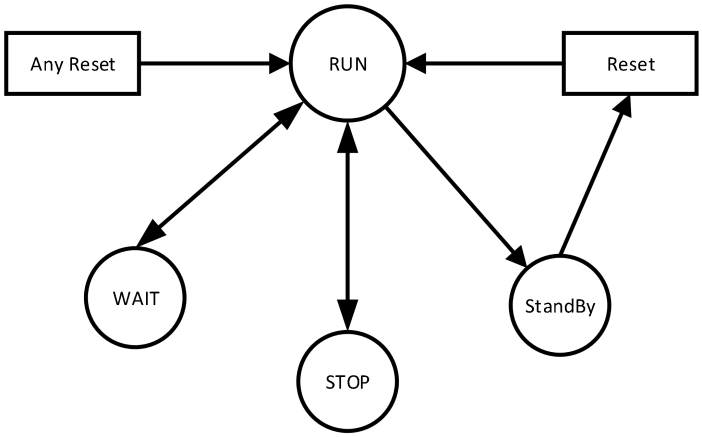

Figure 5. Power mode transition operation

All specifications in the following table assume this clock configuration:

Table 6. Clock configuration

	Z20K11xM
RUN mode	

Clock source	FIRC/OSC40
SYS_CLK/CORE_CLK	Configurable，up to 64 MHz
BUS_CLK	Configurable，up to 64 MHz
FLASH_CLK	Configurable，fixed 8 MHz
WAIT mode	
Clock source	FIRC/OSC40
SYS_CLK/CORE_CLK	CORE_CLK off
BUS_CLK	Configurable，up to 64 MHz
FLASH_CLK	Configurable，fixed 8 MHz
STOP mode	
All clock source disabled (CORE_CLK, BUS_CLK, FLASH_CLK)	
Standby mode (Lower power than Stop mode)	
All clock source disabled (CORE_CLK, BUS_CLK, FLASH_CLK)	

Table 7. Power mode transition operating behaviors for Z20K11xM series

Symbol	Description	Min.	Typ.	Max.	Unit
t_{POR}	After a POR event, amount of time from the point VDD reaches 2.97 V to execution of the first instruction across the operating temperature range of the chip.	—	3050	—	μs
	WAIT → RUN	—	0.1	—	μs
	STOP → RUN	—	35	—	μs
	RESET → RUN	—	50	—	μs
	RUN → STOP	—	0.65	—	μs
	RUN → WAIT	—	0.1	—	μs
	RUN → Standby	—	0.6	—	μs
	Standby → RUN	—	550	—	μs

2.7 Power consumption

The following table shows the power consumption targets for the device in various modes of operation.

Table 8. Power consumption (Typicals unless stated otherwise)[1]

Chip/Device	Ambient Temperature (°C)		Standby (uA)	WAIT (mA)	STOP (uA)[2]	RUN@64 MHz (mA)	IDD/MHz (μA/MHz)[3]

				Peripherals disabled	Peripherals enable	Peripherals disabled	Peripherals disabled	Peripherals enable	
Z20K118	25	Typ.	10.5	4	5	107	6	—	100
	85	Typ.	19.5	4.5	5.5	372	6.5	—	—
		Max.	—	—	—	—	—	—	—
	105	Typ.	—	—	—	—	—	—	—
		Max.	—	—	—	—	—	—	—
	125	Typ.	42	5	6	982	7	—	—
		Max.	—	—	—	—	—	—	—

1. Typical current numbers are indicative for typical silicon process and may vary based on the silicon distribution and user configuration. Typical conditions assume VDD = VDDA = VREFH = 5 V, temperature = 25 °C and typical silicon process unless otherwise stated. All output pins are floating and on-chip pull down is enabled for all unused input pins.
2. Current numbers are for reduced configuration and may vary based on user configuration and silicon process variation.
3. Values mentioned with peripherals disabled.

The following table shows the power consumption targets for **Z20K118** in various modes of operation measured at 3.3 V.

Table 9. Power consumption at 3.3 V[1]

Chip/Device	Ambient Temperature (°C)		Standby (uA)	WAIT (mA)		STOP (uA)[2]	RUN@64 MHz (mA)		IDD/MHz (µA/MHz)[3]
				Peripherals disabled	Peripherals enable	Peripherals disabled	Peripherals disabled	Peripherals enable	
Z20K118	25	Typ.	9.5	4	5	107	6	—	100
	85	Typ.	18.5	4.5	5.5	370	6.5	—	—
		Max.	—	—	—	—	—	—	—
	105	Typ.	—	—	—	—	—	—	—
		Max.	—	—	—	—	—	—	—
	125	Typ.	41	5	6	979	7	—	—
		Max.	—	—	—	—	—	—	—

1. Typical current numbers are indicative for typical silicon process and may vary based on the silicon distribution and user configuration. Typical conditions assume VDD = VDDA =

VREFH = 3.3 V, temperature = 25 °C and typical silicon process unless otherwise stated. All output pins are floating and on-chip pull down is enabled for all unused input pins.

2. Current numbers are for reduced configuration and may vary based on user configuration and silicon process variation.
3. Values mentioned with peripherals disabled.

2.8 ESD handling ratings

Table 10. ESD handling ratings

Symbol	Description	Min.	Max.	Unit
VHBM[1]	Electrostatic discharge voltage, human body model	- 6	6	KV
VCDM[2]	Electrostatic discharge voltage, charged-device model			
	All pins except the corner pins	- 500	500	V
	Corner pins only	- 750	750	V
ILAT[3]	Latch-up current at ambient temperature of 125 °C	- 100	100	mA

1. Determined according to JEDEC Standard AEC Q100-002, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard AEC Q100-011, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

2.9 EMC radiated emissions operating behaviors

EMC measurements to chip-level IEC standards are available from ZHIXIN upon request.

2.10 Thermal handling ratings

Table 11. Thermal handling ratings

Symbol	Description	Min.	Max.	Unit
T_{STG}[1]	Storage temperature	-55	150	℃
T_{SDR}[2]	Solder temperature, lead-free	—	260	℃

1. Determined according to JEDEC Standard JESD22-A103, High Temperature Storage Life.
2. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices.

2.11 Moisture handling ratings

Table 12. Thermal handling ratings

Symbol	Description	Min.	Max.	Unit
MSL[1]	Moisture sensitivity level	—	3	—

1. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices.

3 I/O parameters

3.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

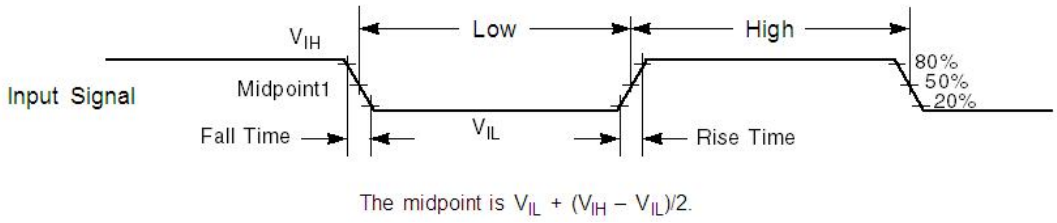

Figure 6. Input signal measurement reference

3.2 General AC specifications

These general purposes specifications apply to all signals configured for GPIO, UART, and timers.

Table 13. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled, passive filter disabled)	50	—	ns	1
WFRST	RESET input filtered pulse	—	10	ns	2
WNFRST	RESET input not filtered pulse	100	—	ns	3

1. These pins do not have a passive filter on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
2. Maximum length of RESET pulse which will be filtered by internal filter only if PCR_PTA5[PFE] is at its reset value of 1'b1.
3. Minimum length of RESET pulse, which is guaranteed not to be filtered by the internal filter only if PCR_PTA5[PFE] is at its reset value of 1'b1. After this filtering mechanism, the software has an option to put additional filtering in addition to this.

3.3 DC electrical specifications

Table 14. DC electrical specifications at 3.3 V Range for Z20K11xM series

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	I/O Supply Voltage	2.97	3.3	4	V	
V_{ih}	Input Buffer High Voltage	0.7 × V_{DD}	—	V_{DD} + 0.3	V	1
V_{il}	Input Buffer Low Voltage	VSS – 0.3	—	0.3 × V_{DD}	V	2
V_{hys}	Input Buffer Hysteresis	0.06 × V_{DD}	—	—	V	
Ioh_{GPIO} $Ioh_{PORT\text{-}PCR\_DSE\_0}$	I/O current source capability measured when pad Voh = (VDD – 0.8 V)	3.5	—	—	mA	
Iol_{GPIO} $Iol_{PORT\text{-}PCR\_DSE\_0}$	I/O current sink capability measured when pad Vol = 0.8 V	3	—	—	mA	
$Ioh_{PORT\text{-}PCR\_DSE\_1}$	I/O current source capability measured when pad Voh = (VDD – 0.8 V)	14	—	—	mA	3
$Iol_{PORT\text{-}PCR\_DSE\_1}$	I/O current sink capability measured when pad Vol = 0.8 V	12	—	—	mA	3
IOHT	Output high current total for all ports	—	—	100	mA	
IIN	Input leakage current (per pin) for full temperature range at VDD = 3.3 V					4
	All pins other than high drive port pins	—	0.005	1	μA	
	High drive port pins	—	0.010	1	μA	
RPU	Internal pullup resistors	—	30	—	kΩ	5
RPD	Internal pulldown resistors	—	30	—	kΩ	6

1. For reset pads, same V_{ih} levels are applicable.
2. For reset pads, same V_{il} levels are applicable.
3. The value given is measured at high drive strength mode. For value at low drive strength mode, see the Ioh_Standard value given above.
4. Several I/Os have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only. For details, see the *Reference Manual*.
5. Measured at input V = VSS
6. Measured at input V = VDD

Table 15. DC electrical specifications at 5.0 V Range for Z20K11xM series

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	I/O Supply Voltage	4	—	5.5	V	
V_{ih}	Input Buffer High Voltage	0.65 × V_{DD}	—	V_{DD} + 0.3	V	1
V_{il}	Input Buffer Low Voltage	VSS – 0.3	—	0.3 × V_{DD}	V	2
V_{hys}	Input Buffer Hysteresis	0.06 × V_{DD}	—	—	V	
Ioh_{GPIO} $Ioh_{PORT\text{-}PCR\_DSE\_0}$	I/O current source capability measured when pad Voh = (VDD – 0.8 V)	5	—	—	mA	
Iol_{GPIO} $Iol_{PORT\text{-}PCR\_DSE\_0}$	I/O current sink capability measured when pad Vol = 0.8 V	5	—	—	mA	
$Ioh_{PORT\text{-}PCR\_DSE\_1}$	I/O current source capability measured when pad Voh = (VDD – 0.8 V)	20	—	—	mA	3
$Iol_{PORT\text{-}PCR\_DSE\_1}$	I/O current sink capability measured when pad Vol = 0.8 V	20	—	—	mA	3
I_{OHT}	Output high current total for all ports	—	—	100	mA	
I_{IN}	Input leakage current (per pin) for full temperature range at VDD = 5.5 V					4
	All pins other than high drive port pins		0.005	1	μA	
	High drive port pins		0.010	1	μA	
R_{PU}	Internal pullup resistors		30		kΩ	5
R_{PD}	Internal pulldown resistors		30		kΩ	6

1. For reset pads, same Vih levels are applicable.
2. For reset pads, same Vil levels are applicable.
3. The value given is measured at high drive strength mode. For value at low drive strength mode, see the Ioh_Standard value given above.
4. Several I/Os have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only. For details, see the *Reference Manual*.
5. Measured at input V = VSS
6. Measured at input V = VDD

3.4 AC electrical specifications

Table 16. AC electrical specifications at 3.3 V Range for Z20K11xM series

Symbol	DSE	Rise time (nS)[1]		Fall time (nS)[1]		Capacitance (pF)[2]
		Min.	Max.	Min.	Max.	
t_{RFGPIO}	NA	2.8	9.0	2.4	7.9	25
		6.1	19.8	5.6	18.5	50
$t_{RFGPIO-HD}$	0	2.8	9.0	2.4	7.9	25
		6.1	19.8	5.6	18.5	50
	1	1.3	4.0	1.3	4.3	25
		2.1	6.7	1.9	5.8	50

1. For reference only. Run simulations with the IBIS model and your custom board for accurate results.
2. Maximum capacitance supported on Standard IOs. However interface or protocol specific specifications might be different; for protocol specific AC specifications, see respective sections.

Table 17. AC electrical specifications at 5 V Range for Z20K11xM series

Symbol	DSE	Rise time (nS)[1]		Fall time (nS)[1]		Capacitance (pF)[2]
		Min.	Max.	Min.	Max.	
t_{RFGPIO}	NA	2.1	6.1	1.9	5.5	25
		4.6	13.3	4.3	12.7	50
$t_{RFGPIO-HD}$	0	2.1	6.1	1.9	5.5	25
		4.6	13.3	4.3	12.7	50
	1	1.0	2.8	1.0	2.8	25
		1.5	4.5	1.4	4.1	50

1. For reference only. Run simulations with the IBIS model and your custom board for accurate results.
2. Maximum capacitance supported on Standard IOs. However, interface or protocol specific specifications might be different; for protocol specific AC specifications, see respective sections.

Table 18. Standard input pin capacitance

Symbol	Description	Min.	Max.	Unit
C_{IN_D}	Input capacitance: digital pins	—	10	pF

3.5 Device clock specifications

Table 19. Device clock specifications

Symbol	Description	Min.	Max.	Unit
Normal run mode (Z20K11xM series)				
f_{SYS}	System and core clock	—	64	MHz
f_{BUS}	Bus clock	—	64	MHz
f_{FLASH}	Flash clock	—	8	MHz

Symbol	Description	Min.	Max.	Unit
WAIT mode (Z20K11xM series)[1]				
f_{SYS}	System and core clock	—	64	MHz
f_{BUS}	Bus clock	—	64	MHz
f_{FLASH}	Flash clock	—	8	MHz
STOP mode (Z20K11xM series)[1]				
f_{SYS}	System and core clock	—	OFF	MHz
f_{BUS}	Bus clock	—	OFF	MHz
f_{FLASH}	Flash clock	—	OFF	MHz

1. The frequency limitations here override any frequency specification listed in the timing specification for any other module.

4 Peripheral operating requirement and behaviors

4.1 Clock interface modules

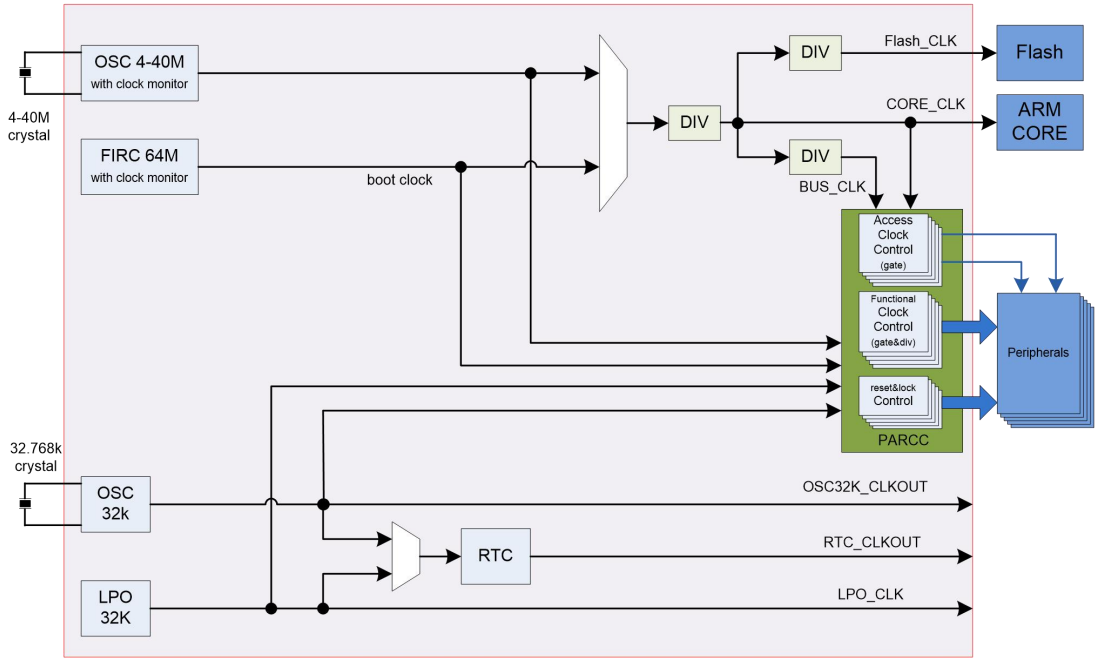

Figure 7. Clock diagram

4.1.1 External system oscillator electrical specifications

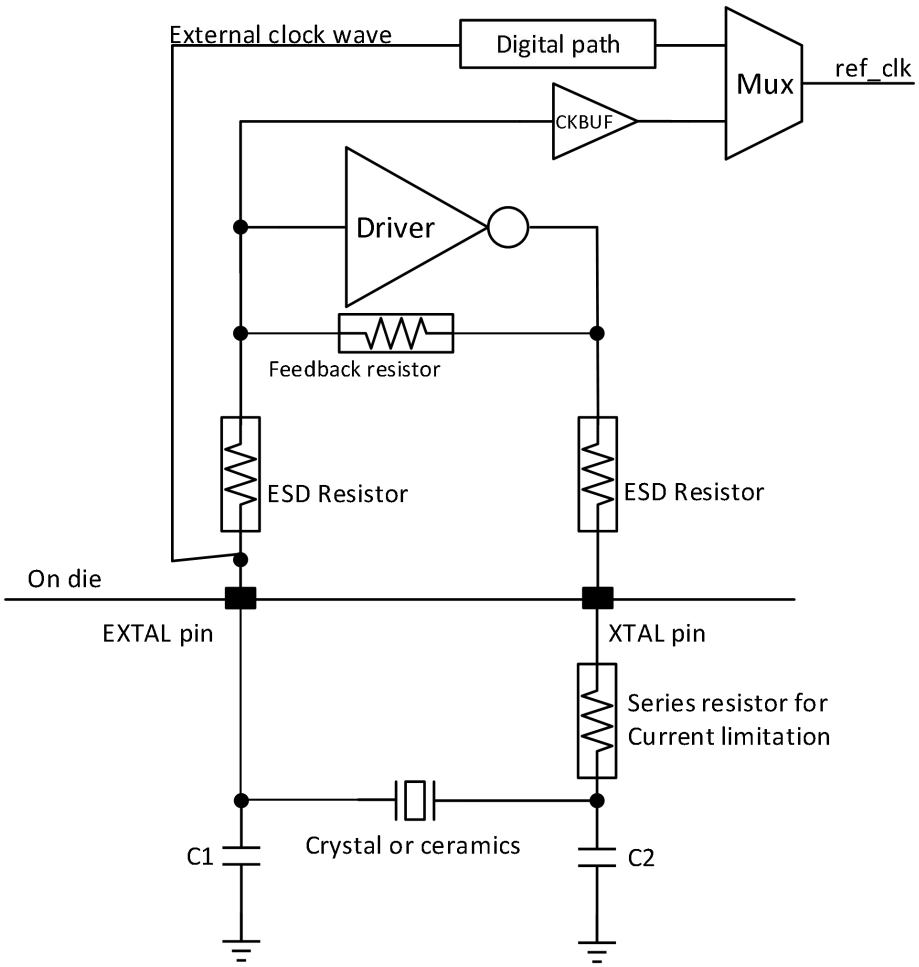

Figure 8. Oscillator connections scheme

Table 20. External System Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit
f_{osc_hi}	Oscillator crystal or resonator frequency with HFREQ =0	8		24	MHz
f_{osc_hi}	Oscillator crystal or resonator frequency with HFREQ =1	24	—	40 [1, 2]	MHz
f_{ec_extal}[1]	Input clock frequency (external clock mode)	—	—	48	MHz
t_{dc_extal}[1]	Input clock duty cycle (external clock mode)	48	50	52	%
I_{OSC}	OSC power consumption using 40MHz crystal		500		μA
T_{cst}[2] (Crystal Start-up Time)	16 MHz low-gain mode (HFREQ =0)	—	1.5	—	ms
	40 MHz high-gain mode (HFREQ =1)	—	1	—	ms

1. Frequencies below 40 MHz can be used for degraded duty cycle up to 40-60%.
2. Proper PC board layout procedures must be followed to achieve specifications.

4.1.2 Fast internal RC oscillator (FIRC) electrical specifications

Table 21. Fast internal RC Oscillator electrical specifications for Z20K11xM series

Symbol	Parameter[1]	Value			Unit
		Min.	Typ.	Max.	Value
F_{FIRC}	FIRC target frequency	—	64	—	MHz
ΔF85	Frequency deviation across process, voltage, and temperature < 85 °C	—	—	—	$\%F_{FIRC}$
ΔF125	Frequency deviation across process, voltage, and temperature < 125 °C	-12		+12	$\%F_{FIRC}$
$T_{Startup}$	Startup time	—	2	—	μs[2]
I_{FIRC}	FIRC Supply Current Consumption	—	160	—	μA

1. With FIRC enable.
2. Startup time is defined as the time between clock enable and clock availability for system use.

4.1.3 Internal Low Power Oscillator (LPO32K)

Table 22. Internal Low Power Oscillator (LPO32K) electrical specifications for Z20K11xM series

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
F_{LPO}	Internal low power oscillator frequency	—	32	—	KHz
ΔF85	Frequency deviation across process, voltage, and temperature < 85°C	—	—	—	$\%F_{LPO}$
ΔF125	Frequency deviation across process, voltage, and temperature < 125°C	—	±13	—	$\%F_{LPO}$
$T_{Startup}$	Startup time	—	—	3000	μs[1]

1. Startup time is defined as the time between clock enable and clock availability for system use.

4.1.4 External low oscillator (OSC32K)

Table 23. External oscillator electrical specifications for Z20K11xM series

Symbol	Description	Min.	Typ.	Max.	Unit
f_{osc_32k}	Crystal frequency	—	32.768	—	KHz
I_{OSC32K}	OSC32K Supply Current Consumption	—	2	—	μA

t_{start}	Crystal start-up time	—	500	—	ms

4.2 Memory and memory interfaces

4.2.1 Flash memory module

This section describes the electrical characteristics of the flash memory module.

Table 24. Flash command timing specifications for Z20K11xM series[3]

Symbol	Description[1]		Z20K116		Z20K118		Unit
			Typ.	Max.	Typ.	Max.	
t_{rd1blk}	Read 1 Block execution time	128 KB flash	1.026	—	—	—	ms
		256 KB flash	—	—	2.050	—	
t_{rd1sec}	Read 1 Section execution time	8 KB flash	66	—	66	—	µs
t_{rd1phr}	Read 1s Phrase execution time	—	2	—	2	—	µs
$t_{rdmisr8k}$	Read into MISR	8KB	66	—	66	—	µs
t_{rdmisr}	Read into MISR	128 KB flash	1.026	—	—	—	ms
		256 KB flash	—	—	2.050	—	ms
$t_{rd1iscr}$	Read 1s IFR Sector execution time	—	66	—	66	—	µs
$t_{rd1iphr}$	Read 1s IFR Phrase execution time	—	2	—	2	—	µs
$t_{rdimisr8k}$	Read IFR into MISR	8 KB	66	—	66	—	µs
$T_{rdimisr32k}$	Read IFR into MISR	32 KB	258	—	258	—	µs
t_{pgmphr}	Program Phrase execution	—	167	375	167	375	µs

Symbol	Description[1]		Z20K116		Z20K118		Unit
			Typ.	Max.	Typ.	Max.	
	time						
t_{ersscr}[2]	Erase Flash Sector execution time	—	1	20	1	20	ms
t_{rd1all}	Read 1s All Block execution time	—	1.795	—	3.589	—	ms
t_{ersall}[2]	Erase All Blocks execution time	—	55	1050	55	1050	ms

1. All command times assume at condition: core_clk = 64M, flash_clk = 8M.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. Minimum configure value of FLASH_FCTRL[RWSC] should consider AHB clock frequency:

   AHB Clock Freq (Full Power)<32 MHz,FLASH_FCTRL[RWSC] should>= 0000b
   AHB Clock Freq (Full Power) in[32 – 64 MHz],FLASH_FCTRL[RWSC] should >= 0001b
   AHB Clock Freq (Full Power) in[64 – 96 MHz],FLASH_FCTRL[RWSC] should >= 0010b

4.2.2 Reliability specifications

Table 25. NVM reliability specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
When using as Program and Data Flash						
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	—	—	years	1
$n_{nvmcycp}$	Cycling endurance	1K	—	—	cycles	2, 3

1. Data retention period per block begins upon initial user factory programming or after each subsequent erase.
2. Program and Erase for Pflash and Dflash are supported across product temperature specification in Normal Mode.
3. Cycling endurance is per Dflash or Pflash Sector.

4.3 Analog characteristics

4.3.1 12-bit A/D converter electrical specifications

Table 26. 12-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
VREFH	ADC reference voltage high			VDDA		V	[2]
VREFL	ADC reference voltage low			0		mV	[2]
V_{ADIN}	Input voltage		VREFL	—	VREFH	V	
			Vss	—	VDDA	V	
R_S	Source impedance		—	—	2.5	kΩ	
R_{AD}	Sampling Switch Impedance		—	100	300	Ω	
C_{P1}	Pin Capacitance		—	10	—	pF	
C_{P2}	Analog Bus Capacitance		—	—	4	pF	
C_S	Sampling capacitance		—	4	5	pF	
f_{CONV}	ADC conversion frequency	No ADC hardware averaging.[5] Continuous conversions enabled, subsequent conversion time	—	1000	—	Ksps	[3, 4, 6]

1. Typical values assume VDDA = 5 V, Temp = 25 °C and CAS=10 nF unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. For packages without dedicated VREFH and VREFL pins, VREFH is internally tied to VDDA, and VREFL is internally tied to VSS. To get maximum performance, reference supply quality should be better than SAR ADC. See Voltage and current operating requirements for [Min, Max] values.
3. Clock and compare cycle need to be set according to the guidelines mentioned in the *Reference Manual*.
4. ADC conversion will become less reliable above maximum frequency.
5. When using ADC hardware averaging, see the *Reference Manual* to determine the most appropriate setting for AVGS.
6. For guidelines and examples of conversion rate calculation, see the *Reference Manual*.

4.3.2 12-bit ADC electrical characteristics

NOTE

- On reduced pin packages where ADC reference pins are

shared with supply pins, ADC analog performance characteristics may be impacted. The amount of variation will be directly impacted by the external PCB layout and hence care must be taken with PCB routing.

- All accuracy numbers assume the ADC is calibrated with VREFH=VDDA=VDD, with the calibration frequency set to less than or equal to half of the maximum specified ADC clock frequency.

Table 27. 12-bit ADC characteristics (3 V to 5.5 V)(VREFH = VDDA, VREFL = VSS)

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
VDDA	Supply voltage	3	—	5.5	V	
IDDA_ADC	Supply current per ADC	—	0.16	—	mA	[2]
SMPLTS	Sample Time	300	—	—	ns	
TUE[3]	Total unadjusted error	—	±4	—	LSB[4]	[5, 6, 7, 8]
DNL	Differential non-linearity	—	±1.0	—	LSB[4]	[5, 6, 7, 8]
INL	Integral non-linearity	—	±2.0	—	LSB[4]	[5, 6, 7, 8]

1. Typical values assume VDDA = 5.0 V, Temp = 25 °C unless otherwise stated.
2. The ADC supply current depends on the ADC conversion rate.
3. TUE, which represents total static error, includes offset and full scale error. Ignore 20LSB in header and tail while calculating.
4. 1 LSB = (VREFH – VREFL)/2^N
5. The specifications are with averaging and in standalone mode only. Performance may degrade depending upon device use case scenario. When using ADC averaging, refer to the *Reference Manual* to determine the most appropriate settings for AVGS.
6. For ADC signals adjacent to VDD/VSS or XTAL/EXTAL or high frequency switching pins, some degradation in the ADC performance may be observed; for ADC signal around VSS or VDD, some degradation in the ADC performance may be observed
7. All values guarantee the performance of the ADC for multiple ADC input channel pins. When using ADC to monitor the internal analog parameters, assume minor degradation.
8. All the parameters in the table are given assuming system clock as the clocking source for ADC.

4.4 CMP with 8-bit DAC electrical specifications

Table 28. CMP with 8-bit DAC electrical specifications for Z20K11xM series

Symbol	Description	Min.	Typ.	Max.	Unit
V_{AIN}	Analog input voltage	0	0 –	VDDA	V

Symbol	Description	Min.	Typ.	Max.	Unit
			VDDA		
V_{AIO}	Analog input offset voltage, High-speed mode				mV
	-40 – 125 ℃	—	±1.5	—	
V_{AIO}	Analog input offset voltage, Low-speed mode				mV
	-40 – 125 ℃	—	±0.7	—	
	-40 – 125 ℃	—	1.325	—	
I_{DAC8b}	8-bit DAC current adder (enabled)				
	3.3V Reference Voltage	—	28	—	μA
	5V Reference Voltage	—	30	—	μA
INL[1]	8-bit DAC integral non-linearity	—	±0.6	—	LSB[2]
DNL	8-bit DAC differential non-linearity	—	±0.5	—	LSB[2]
t_{DDAC}	Initialization and switching settling time	—	0.5	—	μs

1. Calculation method used: Linear Regression Least Square Method.
2. 1 LSB = $V_{reference}$ /256； while the INL and DNL are calculated, DAC code is in range of [10,245].

NOTE

For comparator input signals adjacent to VDD/VSS or XTAL/ EXTAL or switching pins cross coupling may happen and hence hysteresis settings can be used to obtain the desired comparator performance. Additionally, an external capacitor (1nF) should be used to filter noise on input signal. Also, source drive should not be weak (Signal with < 50 K pull up/down is recommended).

4.5 Communication modules

4.5.1 UART electrical specifications

Refer to General AC specifications for LPUART specifications.
Baud rate = (function clock frequency)/(16*divisor)
For details, see section: ‘Baud rate clock generation’ of the *Reference Manual*.

4.5.2 SPI electrical specifications

The Low Power Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following table provides timing characteristics for classic SPI timing modes.

- All timing is shown with respect to 20% VDD and 80% VDD thresholds.
- All measurements are with maximum output load of 50 pF, input transition of 1 ns and pad configured with fastest slew setting (DSE = 1).

Table 29. SPI electrical specifications[1]

Num	Symbol	Description	Conditions	Run Mode				Unit
				5.0 V IO		3.3 V IO		
				Min.	Max.	Min.	Max.	
	f_{periph}[2,3]	Peripheral Frequency	Slave	-	64	-	64	MHz
			Master	-	64	-	64	
1	f_{op}	Frequency of operation	Slave	-	8	-	8	MHz
			Master[4]	-	8	-	8	
2	t_{SPSCK}	SPSCK period	Slave	125	-	125	-	ns
			Master	125	-	125	-	
3	t_{Lead}[5]	Enable lead time (PCS to SPSCK delay)	Slave	-	-	-	-	ns
			Master	$t_{SPSCK}/2$	-	$t_{SPSCK}/2$	-	
4	t_{Lag}[6]	Enable lag time (After SPSCK delay)	Slave	-	-	-	-	ns
			Master	$t_{SPSCK}/2$	-	$t_{SPSCK}/2$	-	
5	t_{WSPSCK}[7]	Clock(SPSCK) high or low time (SPSCK duty cycle)	Slave	$t_{SPSCK}/2-3$	$t_{SPSCK}/2+3$	$t_{SPSCK}/2-3$	$t_{SPSCK}/2+3$	ns
			Master					
6	t_{SU}	Data setup time(inputs)	Slave	9	-	11	-	ns
			Master	29	-	38	-	
7	t_{HI}	Data hold time(inputs)	Slave	7	-	9	-	ns
			Master	0	-	0	-	
8	t_a	Slave access time	Slave	-	29+（3*1000/f_{periph}）	-	38+（3*1000/f_{periph}）	ns
9	t_{dis}	Slave MISO (SOUT) disable time	Slave	-	29+（3*1000/f_{periph}）	-	38+（3*1000/f_{periph}）	ns
10	t_v	Data valid (after SPSCK	Slave	-	25	-	34	ns
			Master	-	12	-	16	

Num	Symbol	Description	Conditions	Run Mode				Unit
				5.0 V IO		3.3 V IO		
				Min.	Max.	Min.	Max.	
		edge)						
11	t_{HO}	Data hold time(outputs)	Slave	22	-	22	-	ns
			Master	2	-	2	-	
12	$t_{RI/FI}$	Rise/Fall time input	Slave	-	t_{periph} – 6	-	t_{periph} – 11	ns
			Master	-	-	-	-	
13	$t_{RO/FO}$	Rise/Fall time output	Slave	-	6	-	11	ns
			Master	-	-	-	-	

1. Trace length should not exceed 11 inches for SCK pad when used in Master loop-back mode.
2. f_{periph} = SPI peripheral clock
3. $t_{periph} = 1/f_{periph}$
4. This maximum operating frequency (fop) is 10 MHz.
5. Set the PCSSCK configuration bit as 0, for a minimum of 1 delay cycle of SPI baud rate clock, where PCSSCK ranges from 0 to 255.
6. Set the SCKPCS configuration bit as 0, for a minimum of 1 delay cycle of SPI baud rate clock, where SCKPCS ranges from 0 to 255.
7. While selecting odd dividers, ensure Duty Cycle is meeting this parameter.

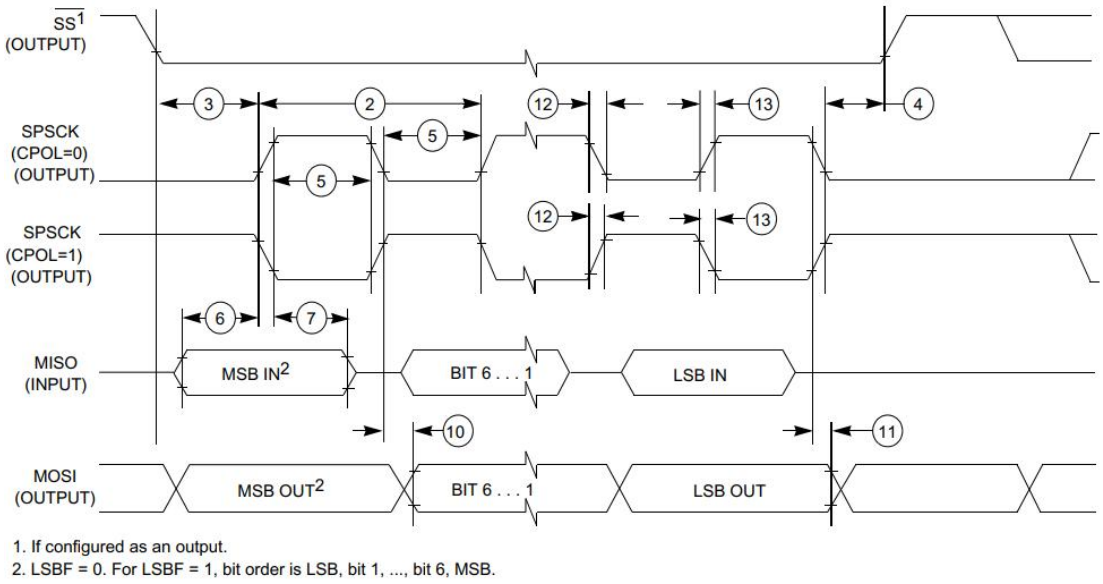

Figure 9. SPI master mode timing (CPHA = 0)

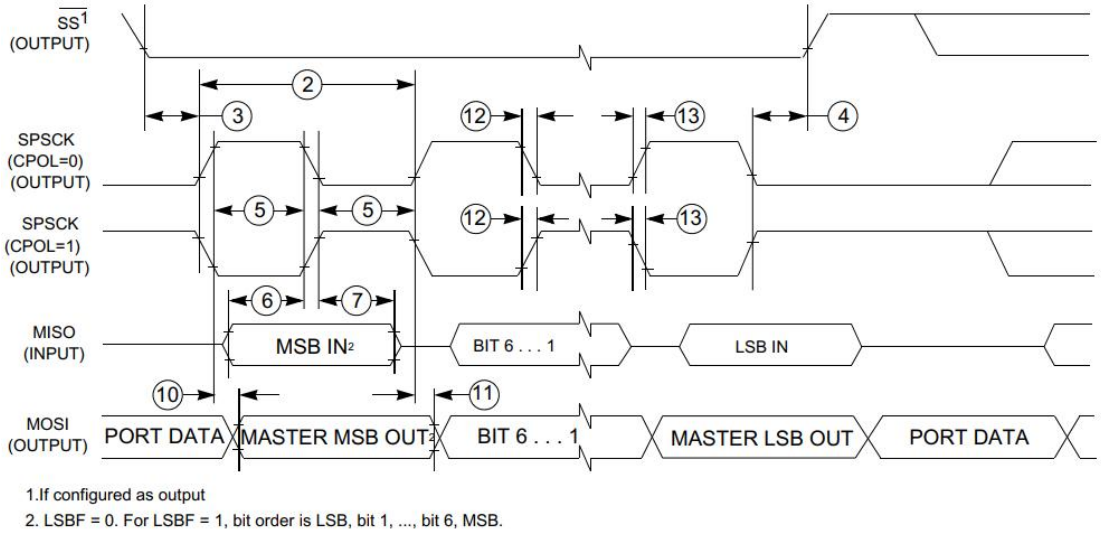

Figure 10. SPI master mode timing (CPHA = 1)

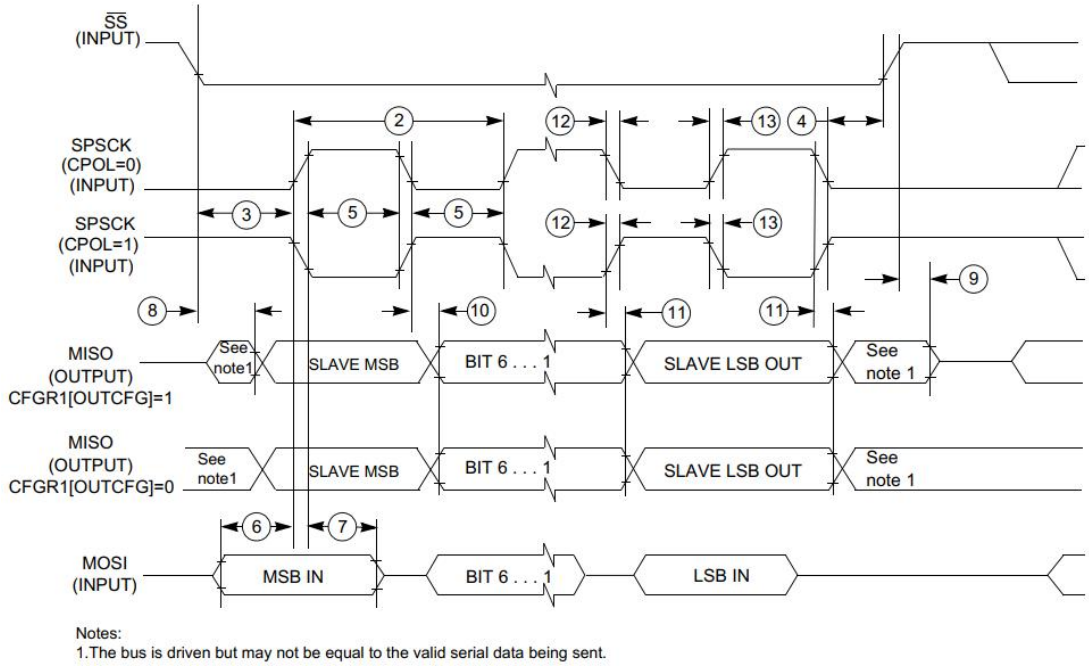

Figure 11. SPI slave mode timing (CPHA = 0)

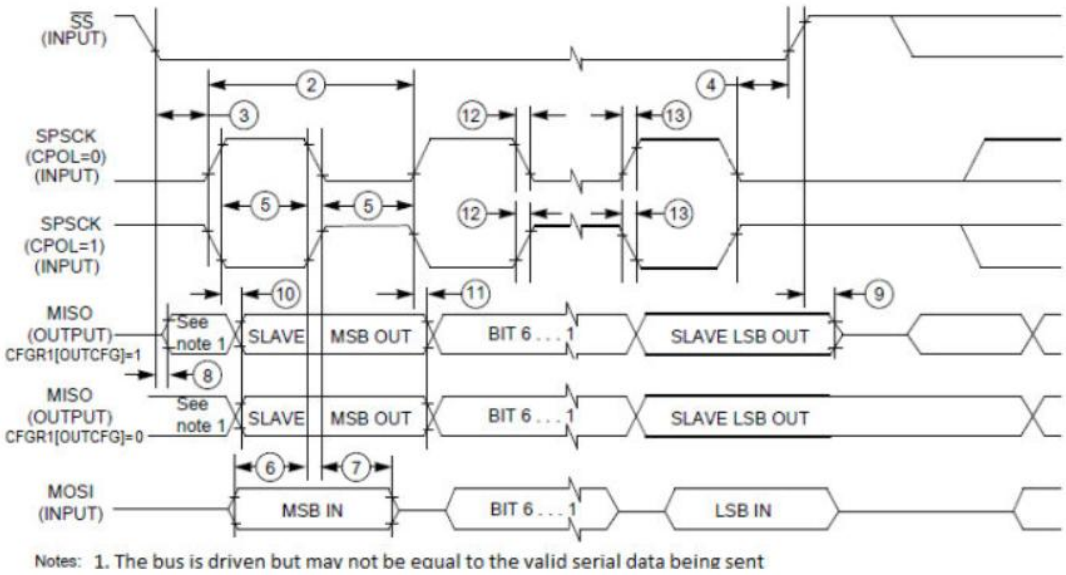

Figure 12. SPI slave mode timing (CPHA = 1)

4.5.3 I2C electrical specifications

See General AC specifications for LPI2C specifications.

For supported baud rate, see section 'Inter-Integrated Circuit (I2C)' of the *Reference Manual*.

4.5.4 CAN electrical specifications

For supported baud rate, see section 'Protocol timing' of the *Reference Manual*

4.5.5 Clock-out frequency

The maximum supported clock out frequency for this device is 15 MHz.

4.6 Debug modules

4.6.1 SWD electrical specifications

Table 30. SWD electrical specifications

Symbol	Description	Run Mode				Unit
		5.0 V IO		3.3 V IO		
		Min.	Max.	Min.	Max.	

Symbol	Description	Run Mode				Unit
		5.0 V IO		3.3 V IO		
		Min.	Max.	Min.	Max.	
S1	SWD_CLK frequency of operation	-	20	-	20	MHz
S2	SWD_CLK cycle period	1/S1	-	1/S1	-	ns
S3	SWD_CLK clock pulse width	S2/2 – 5	S2/2 + 5	S2/2 – 5	S2/2 + 5	ns
S4	SWD_CLK rise and fall times	-	1	-	1	ns
S9	SWD_DIO input data setup time to SWD_CLK rise	5	-	5	-	ns
S10	SWD_DIO input data hold time after SWD_CLK rise	5	-	5	-	ns
S11	SWD_CLK high to SWD_DIO data valid	-	30	-	40	ns
S12	SWD_CLK high to SWD_DIO high-Z	-	30	-	40	ns
S13	SWD_CLK high to SWD_DIO data invalid	0	-	0	-	ns

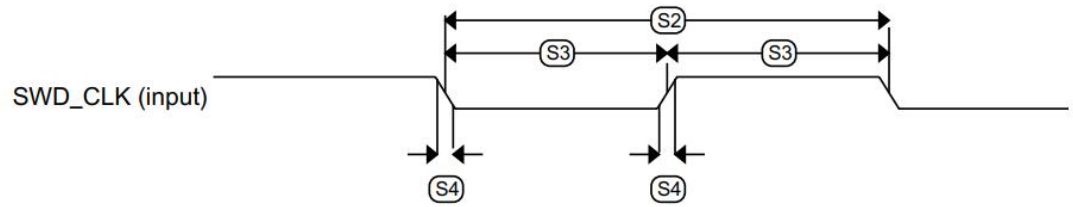

Figure 13. Serial wire clock input timing

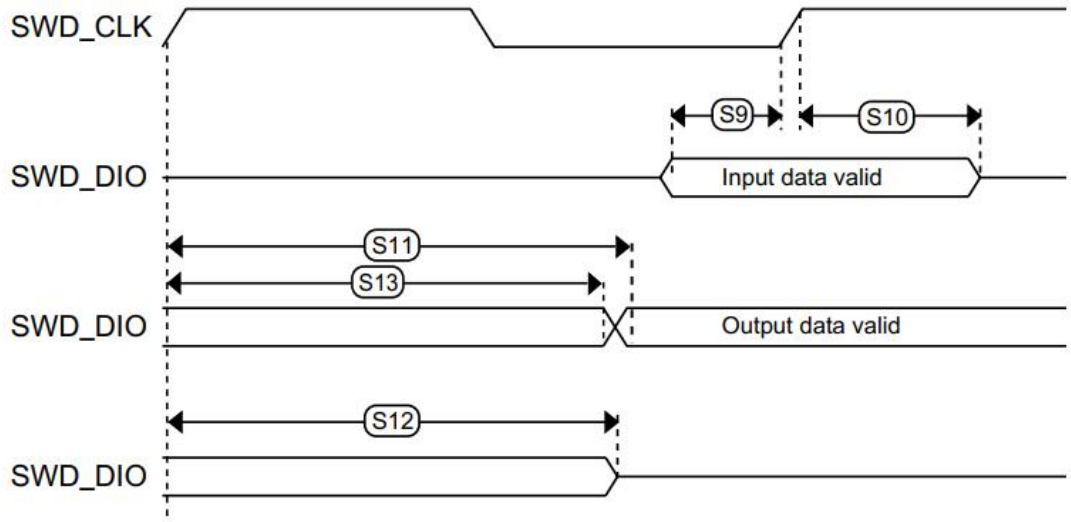

Figure 14. Serial wire data timing

5 Thermal attributes

5.1 Description

The table in the following section describes the thermal characteristics of the device.

NOTE

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting side (board) temperature, ambient temperature, air flow, power dissipation or other components on the board, and board thermal resistance.

5.2 Thermal characteristics

Table 31. Thermal characteristics for 48/64-pin LQFP package

Rating	Conditions	Symbol	Package	Values (in °C/W)
				Z20K118
Thermal resistance, Junction to Ambient (Natural Convection)[1, 2]	Four layer Board (2s2p)	$R_{\theta JA}$	48	63.04
			64	55.3
Thermal resistance, Junction to Package Top[1, 3]	Natural Convection	Ψ_{JT}	48	0.84
			64	0.8

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board construction.

2. Determined according to JEDEC Standard JESD51-2.
3. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2.

The thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top of the package case using the following equation:

$T_J = T_T + \Psi_{JT}$ x chip power dissipation

where T_T is the thermocouple temperature at the top of the package.

6 Package information

6.1 48-pin products

Table 32. 48-pin product

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	---	1.45
LEAD WIDTH(PLATING)		b	0.17	---	0.27
LEAD WIDTH		b1	0.17	---	0.23
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
	X	D	9 BSC		
	Y	E	9 BSC		
BODY SIZE	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.5 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.08		
MOLD FLATNESS		eee	0.05		

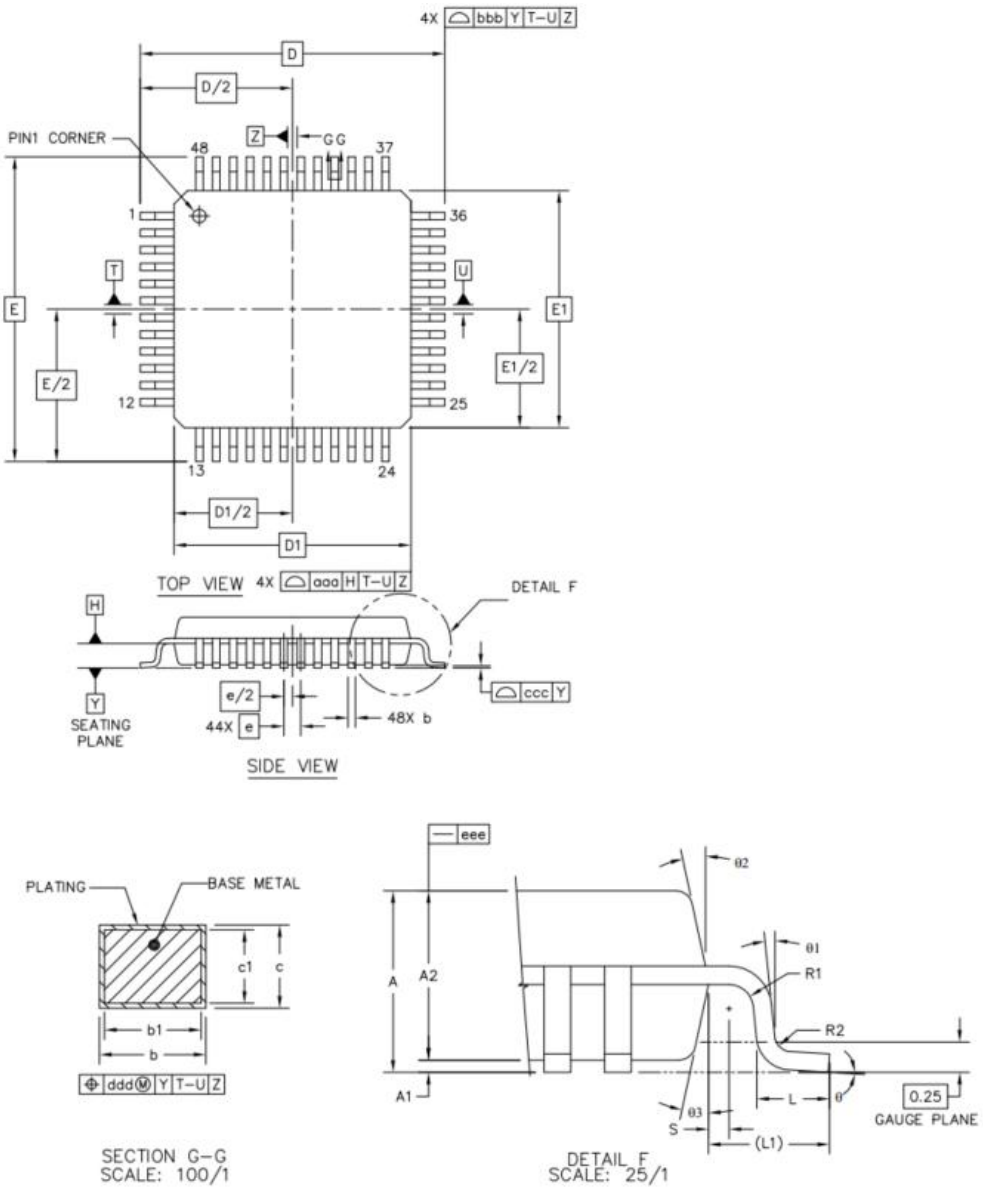

Figure 15. 48-pin products

6.2 64-pin products

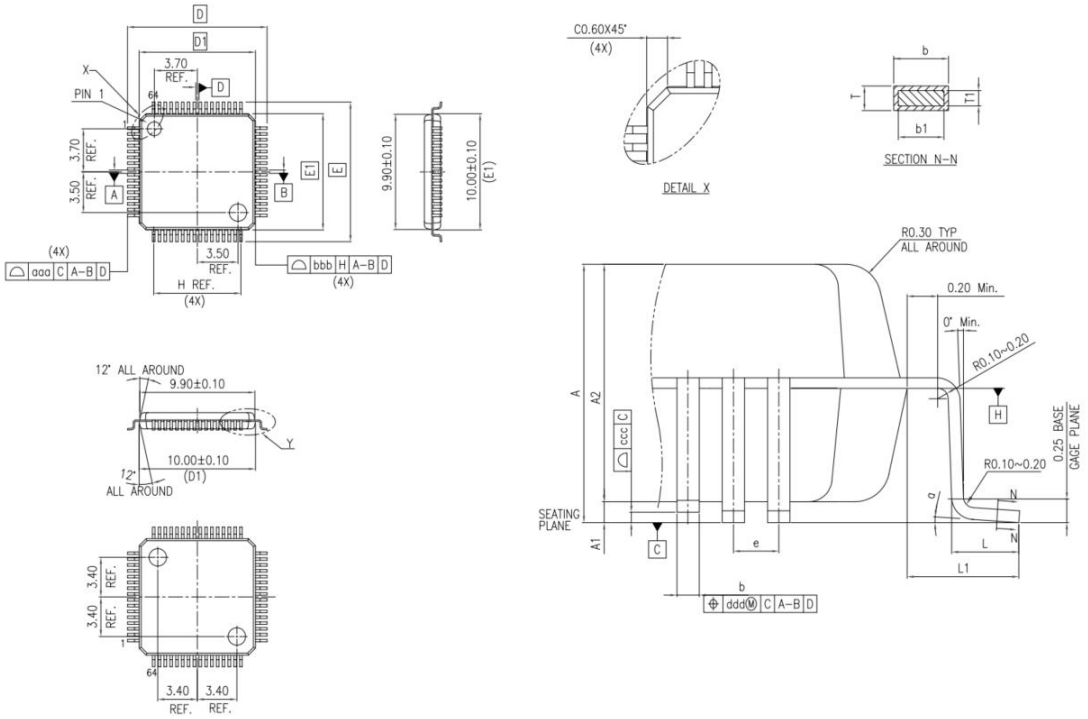

Figure 16. 64-pin products

Table 33. 64-pin product

	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	---	---	1.6
STAND OFF	A1	0.05	---	0.15
MOLD THICKNESS	A2	1.35	---	1.45
LEAD TIP TO TIP	D	11.8	---	12.2
LEAD TIP TO TIP	E	11.8	---	12.2
PKG LENGTH	D1	9.9	---	10.1
PKG WIDTH	E1	9.9	---	10.1
LEAD PITCH	e	0.5 BSC		
FOOT LENGTH	L	0.45	0.6	0.75
FOOTPRINT	L1	1 REF		
LEAD THICKNESS	T	0.09	---	0.2
LEAD BASE METAL THICKNESS	T1	0.097	---	0.157
FOOT ANGLE	a	0°	3.5°	7°
LEAD WIDTH	b	0.17	---	0.27
LEAD BASE METAL WIDTH	b1	0.17	---	0.23
PROFILE OF LEAD TIPS	aaa	0.2		
PROFILE OF MOLD SURFACE	bbb	0.2		
FOOT COPLANARITY	ccc	0.08		
FOOT POSITION	ddd	0.08		
CUM. LEAD PITCH	H(REF.)	7.5		

6.3 32-pin products

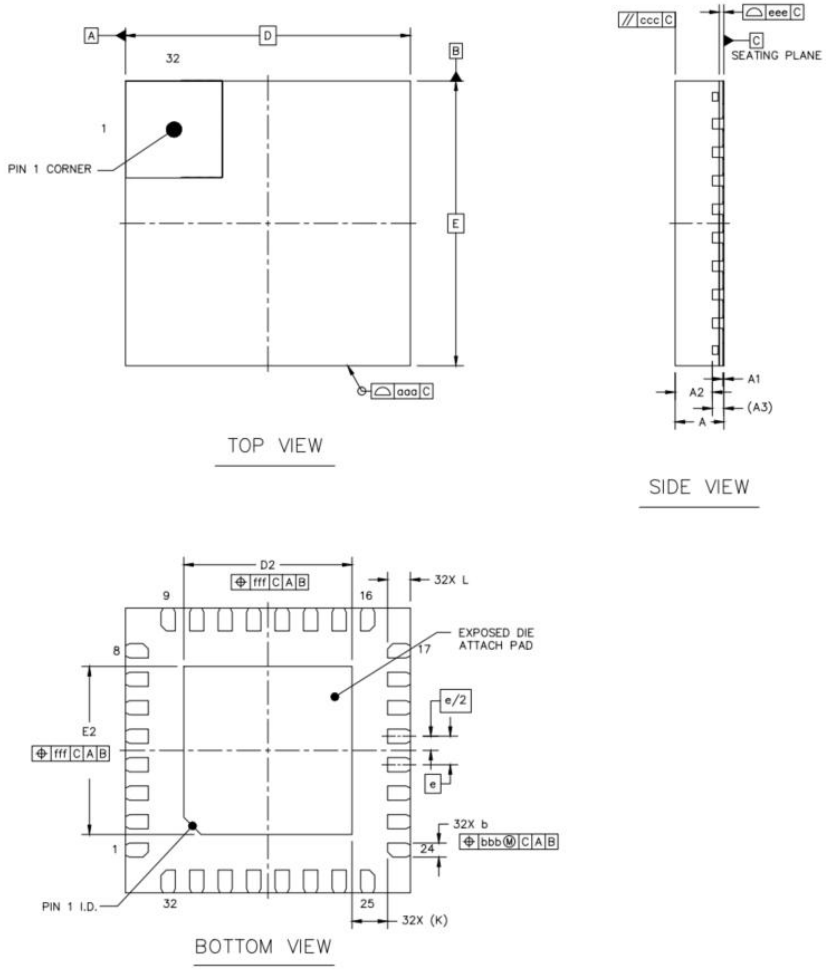

Figure 17. 32-pin products

Table 34. 32-pin product

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	—	0.65	—
L/F THICKNESS		A3	0.203 REF		
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D	5 BSC		
	Y	E	5 BSC		
LEAD PITCH		e	0.5 BSC		
EP SIZE	X	D2	2.85	2.95	3.05
	Y	E2	2.85	2.95	3.05

LEAD LENGTH	L	0.35	0.4	0.45
LEAD TIP TO EXPOSED PAD EDGE	K	0.625 REF		
PACKAGE EDGE TOLERANCE	aaa	0.1		
MOLD FLATNESS	ccc	0.1		
COPLANARITY	eee	0.08		
LEAD OFFSET	bbb	0.1		
EXPOSED PAD OFFSET	fff	0.1		

Appendix A

Feature comparison

This summarizes the memory, peripherals and packaging options for the Z20K11xM devices. All devices which share a common package are pin-to-pin compatible.

		Z20K11xM		
	Parameter	K114M	K116M	K118M
	Core	ARM® Cortex®-M0+ core		
	Frequency	64MHz	64MHz	64MHz
System	CRC module	1x		
	Peripheral speed	up to 64 MHz		
	Crossbar	●		
	DMA	●		
	External Watchdog Detect Timer (EWDT)	●		
	Memory protection unit (MPU)	●		
	Watchdog	1x		
	System Control module (SCM)	●		
	System reset and mode controller (SRMC)	●		
	AHB to APB Peripheral bridge (AHB-APB)	●		
	Power management unit (PMU)	●		
	Low power modes	●		
	HardwareDivider(HWDIV)	●		
	Number of I/Os	up to 40	up to55	up to 55
	Single supply voltage	2.97 - 5.5 V		
	Ambient Operation Temperature (Ta)	-40℃ to +125℃		
Memory	Program flash memory	64 KB	128 KB	256 KB
	Data flash memory	64 KB	128 KB	128 KB

	Error Correcting Code (ECC)	●		
	System RAM	8 KB	16 KB	32 KB
	Regfile	32 x 32Bit		
	EEPROM	Emulated by Data flash		
Timer	System Timer	1x (4ch 32bit)	1x (4ch 32bit)	1x (4ch 32bit)
	Timer	3x (8ch 16bit)	3x (8ch 16bit)	3x (8ch 16bit)
	Real Time Counter (RTC)	1x	1x	1x
	Trigger delay generator (TDG)	1x	1x	1x
Analog	Trigger mux (TMU)	●		
	12-bit SAR ADC (1 Msps each)	1x (15ch)	1x (18ch)	1x (18ch)
	Comparator with 8-bit DAC	1x (7ch)	1x (11ch)	1x (11ch)
Communication	UART and LIN (UART)	3x	3x	4x
	Serial peripheral interface (SPI)	2x	2x	3x
	Inter-integrated circuit (I2C)	1x	1x	2x
	Control area network (CAN)	1x(1x with FD)	1x(1x with FD)	2x(2x with FD)
IDE	Debug	SWD	SWD	SWD
	Ecosystem (IDE, compiler, debugger)	IAR, GHS, Arm®, Lauterbach		
Other	Packages	32-pin QFN 48-pin LQFP	32-pin QFN 48-pin LQFP 64-pin LQFP	48-pin LQFP 64-pin LQFP

LEGEND:

○ Not implemented

● Available on the device

Appendix B

Memory map

This appendix contains various memories and memory-mapped peripherals that are located in one 32-bit contiguous memory space. This chapter describes the memory and peripheral locations within that memory space.

	Z20K11xM								
	K114M			K116M			K118M		
Memory	**Size (KB)**	**Start Address (hex)**	**End Address (hex)**	**Size (KB)**	**Start Address (hex)**	**End Address (hex)**	**Size (KB)**	**Start Address (hex)**	**End Address (hex)**
Program flash memory	64	00000000	0000FFFF	128	00000000	0001FFFF	256	00000000	0003FFFF
Data flash memory	64	01000000	0100FFFF	128	01000000	0101FFFF	128	01000000	0101FFFF
SRAM	8	20000000	20001FFF	16	20000000	20003FFF	32	1FFFC000	20003FFF
Peripheral Instance	**Size (KB)**	**Start Address (hex)**	**End Address (hex)**	**Size (KB)**	**Start Address (hex)**	**End Address (hex)**	**Size (KB)**	**Start Address (hex)**	**End Address (hex)**
DMA	4	40008000	40008FFF	4	40008000	40008FFF	4	40008000	40008FFF
Flash	4	40020000	40020FFF	4	40020000	40020FFF	4	40020000	40020FFF
DMAMUX	4	40022000	40022FFF	4	40022000	40022FFF	4	40022000	40022FFF
CAN 0	4	40024000	40024FFF	4	40024000	40024FFF	4	40024000	40024FFF
ADC	4	40026000	40026FFF	4	40026000	40026FFF	4	40026000	40026FFF
RTC	4	40028000	40028FFF	4	40028000	40028FFF	4	40028000	40028FFF
CAN 1	Reserved			Reserved			4	4002A000	4002AFFF

SPI 0	4	4002C000	4002CFFF	4	4002C000	4002CFFF	4	4002C000	4002CFFF
SPI 1	4	4002D000	4002DFFF	4	4002D000	4002DFFF	4	4002D000	4002DFFF
SPI 2	Reserved			Reserved			4	4002E000	4002EFFF
REGFILE	4	40034000	40034FFF	4	40034000	40034FFF	4	40034000	40034FFF
TDG	4	40035000	40035FFF	4	40035000	40035FFF	4	40035000	40035FFF
TMU	4	40036000	40036FFF	4	40036000	40036FFF	4	40036000	40036FFF
TIM 0	4	40038000	40038FFF	4	40038000	40038FFF	4	40038000	40038FFF
TIM 1	4	40039000	40039FFF	4	40039000	40039FFF	4	40039000	40039FFF
TIM 2	4	4003A000	4003AFFF	4	4003A000	4003AFFF	4	4003A000	4003AFFF
STIM	4	40040000	40040FFF	4	40040000	40040FFF	4	40040000	40040FFF
CRC	4	40043000	40043FFF	4	40043000	40043FFF	4	40043000	40043FFF
SCM	4	40048000	40048FFF	4	40048000	40048FFF	4	40048000	40048FFF
Port A	4	40049000	40049FFF	4	40049000	40049FFF	4	40049000	40049FFF
Port B	4	4004A000	4004AFFF	4	4004A000	4004AFFF	4	4004A000	4004AFFF
Port C	4	4004B000	4004BFFF	4	4004B000	4004BFFF	4	4004B000	4004BFFF
Port D	4	4004C000	4004CFFF	4	4004C000	4004CFFF	4	4004C000	4004CFFF
Port E	4	4004D000	4004DFFF	4	4004D000	4004DFFF	4	4004D000	4004DFFF
WDOG	4	40052000	40052FFF	4	40052000	40052FFF	4	40052000	40052FFF

EWDT	4	40061000	40061FFF	4	40061000	40061FFF	4	40061000	40061FFF
SCC	4	40064000	40064FFF	4	40064000	40064FFF	4	40064000	40064FFF
PARCC	4	40065000	40065FFF	4	40065000	40065FFF	4	40065000	40065FFF
I2C 0	4	40066000	40066FFF	4	40066000	40066FFF	4	40066000	40066FFF
I2C 1	Reserved			Reserved			4	40067000	40067FFF
UART 0	4	4006A000	4006AFFF	4	4006A000	4006AFFF	4	4006A000	4006AFFF
UART 1	4	4006B000	4006BFFF	4	4006B000	4006BFFF	4	4006B000	4006BFFF
UART 2	4	4006C000	4006CFFF	4	4006C000	4006CFFF	4	4006C000	4006CFFF
UART 3	Reserved			Reserved			4	4006D000	4006DFFF
CMP	4	40073000	40073FFF	4	40073000	40073FFF	4	40073000	40073FFF
PMU	4	4007D000	4007DFFF	4	4007D000	4007DFFF	4	4007D000	4007DFFF
SRMC	4	4007E000	4007EFFF	4	4007E000	4007EFFF	4	4007E000	4007EFFF
HWDIV	4	400FE000	400FEFFF	4	400FE000	400FEFFF	4	400FE000	400FEFFF
GPIO	4	400FF000	400FFFFF	4	400FF000	400FFFFF	4	400FF000	400FFFFF
RGPIO	4	F8000000	F8000FFF	4	F8000000	F8000FFF	4	F8000000	F8000FFF

7 Revision history

The following table provides a revision history for this document.

Table 35. Revision History

Rev. No.	Date	Substantial Changes
1	6 August 2021	Rev. 1.0
1.1	6 August 2021	Rev. 1.1 Correct 64pin package dimension Update flash command timing, add 2us tolerance for each item Update fbus max-frequency to 64MHz Update IO drive strength
1.2	22 Dec 2021	Rev 1.2 Add comments for DAC linearity result Add comments for ADC linearity result Add comments for boot capacitors placement and layout Increase LPO32K, FIRC frequency deviation Modify DAC INL and DNL range Change min voltage from 2.7V to 2.97V
1.3	10 Mar 2022	Rev 1.3 Remove some TBD fields
1.4	27 Apr 2022	Rev 1.4 Add Thermal handling ratings table and Moisture handling ratings
1.5	Oct 2022	Rev 1.5 Add Z20K114M device(Z20K114MCMHL, Z20K114MCMFL, Z20K114MCMCN) Add feature comparison table Add memory map comparison table Change 32pinLQFP product package to 32pinQFN package Add 48pin decouple figure
1.6	Apr 2023	Modify t_{por}(POR to 1st instruction) and wake up time from Standby to run mode Update SPI maximum baudrate Add package information for 32-pin QFN Remove K114 related information
1.6.1	May 2023	Add 114 part feature list and memory compare information Add Fig4 for device operations supply range

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