



**Genesys Logic, Inc.**

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# **GL3232S**

## **USB 3.1 GEN1 to SD 4.0 Memory Card Reader Controller**

### **Datasheet**

**Revision 1.04  
Mar. 11, 2020**



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## Revision History

Revision	Date	Description
1.00	07/19/2018	Formal release
1.01	01/11/2019	Update CH2 Features
1.02	07/10/2019	1. Add CH5.5 IC ESD/LU Level 2. Add CH5.6 Thermal information
1.03	11/22/2019	Update Table 6.1 - SPI NOR Flash Support List
1.04	03/11/2020	Update Table 3.1 – Power I/O description

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## CHAPTER 1 GENERAL DESCRIPTION

GL3232S is an USB 3.1 GEN1 to SD 4.0 Single LUN Memory Card Reader Controller.

GL3232S supports various types of SD memory cards, such as Secure Digital™ (SD), SDHC, miniSD and microSD (T-Flash), MultiMediaCard™ (MMC), RS-MMC, MMCmicro and MMCmobile. It also supports high density memory cards (Capacity up to 2TB), such as SDXC, ultra high speed memory cards, SD3.0 UHS-I and the latest generation high speed memory cards SD4.0 UHS-II card. GL3232S also supports SANDISK EXTREME® 160 MB/s microSD UHS-I CARD.

The GL3232S integrates a high speed 8051 microprocessor and a high efficiency hardware engine for the best data transfer performance between USB and various memory card interfaces. It supports ISP (In System Programming) for firmware upgrade from the external SPI Flash via USB port. It integrates 5V to 3.3V and 3.3V to 1.2V regulators and power MOSFETs which can reduce system BOM cost. It also integrates 5V to 1.2V DC-DC as alternative to improve the power efficiency.

## **CHAPTER 2 FEATURES**

- USB specification compliance
  - Comply with Universal Serial Bus 3.1 Specification (USB 3.1 GEN1)
  - Comply with Universal Serial Bus Specification rev. 2.0 (USB 2.0)
  - Comply with USB Mass Storage Class Specification rev. 1.0
  - Support USB Mass Storage Class Bulk-Only Transport (BOT)
  - Support 1 device address and up to 3 endpoints: Control (0) / Bulk Data Read In (1) / Bulk Data Write Out (2)
  - Support 5 Gbps/SuperSpeed, 480 Mbps/high-speed, and 12 Mbps/full-speed transfer rates
- Integrated USB building blocks
  - SuperSpeed USB/USB 2.0 transceiver macro (UTM), Serial Interface Engine (SIE), and embedded Power-On Reset (POR)
- Embedded high speed 8051 micro-controller
- High efficiency hardware DMA engine improves data transfer performance between USB and flash card interfaces
- Support Secure Digital™ v1.0 / v1.1 / v2.0/ SDHC / SDXC (capacity up to 2TB)
- Support Secure Digital™ v3.0 UHS-I (Ultra High Speed): SDR12/SDR25/SDR50/DDR50/SDR104
- Support Secure Digital™ v4.0 UHS-II: Full Duplex Mode and Half Duplex Mode
- Support DDR200 speed mode to enhance the UHS-I performance
- Support SANDISK EXTREME® 160 MB/s microSD UHS-I CARD
- Support MultiMediaCard™ (MMC)
  - MMC specification v3.x / v4.0 / v4.1 / v4.2 / v4.3 / v4.4
  - x1 / x4 bit data bus
- Support HUAWEI Nano Memory Card
- Support ISP (In System Programming) for firmware upgrade from the external SPI Flash via USB port
- On-Chip power MOSFETs for supplying flash media card power
- On-chip 5V to 3.3V and 3.3V to 1.2V regulator
- On-chip 5V to 1.2V DC-DC to improve power efficiency.
- Support Over-Current protection mechanism
- Support USB 2.0 LPM (Link Power Management)
- Support USB 3.1 GEN1 LTM (Latency Tolerance Messaging)
- Support USB 3.1 GEN1 U1/U2/U3 low power link state
- Support Latency Tolerance Messaging
- Support remote wakeup function
- Support Intel Power Optimizer
- Support Windows Connected Standby
- Support Spread Spectrum Clock for SD to reduce EMI effect
- Available in QFN48 pin package (6x6mm)

## CHAPTER 3 PIN ASSIGNMENT

### 3.1 QFN 48 Pinout

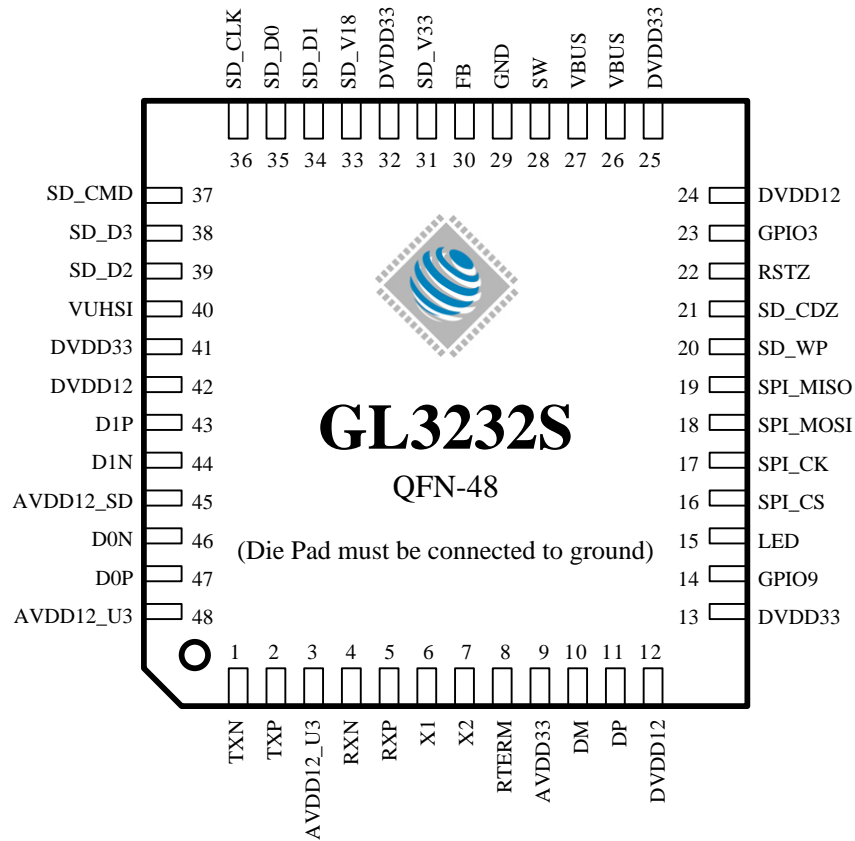


Figure 3.1 - QFN 48 Pinout Diagram



## 3.2 Pin Description

**Table 3.1 - Pin Description**

Pin Name	QFN 48 Pin	Type	Description
<b>Power/Ground</b>			
AVDD12_U3	3, 48	P, I	Analog 1.2V power source to USB 3.1 GEN1 PHY
AVDD12_SD	45	P, I	Analog 1.2V power source to SD
AVDD33	9	P, I	Analog 3.3V power source
DVDD12	12, 42	P, I	Digital 1.2V power input
	24	P, I/O	LDO mode : digital 1.2V power source DC-DC mode : digital 1.2V power input
DVDD33	13,25,32	P, O	Digital 3.3V power source
	41	P, I	Digital 3.3V power input
VBUS	26, 27	P, I	5V power source
FB	30	P, I	Feedback pin, connected to 1.2V output
SW	28	P, O	Switch out of 5V to 1.2V DC-DC
VUHSI	40	P, O	UHS-I IO PAD Power, the power source of this pin comes from the internal regulator of GL3232S and no need of external power input
SD_V18	33	P, O	Card Power 200mA for UHS-II card only
SD_V33	31	P, O	Card power 600mA
GND	29	P	Ground
<b>USB PHY Interface</b>			
DP	11	A	USB 2.0 D+
DM	10	A	USB 2.0 D-
TXN	1	A	USB 3.1 GEN1 TX-
TXP	2	A	USB 3.1 GEN1 TX+
RXN	4	A	USB 3.1 GEN1 RX-
RXP	5	A	USB 3.1 GEN1 RX+
RTERM	8	A	USB reference resistor. This pin is used to control the level of USB signal. A 680ohm, 1% resistor is recommended to be populated between RTERM and GND
X1	6	I	25MHz XTAL input. It can be connected to external 25MHz clock input
X2	7	B	25MHz XTAL output
<b>Memory Card Interface</b>			
D1P	43	A	UHS-II D1+
D1N	44	A	UHS-II D1-
D0N	46	A	UHS-II D0-
D0P	47	A	UHS-II D0+

SD_CDZ	21	I, pu	SD card detect 0: Card insert 1: No card Internal pull-up to DVDD33(3.3V)
SD_D1	34	B	SD_DATA1/ RCLKON(UHS-II Clock Output)
SD_D0	35	B	SD_DATA0/ RCLKOP(UHS-II Clock Output)
SD_CLK	36	O	SD clock
SD_CMD	37	B	SD command/response
SD_D3	38	B	SD_DATA3
SD_D2	39	B	SD_DATA2
SD_WP	20	I, pu	SD write protect 0: write enable 1: write protection Internal pull-up to DVDD33(3.3V)
<b>Others</b>			
LED	15	O	Card Access LED
SPI_CS	16	O	SPI interface: chip select
SPI_CK	17	O	SPI interface: clock
SPI_MOSI	18	O	SPI interface: connect to SPI flash data input
SPI_MISO	19	I	SPI interface: connect to SPI flash data output
RSTZ	22	I, pu	Chip reset, active low Internal pull-up to DVDD33(3.3V)
GPIO	14,23	B	General purpose I/O

**Notation:**

<b>Type</b>	<b>O</b>	Output
	<b>I</b>	Input
	<b>B</b>	Bi-directional
	<b>pu</b>	internal pull-up when input
	<b>pd</b>	internal pull-down when input
	<b>P</b>	Power / Ground
	<b>A</b>	Analog

## CHAPTER 4 BLOCK DIAGRAM

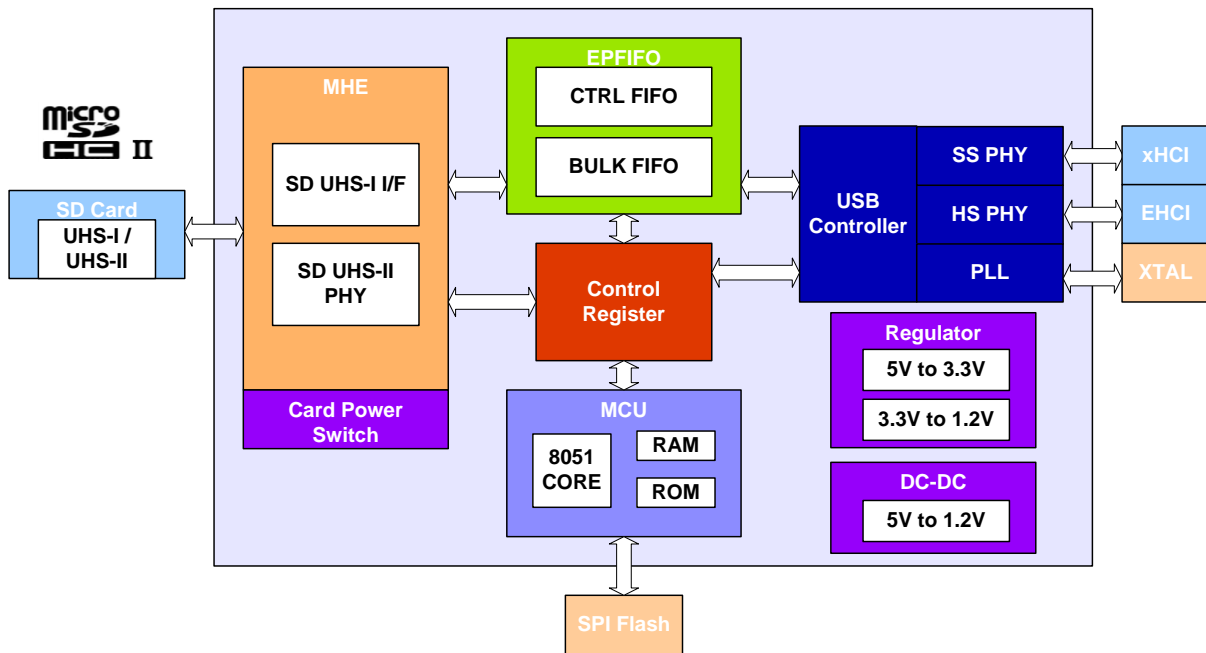


Figure 4.1 - Functional Block Diagram

### 4.1 Super Speed and HS PHY

The transceiver macro is the analog circuitry that handles the low level USB protocol and signaling, and shifts the clock domain of the data from the USB to one that is compatible with the general logic.

### 4.2 USB Controller

The USB Controller, which contains the USB PID and address recognition logic, and other sequencing and state machine logic to handle USB packets and transactions.

### 4.3 EPFIFO

Endpoint FIFO includes Control FIFO (FIFO0) and Bulk In/Out FIFO

- **CTRL FIFO** FIFO of control endpoint 0. It is 512-byte FIFO and used for endpoint 0 data transfer.
- **Bulk In/Out FIFO** It can be in the TX mode or RX mode:
  1. It can be transmit/receive 512-byte data of USB 2.0 and 1K-byte data of USB 3.1 GEN1 continuously.
  2. It can be directly accessed by micro-controller

#### **4.4 MCU**

8051 micro-controller inside.

- **8051 Core** Compliant with Intel 8051 high speed micro-controller
- **ROM** Firmware code on ROM
- **RAM** Internal RAM area for MCU access

#### **4.5 MHE (Media Hardware Engine)**

Media Interface: SD/MMC

#### **4.6 Regulator**

- **5V to 3.3V** 3.3V Power Source
- **3.3V to 1.2V** 1.2V Power Source

#### **4.7 DC-DC**

- **5V to 1.2V** 1.2V Power Source to analog

#### **4.8 UHS-II PHY**

The UHS-II PHY Layer handles the low level UHS-II protocol and signal.

## CHAPTER 5 ELECTRICAL CHARACTERISTICS

### 5.1 Temperature Conditions

Table 5.1 - Temperature Conditions

Parameter	Value
Storage Temperature	-65°C to +150 °C
Operating Temperature	0°C to +70 °C

### 5.2 Operating Conditions

Table 5.2 - Operating Conditions

Parameter	Value
Supply Voltage	+4.75V to +5.25V
Ground Voltage	0V
F <sub>OSC</sub> (Oscillator or Crystal Frequency)	25 MHz ± 0.03%

### 5.3 DC Characteristics

Table 5.3 - DC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply Voltage		4.75	5.0	5.25	V
V <sub>IH</sub>	Input High Voltage		2.0			V
V <sub>IL</sub>	Input Low Voltage				0.4	V
I <sub>I</sub>	Input Leakage Current	0 < V <sub>IN</sub> < DVDD	-10		10	μA
V <sub>OH</sub>	Output High Voltage	DVDD = 3.3V	2.8			V
V <sub>OL</sub>	Output Low Voltage				0.4	V
I <sub>OH</sub>	Output Current High			8		mA
I <sub>OL</sub>	Output Current Low			8		mA
C <sub>IN</sub>	Input Pin Capacitance			5		pF
*I <sub>NORMAL</sub>	HS mode			35		mA
	SS mode	U0 state		46		mA
		U1 state		14		mA
		U2 state		9.8		mA
*I <sub>ACTIVE</sub>	HS mode			46		mA
	SS mode	U0 state		55		mA

$I_{RESET}$			42		mA
$I_{SUS}$	HS Suspend current	1.5K pull-up included	0.80		mA
	SS Suspend current	U3 State	0.63		mA
$R_{pu}$	Reset Pad pull-up		46		K $\Omega$
	SD_CDZ, SD_WP, GPIO Pad pull-up		46		K $\Omega$
	SD_CMD pull-up		15		K $\Omega$
	SD_CLK, D[3:0] Pad pull-up		15		K $\Omega$
$R_{pd}$	SD_CMD pull-down		15		K $\Omega$
	SD_CLK, D[3:0] Pad pull-down		15		K $\Omega$
$R_{IMP}$	SD_CMD, SD_CLK, D[3:0] impedances		50		$\Omega$

\*  $I_{NORMAL}$ : The memory card is inserted but not in read/write

\*  $I_{ACTIVE}$ : The memory card is in read/write

## 5.4 AC Characteristics of Reset Timing

### 5.4.1 Reset Timing

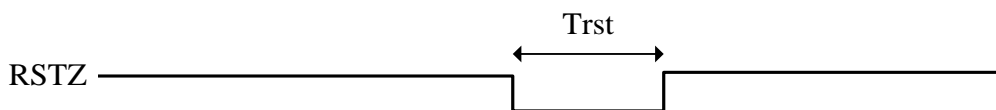


Figure 5.1 - Timing Diagram of Reset Width

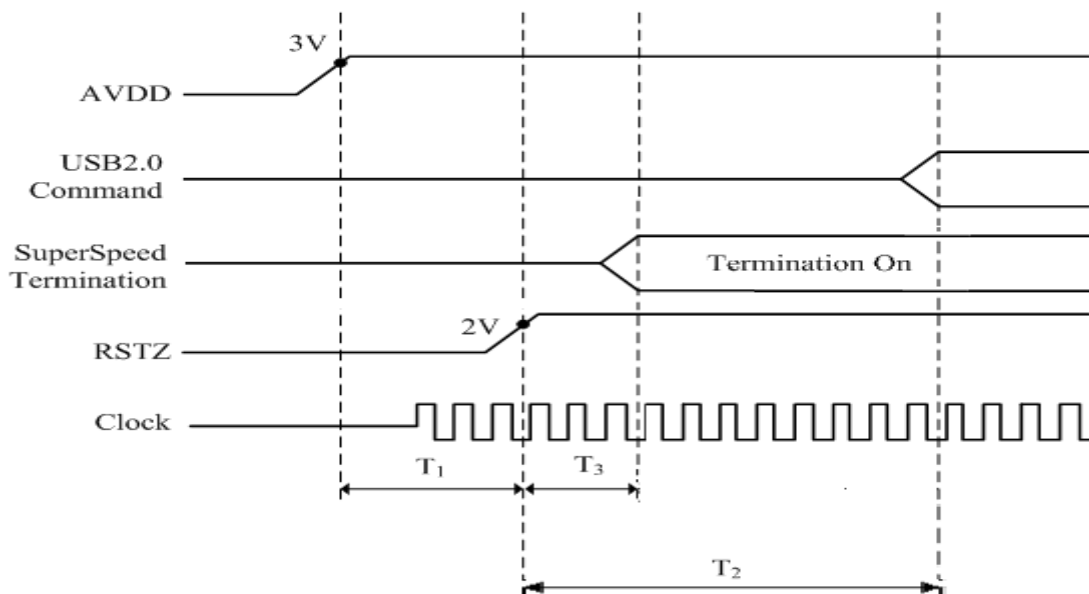


Figure 5.2 - Timing Diagram of Power-on to USB Bus Ready

**Table 5.4 - Reset Timing**

Parameter	Description	Min.	Max.	Unit
Trst	Chip reset sense timing width	2		us
T1	AVDD power up to reset de-assert	500		us
T2	Reset de-assert to respond USB2.0 command ready		100	ms
T3	Reset de-assert to SuperSpeed termination on		35	ms

## 5.4.2 SD Card Clock Frequency

**Table 5.5 - SD Card Clock Frequency**

Parameter	Description	Max.	Unit
F <sub>ID</sub>	Clock frequency Identification Mode	187	KHz
F <sub>DS</sub>	Clock frequency Default Speed Mode	25	MHz
F <sub>HS</sub>	SD Clock frequency High Speed Mode	50	MHz
F <sub>HS</sub>	MMC Clock frequency High Speed Mode	52	MHz
F <sub>SDR25</sub>	Clock frequency UHS-I Mode: SDR25	50	MHz
F <sub>DDR50</sub>	Clock frequency UHS-I Mode: DDR50	50	MHz
F <sub>SDR50</sub>	Clock frequency UHS-I Mode: SDR50	100	MHz
F <sub>SDR104</sub>	Clock frequency UHS-I Mode: SDR104	208	MHz
F <sub>DDR200</sub>	Clock frequency Ultra High Speed Mode: DDR200	200	MHz
F <sub>RCLK52</sub>	Clock frequency UHS-II Mode: Up to 1.56Gbps	52	MHz

## 5.5 IC ESD/LU Level

**Table 5.6 - IC ESD/LU Level**

Test Mode and Trigger Mode	Value
ESD HBM	± 4KV
ESD CDM	± 500V
ESD MM	± 200V
Latch-up	± 500mA

## 5.6 Thermal information

Table 5.7 - Thermal information (QFN48)

Ambient Temp ( $T_a$ )	Power (P)	Thermal Resistance ( $\Theta_{ja}$ )	Thermal Resistance ( $\Theta_{jc}$ )	Junction Temp ( $T_j$ )	Case Temp ( $T_c$ )
70°C	0.350W	33.64°C/W	5.06°C/W	81.8°C	80.0°C



## CHAPTER 6 SPI NOR FLASH SUPPORT LIST

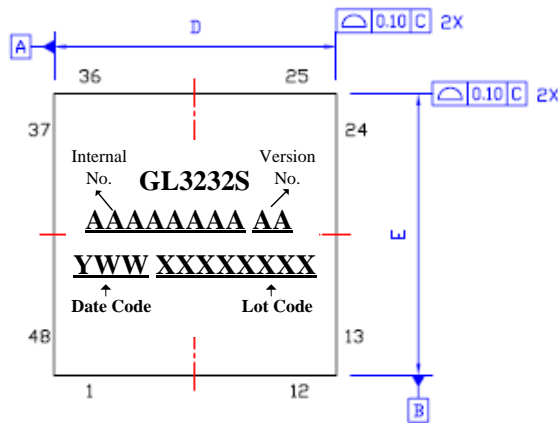
**Table 6.1 - SPI NOR Flash Support List**

Vendor	Model
GigaDevice	GD25D10B
	GD25D10C
PMC	PM25LD010
	PM25LD020
WINBOND	W25X10CL
	W25X20CL
MXIC	MX25L1006E
	MX25L4006E
ESMT	F25L01PA(86P)
	F25L01PA(100P)
FMSH	FM25F01

**Note :**

- GL3232S supports Page-Program SPI Flash only, not for Byte-program SPI Flash
- Firmware file (xxxx.bin) which provided by Genesys Logic is only used for Genesys Logic's Multi-Tool and MP Tool ISP (In System Programming via USB interface) purpose. If you would like to provide FW for SPI Flash vendor mass production or Flash ROM writer, please contact GL technical support team.

## CHAPTER 7 PACKAGE DIMENSION



SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	0.70 (27.6)	0.75 (29.5)	0.80 (31.5)
A1	---	0.02 (0.8)	0.05 (2.0)
A3	0.203 (8.0) REF		
b	0.13 (5.1)	0.18 (7.1)	0.25 (9.8)
D	6.00 (236.2) BSC		
D2	4.40 (173.2)	4.50 (177.2)	4.60 (181.1)
E	6.00 (236.2) BSC		
E2	4.40 (173.2)	4.50 (177.2)	4.60 (181.1)
e	0.40 (15.7) BSC		
L	0.30 (11.8)	0.40 (15.7)	0.50 (19.7)

NOTE: 1. REFER TO JEDEC STD. MO-220  
2. ALL DIMENSIONS IN MILLIMETERS.

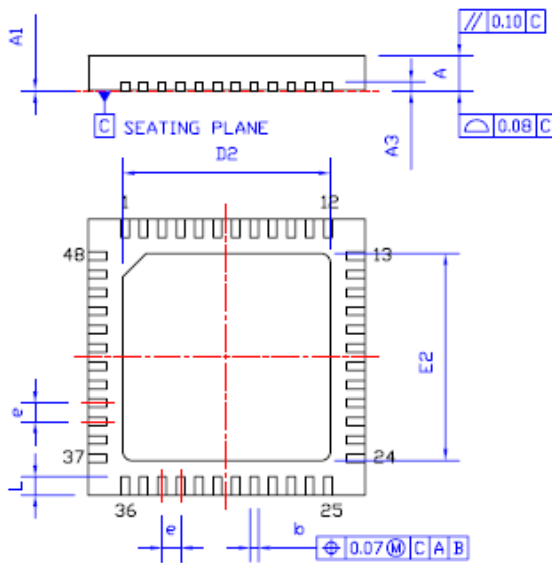


Figure 7.1 - QFN 48 Pin Package

## CHAPTER 8 ORDERING INFORMATION

**Table 8.1 - Ordering Information**

Part Number	Package	Green/Wire Material	Version	Status
GL3232S-ONYXX	QFN 48	Green Package + CU Wire	XX	MP